Amiga **CD32_R3**

Rev.1.43 (27.09.2015)



Jumpers and Stuff

DEE	TYPE	DESCRIPTION	LDACE
REF	TTPE	DESCRIPTION	PAGE
R203	SMT	PAL/NTSC COMPOSITE	4
R205	SMT	M/N-PAL COMPOSITE	4
R245	SMT	PAL SUBCARRIER	4
R246	SMT	NTSC SUBCARRIER	4
R596-9	SMT	ROM SIZE/WIDTH	3
R765	SMT	CD POWER BYPASS	6
XJ1	SMT	32 BIT ROM OPTION	3
SW1	PTH	POWER SWITCH	9

Connectors

REF	TYPE	DESCRIPTION	PAGE
CN1	DB9P	Game Controller #1	5
CN2	DB9P	Mouse Controller #2	5
CN3	RCA-J	Right Audio Output	7
CN4	RCA-J	Left Audio Output	7
CN8	DIN-4	Power Connector	9
CN9	M.DIN-4	S-Video	4
CN10	RCA-J	Composite Video	4
CN13	M.DIN-6	Keyboard	5
CN14	2mm10×1	LED/Headphone PCB	6
CN17	Flex-23	CD Drive	6
P1	Edge182	Expansion Connector	8
X2	RCA	Modulator/RF	4

Revision History

REV	DESCRIPTION	DATE	APRVL	MANAGER
0	Engineering Prototype	10/06/92	GRR	
0A	Developer/BugFix Release	01/06/93	GRR	
1	Advance Engineering Release	2/3/93	GRR	
2	Revised Per ECO 930095	03/17/93	D. Sh	annon
Α	Pilot Production Release	04/15/93	GRR	
В	Revised Per ECO 930162	05/07/93	D. Sh	annon
С	Revised Per ECO 930177 Rev3.0	05/22/93	D. Sh	annon
D	Revised Per ECO 930222	06/17/93	B. Ba	rtling
E	Revised per ECO 930238	07/20/93	Н. На	rman
F	Revised per ECO 930253			
G	Revised per ECO 930277			

Signal Glossary

SIGNAL	DESCRIPTION (AREA)	PAGES
28MHZ	28.63636 MHz Master Clock	
7MHZ	7.15909 MHz Processor Clock	
A[23:1]	Processor Address Bus (68000)	
ACK	Data Acknowledge (Parallel Port)	
AS	Address Strobe (68000)	
AUDIN	Audio Input (RS232 Port)	
AUDOUT	Audio Output (RS232 Jack)	
BEER	Bus Error (68000)	
BG	Bus Grant (68000)	
BGACK	Bus Grant Acknowledge (68000)	
BLISS	Blitter Slowdown (Chips)	
BLIT	Chip Memory Access (Chips)	
BR	Bus Request (68000)	
BUSY	Device Busy (Parallel Port)	
CASL/U	Column Address Strobe (DRAM)	
CCK/CCK0	Color Clock / Quadrature (Chips)	
CDAC	7.15909 MHz Quadrature Clock (Chips)	
CHNG	Media Change (Floppy)	
CLKRD/WR	Read-Time Clock Read / Write (RTC)	
COMP	Monochrome Composite Video (Video)	
CSYNC	Composite Sync (Video)	
CTS	Clear to Send (RS232 Port)	
D[15:0]	Processor Data Bus (68000)	
DIR	Step Direction (Floppy)	
DKRD	Disk Read Data (Floppy)	
DKWD	Disk Write Data (Floppy)	
DKWE	Disk Write Enable (Floppy)	
DMAL	Chip DMA Request Line (Chips)	
DRA[8:0]	DRAM Address Bus (DRAM)	
DRD[15:0]	DRAM Data Bus (DRAM)	
DSR	Data Set Ready (RS232 Port)	
DTACK	Data Transfer Acknowledge (68000)	
DTACK	Data Transfer Acknowledge (88000)	
E	Peripheral Enable Clock (68000)	
EXTICK	Expansion Present / RTC Tick	
FC[2:0]	Function Code (68000)	
FIRE0/1		
HLT	Fire Button 0/1 (Joysticks) Processor Halt (68000)	
	Horizontal Sync (Video)	
HSYNC		
INDEX	Index Pulse (Floppy)	
INT[2,3,6]	Interrupt Request (Chips)	
IORESET TRUES	I/O Reset	
IPL[2:0]	Interrupt Priority Level (68000)	
KBCL0CK	Keyboard Clock (Keyboard)	
KBDATA	Keyboard Data (Keyboard)	
KBRESET	Keyboard Reset (Keyboard)	
LDS/UDS	Upper / Lower Data Strobes (68000)	
LED	Power On LED / Audio Filter Disable	
LEFT/RIGHT	Left Right Audio (Audio)	1

SIGNAL	DESCRIPTION (AREA)	PAGES
LPEN	Light Pen Trigger (Joysticks)	
MTR	Motor On (Floppy)	
MTR0	Motor On - Drive 0 (Floppy)	
MOV/MOH	Mouse 0 Quadrature V/H (Joysticks)	
M1V/M1H	Mouse 1 Quadrature V/H (Joysticks)	
OVL	Overlay ROM over RAM	
OVR	Override System Decoding	
PIXELSW	Genlock Pixel Switch (Video)	
POTOX/OY	Pot Lines 0 X/Y (Joysticks)	
POT1X/1Y	Pot Lines 1 X/Y (Joysticks)	
POUT	Paper Out (Parallel Port)	
PPD[7:0]	Parallel Port Data (Parallel Port)	
RAMEN	RAM Enable (Chips)	
REGEN	Chip Register Enable (Chips)	
RAS0/1	Row Address Strobe (DRAM)	
RDY	Drive Ready (Floppy)	
RESET	General Reset	
RGA[8:1]	Register Address Bus (Chips)	
R/G/B	Red / Green / Blue (Video)	
RI	Ring Indicate (RS232 Port)	
ROMEN	ROM Enable (ROM)	
RTS	Request to Send (RS232 Port)	
RST	Processor Reset (68000)	
RXD	Receive Data (RS232 Port)	
RW	Processor Read/Write (68000)	
SEL	Select (Parallel Port)	
SEL[3:0]	Drive Select (Floppy)	
SEL[3:0]		
STEP	Side Select (Floppy) Step In/Out Command (Floppy)	
TRK0	Track Zero Sense (Floppy)	
		-
TXD	Transmit Data (RS232 Port) Valid Memory Address (68000)	
VMA		
VPA	Valid Peripheral Address (68000) Vertical Sync (Video)	
VSYNC		
WE	Write Enable (DRAM)	
WPR0T	Write Protect Sense (Floppy)	
XCLK	External Genlock Clock (Video)	
XCLKEN	External Clock Enable (Video)	
XRDY	External Data Ready	
	We Could't Could and TDE Charles and	
	** Credit Card and IDE Stuff? **	

Key Components

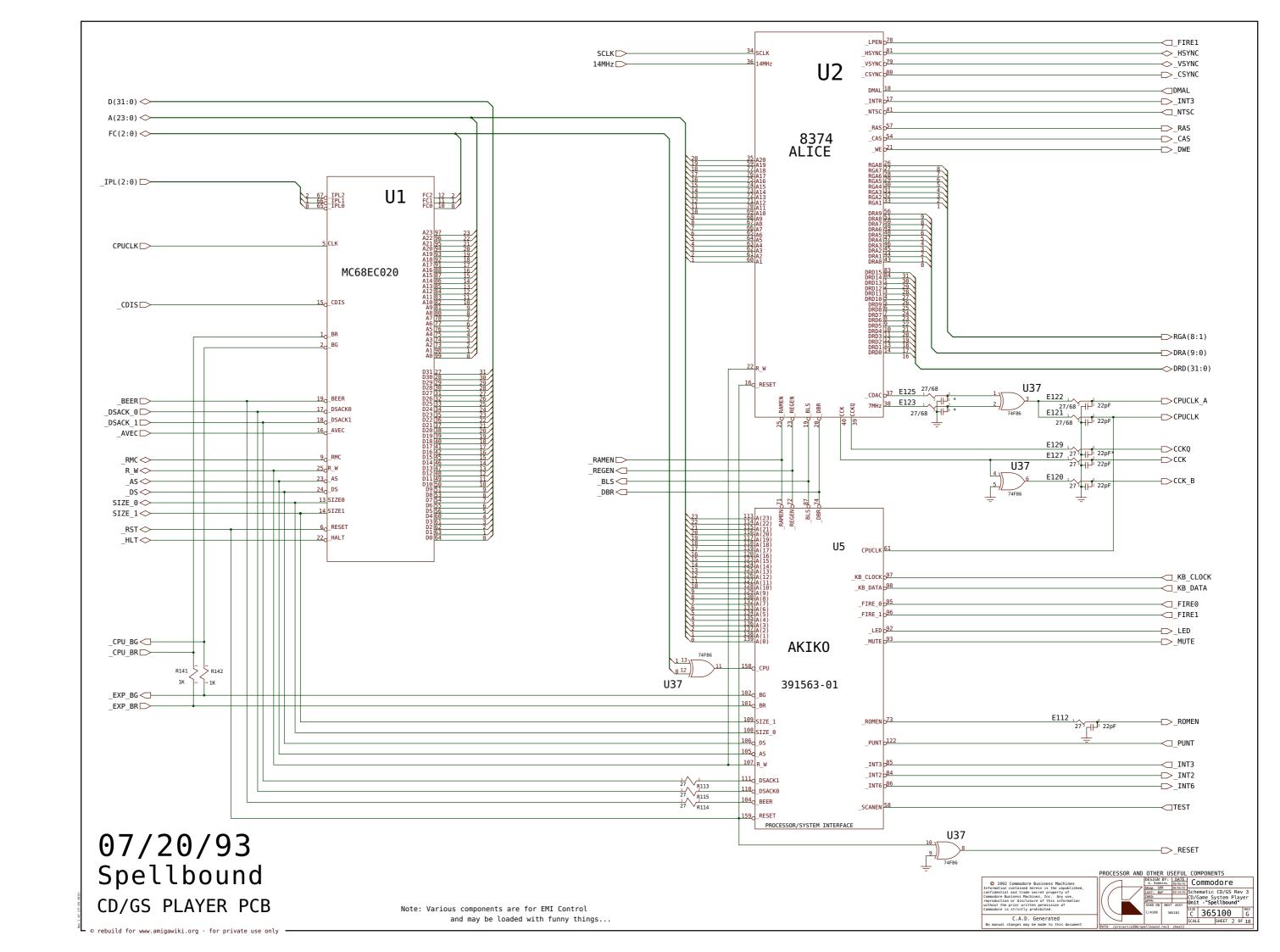
CHIP	DESCRIPTION	PAGE
68EC020	68EC020 Proc. 16MHz	2
8374	Alice	2
8364	Paula	5
4203	Lisa	4
391563	AKIKO	2,3,6
27C8000	CD32 ROM 256Kx16,120nS	3
24C08	Serial NVRAM	6
CXA1145	Composite Encoder	4
RH5VA43	Voltage Sense IC	5,7
514800	DRAM 512Kx8, 80nS	3
BT101	Triple 8-bit Video DAC	4
LC78835	16-bit Audio DAC	7
CXA1553	Headphone Amplifier	7
LM385		4
TTL-0SC	28.63636 MHz (NTSC)	4
TTL-0SC	28.37516 MHz (PAL)	4
VA3424	RF Modulator (NTSC)	4
UD3626	RF Modulator (PAL)	4
		6
1		
XTAL	4.433619 MHz (PAL)	4
	M/N-PAL	4
	,	
BPF	Chroma Bandpass Filter	4
Delav		4
	1	
1	· · · · · · · · · · · · · · · · · · ·	
	68EC020 8374 8364 4203 391563 27C8000 24C08 CXA1145 514800 BT101 LC78835 CXA1553 LM385 TTL-0SC TTL-0SC VA3424 UD3626 TTL-0SC	68EC020 Proc. 16MHz 8374 Alice 8364 Paula 4203 Lisa 391563 AKIKO 27C8000 CD32 ROM 256Kx16,120nS 24C08 Serial NVRAM CXA1145 Composite Encoder RH5VA43 Voltage Sense IC 514800 DRAM 512Kx8, 80nS BT101 Triple 8-bit Video DAC LC78835 16-bit Audio DAC CXA1553 Headphone Amplifier LM385 DAC Reference Diode TTL-0SC 28.6366 MHz (NTSC) TTL-0SC 28.6366 MHz (PAL) VA3424 RF Modulator (NTSC) UD3626 RF Modulator (PAL) TTL-0SC 16.9344 MHz XTAL 4.433619 MHz (PAL) XTAL 4.433619 MHz (PAL) XTAL M/N-PAL

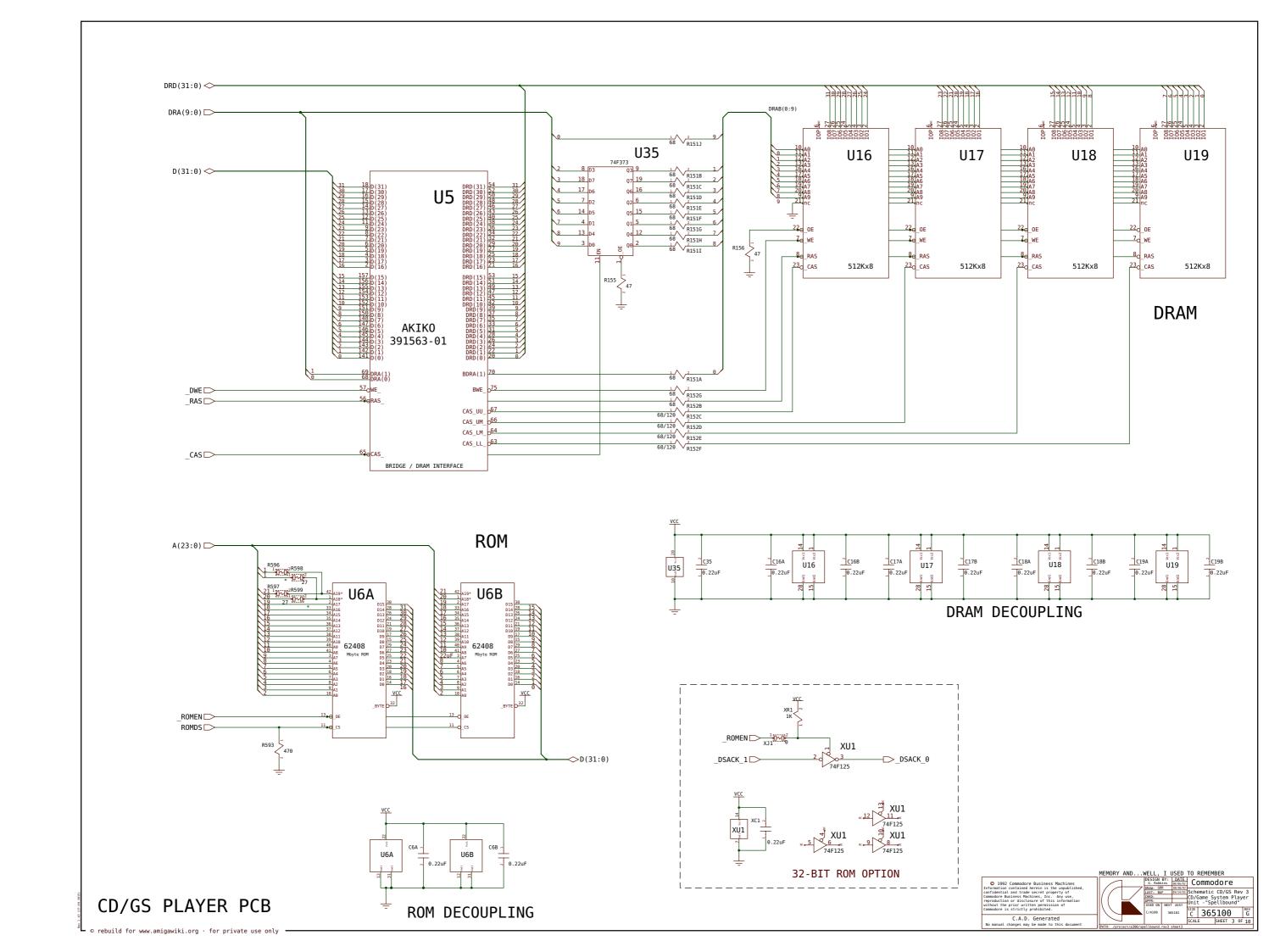
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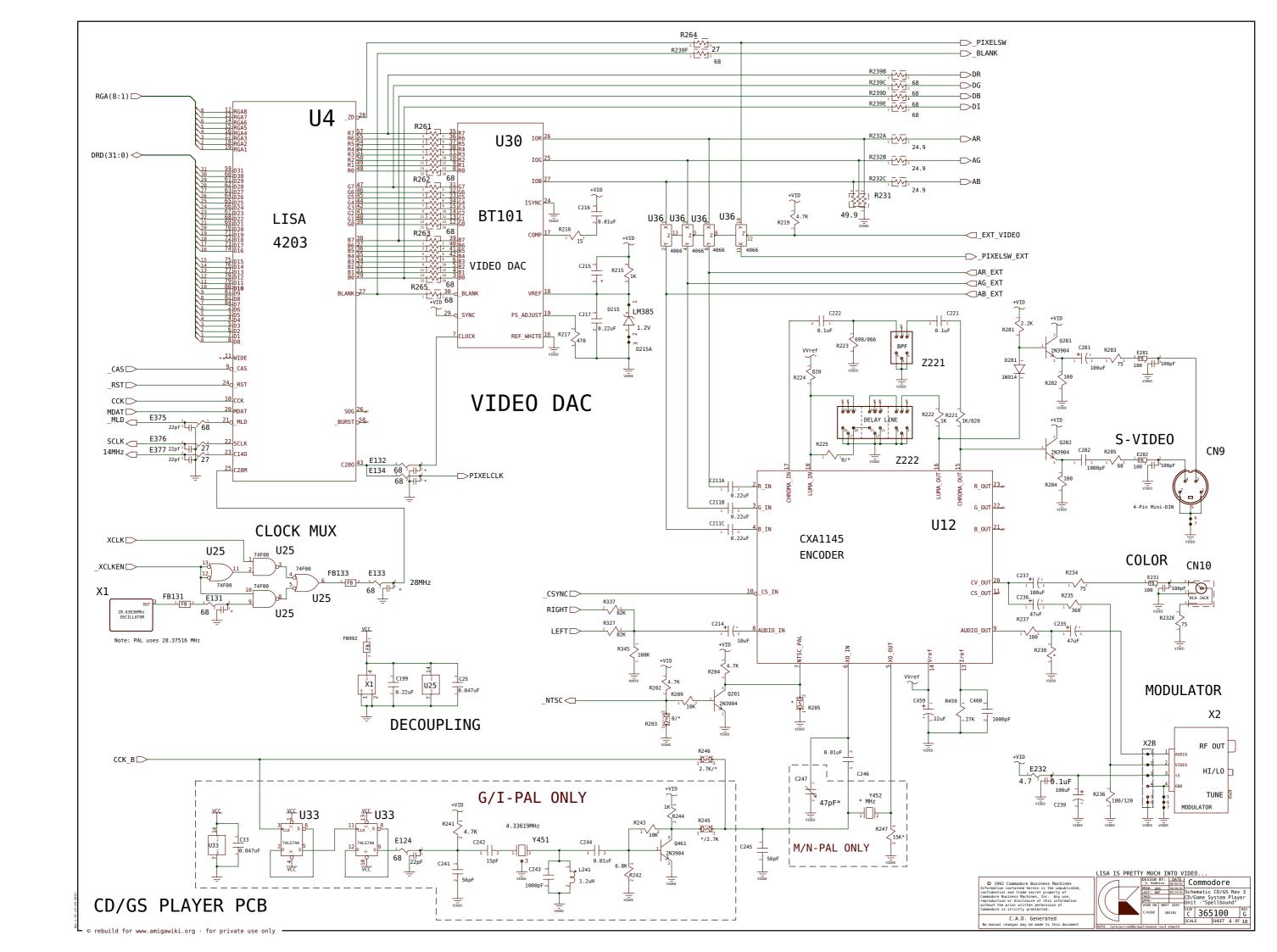
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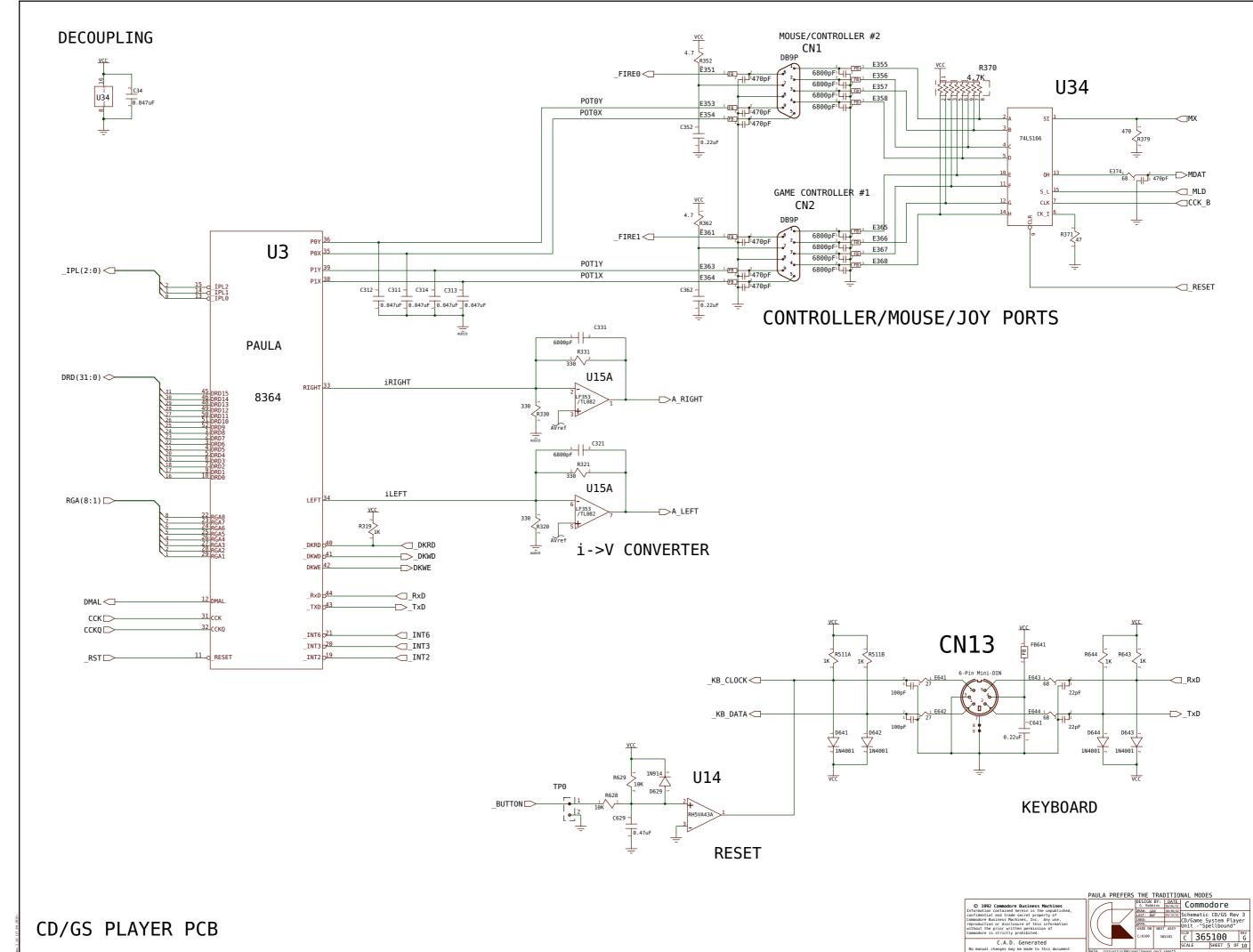
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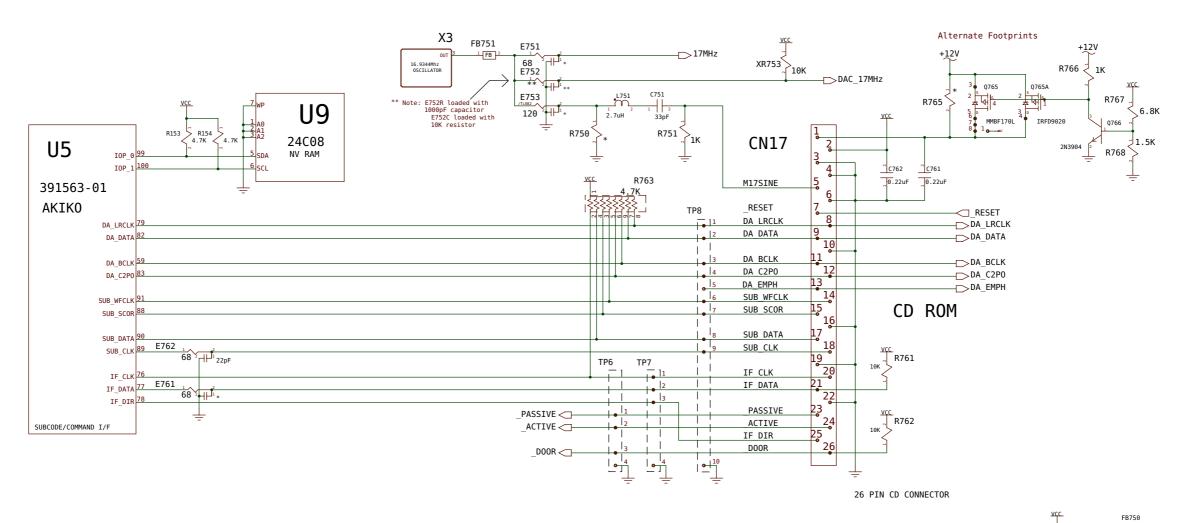
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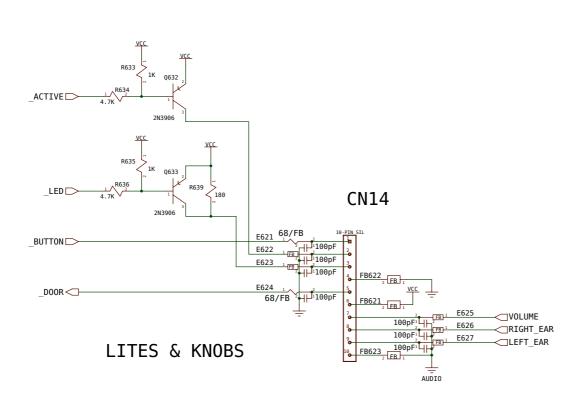


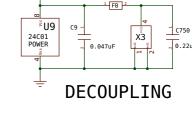


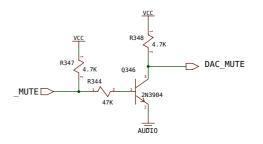










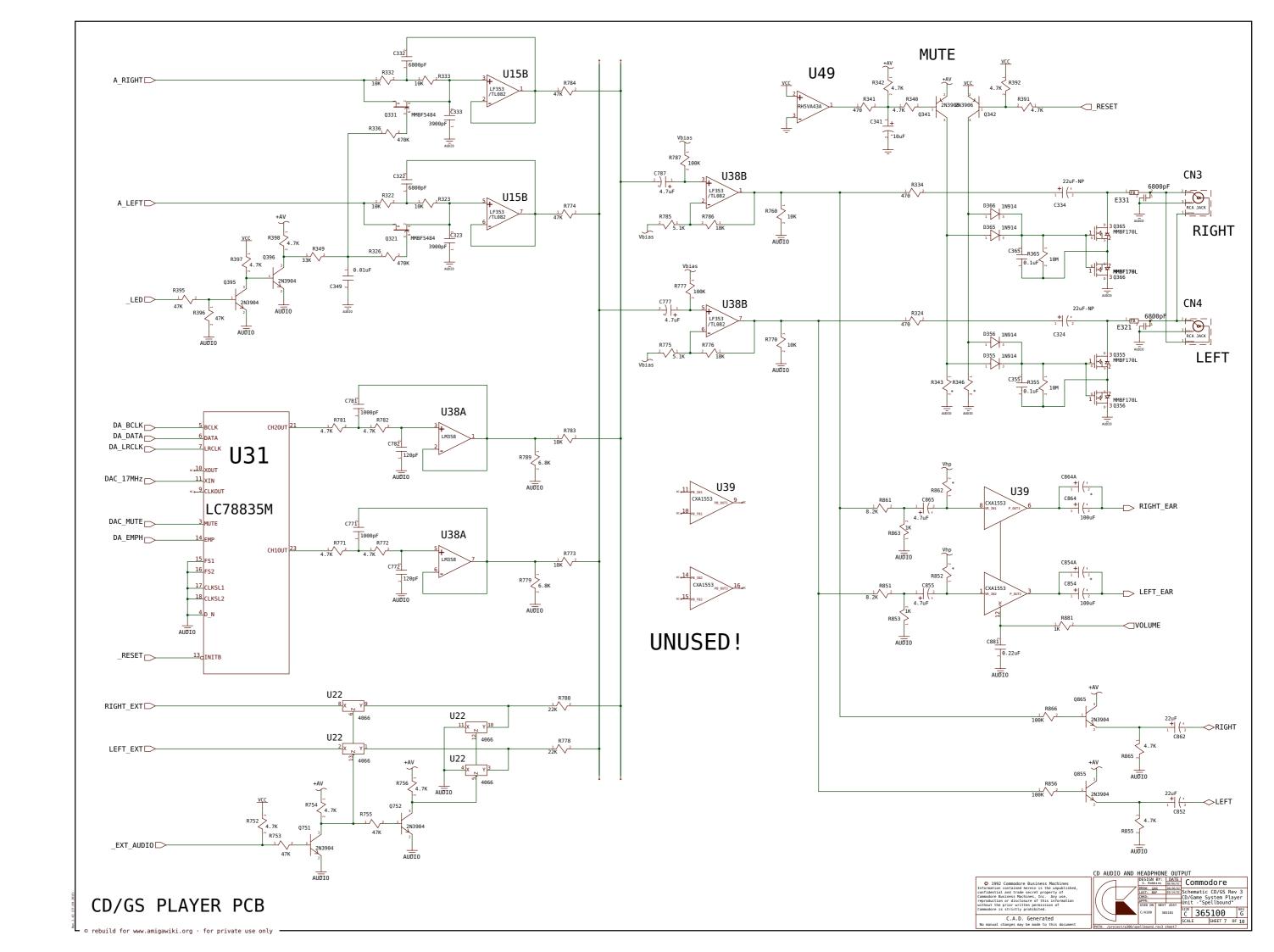


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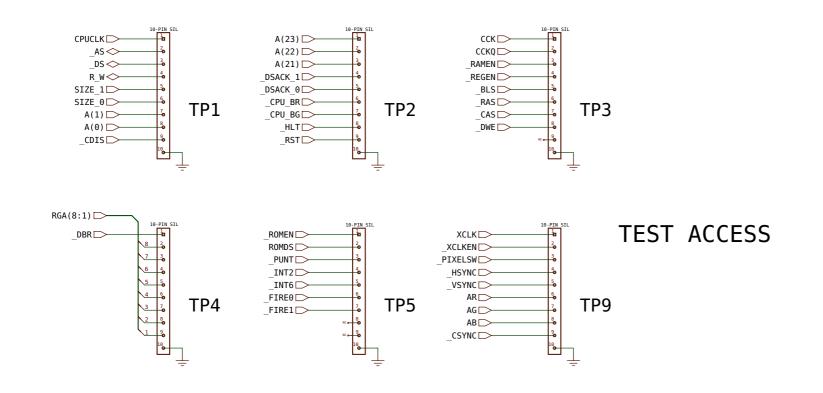
CD ROM, THE WAVE OF THE FUTURE - NOT!

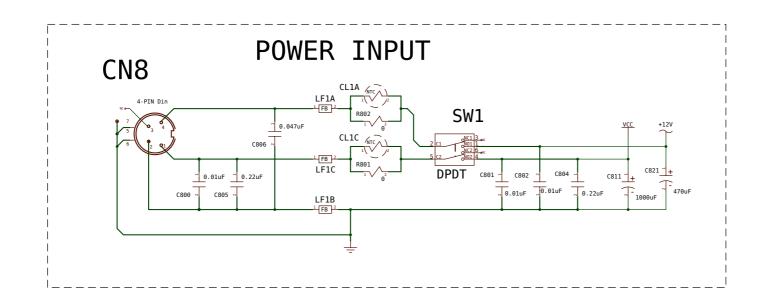
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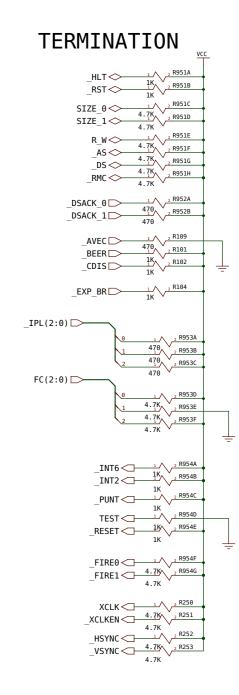
CD/GS PLAYER PCB



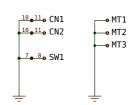
EXPANSION CONNECTOR A(31:0) <> D(31:0) <> P1 **WARNING:** Pin numbers are backwards _IPL(2:0) 🗁 FC(2:0) _ IPEND _RST 🗁 _ECS **• SIZE_1 SIZE_0 ___DS _AS 🗁 ___BEER $R_W \triangleright$ ___AVEC _STERM ** _DSACK_1 🗁 ____DSACK_0 CPUCLK_A □ **0**101 __RMC _CIIN * **•**107 ⊸ _CIOUT _CBREQ **• --≪ _CBACK _CPU_BR 🗁 ____EXP_BG _CPU_BG < ____EXP_BR CPU BGACK **™**• ⊸ _EXP_BGACK **•**115 RESET PUNT 🗀 **0**117 __INT6 INT2 ____KB_DATA _KB_CL0CK 🗁 FIRE0 ____FIRE1 _LED < ____ACTIVE **•**125 TxD RxD 🗀 ____DKWD _DKRD 🗁 **0**129 SYSTEM -DKWE **9**131 _CONFIG_OUT ____CONFIG_IN **•**133 **0**135 ____EXT_AUDIO DA_DATA **•**141 DA_BCLK DA_LRCLK **•**143 0144 **0**145 0146 DR < –**D**G DB < __ —DI PIXELSW PIXELCLK _PIXELSW_EXT< **•**151 _BLANK _> **0**153 **0**155 -⇔CCK B _CSYNC <--**9**157 **0**150 —<>_VSYNC _HSYNC 🗁 €159 AR_EXT > –<mark>□></mark>AR AG_EXT □ –**□**>AG **•**165 AB_EXT –**⊳**AB **0**168 €167 ___XCLKEN _NTSC < **0**171 0172 ____EXT_VIDEO XCLK ___ **•**173 0178 **•**177 LEFT EXT LEFT **•**179 RIGHT_EXT RIGHT •181 •182 | 22 | Committed | Early | 20 | Committed | Early | 20 | Committed | Early | Committed | Early | Committed | Early | Early | Committed | Early CD/GS PLAYER PCB C.A.D. Generated manual changes may be made to this © rebuild for www.amigawiki.org ⋅ for private use only



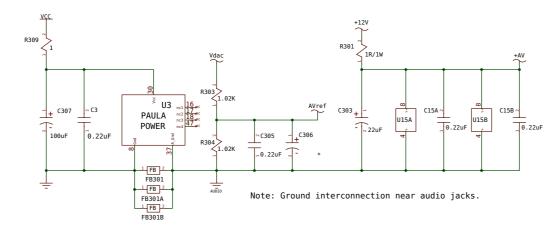




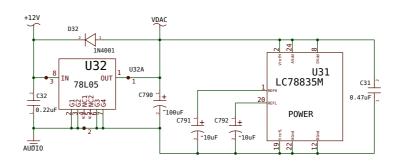
HOLES &c.



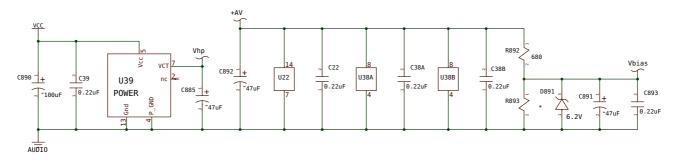
PAULA/AUDIO DECOUPLING



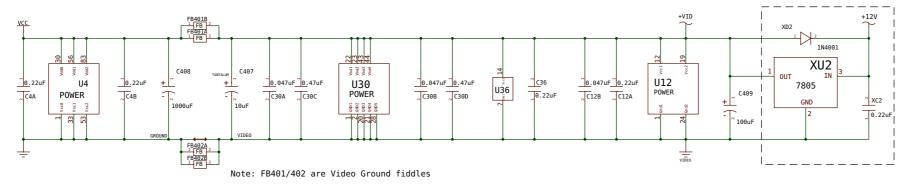
CD/AUDIO DAC DECOUPLING



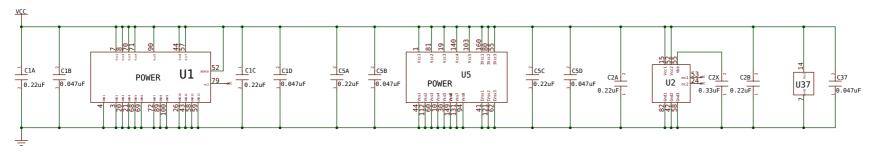
HEADPHONE/AUDIO DECOUPLING



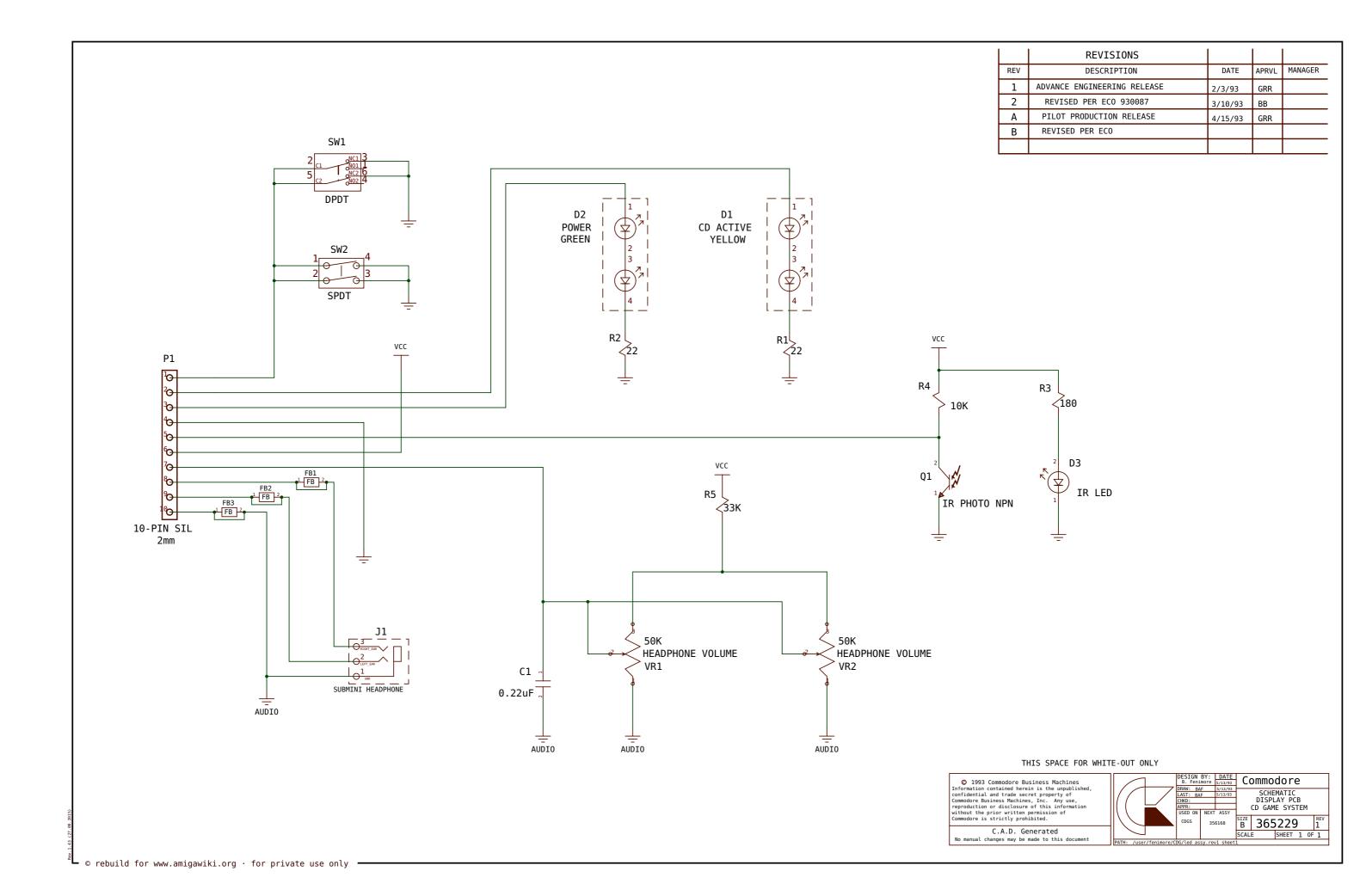
VIDEO DECOUPLING

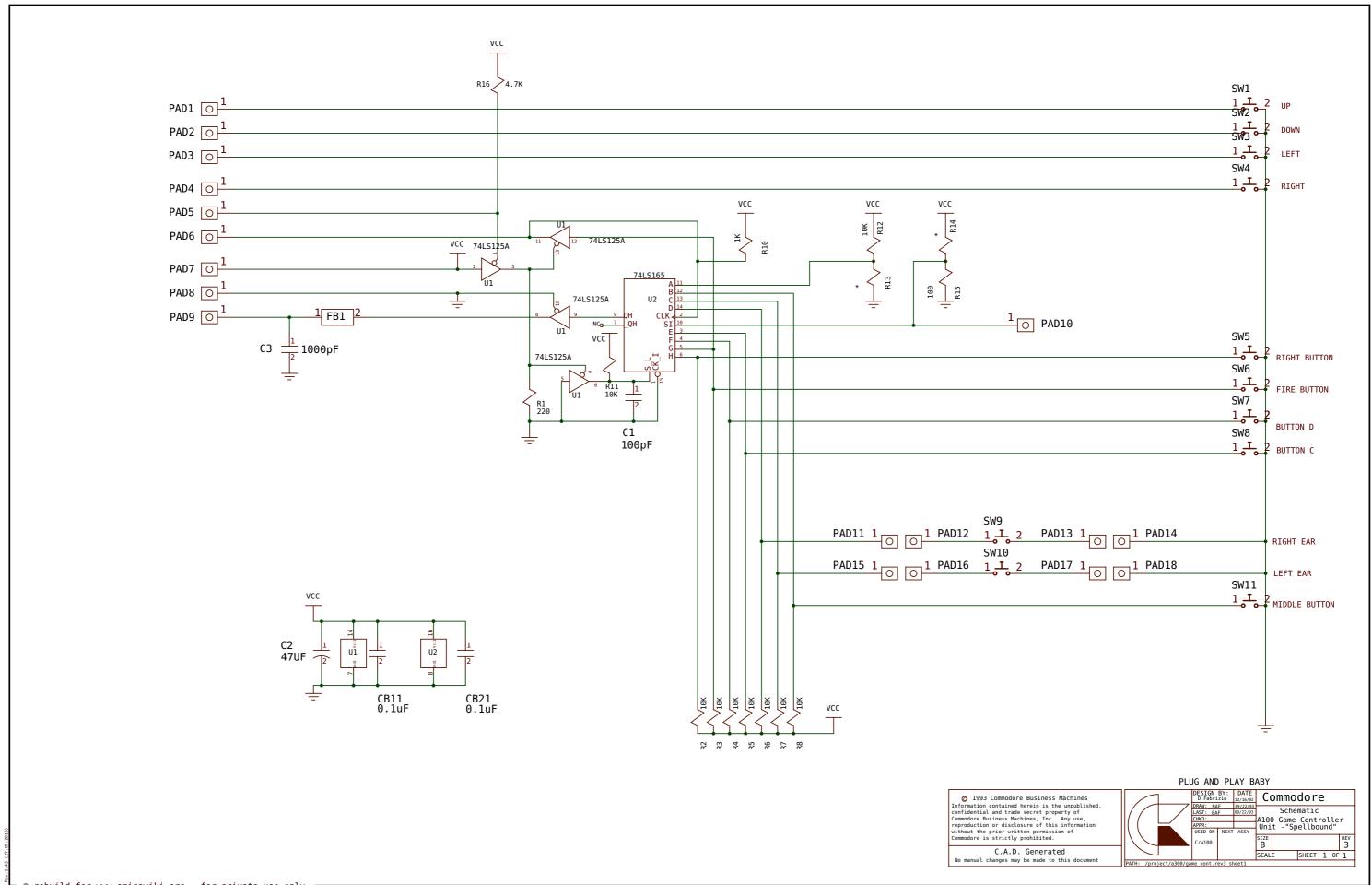


PROCESSOR/AKIKO/ALICE DECOUPLING



CD/GS PLAYER PCB





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