Amiga

A600_R1.5

Rev.1.37 (02.09.2012)

Revision History

REV	DESCRIPTION	DATE	APRVL	MANAGER
0	Engineering Prototype	08/01/91	GRR	
1	Pilot Production	10/22/91	GRR	

Jumpers and Stuff

REF	TYPE	DESCRIPTION	PAGE
R246	SMT	NTSC Color Burst	4
R202	SMT	PAL Color Burst	4
R625	SMT	Keyboard MPU Clock	9
R624	SMT	Keyboard/System Reset	9

Connectors

REF	TYPE	DESCRIPTION	PAGE
CN1	DB9P	Mouse/Joystick 1	5
CN2	DB9P	Mouse/Joystick 2	5
CN3	RCA-J	Right Audio Output	5
CN4	RCA-J	Left Audio Output	5
CN5	DB23S	External Floppy	8
CN6	DB25P	RS232 Serial Port	7
CN7	DB25S	Parallel Printer Port	7
CN8	SQ DIN	Power Supply Connector	13
CN9	DB23P	Video Output	6
CN10	RCA-J	Composite Video	4
CN11	DIL-34	Internal Floppy Signal	8
CN12	SIL-4	Internal Floppy Power	8
CN13	MEM-30	Keyboard Membrane	9
CN14	SIL-4	Internal Floppy Power	8
CN13	MEM-30	Keyboard Membrane	9
CN14	SIL-4	Keyboard Status LED's	9
CN15	PCMCIA	PC"Memory Card"	11
P9	EDGE-80	Memory Bus Expansion	12

Signal Glossary

SIGNAL	DESCRIPTION (AREA)	PAGES
28MHZ	28.63636 MHz Master Clock	
7MHZ	7.15909 MHz Processor Clock	
A[23:1]	Processor Address Bus (68000)	
ACK	Data Acknowledge (Parallel Port)	
AS	Address Strobe (68000)	
AUDIN	Audio Input (RS232 Port)	
AUDOUT	Audio Output (RS232 Jack)	
BEER	Bus Error (68000)	
BG	Bus Grant (68000)	
BGACK	Bus Grant Acknowledge (68000)	
BLISS	Blitter Slowdown (Chips)	
BLIT	Chip Memory Access (Chips)	
BR	Bus Request (68000)	
BUSY	Device Busy (Parallel Port)	
CASL/U	Column Address Strobe (DRAM)	
CCK/CCKQ	Color Clock / Quadrature (Chips)	
CDAC	7.15909 MHz Quadrature Clock (Chips)	
CHNG	Media Change (Floppy)	
CLKRD/WR	Read-Time Clock Read / Write (RTC)	
COMP	Monochrome Composite Video (Video)	
CSYNC	Composite Sync (Video)	
CTS	Clear to Send (RS232 Port)	
D[15:0]	Processor Data Bus (68000)	
DIR	Step Direction (Floppy)	
DKRD	Disk Read Data (Floppy)	
DKWD	Disk Write Data (Floppy)	
DKWE	Disk Write Enable (Floppy)	
DMAL	Chip DMA Request Line (Chips)	
DRA[8:0]	DRAM Address Bus (DRAM)	
DRD[15:0]	DRAM Data Bus (DRAM)	
DSR	Data Set Ready (RS232 Port)	
DTACK	Data Transfer Acknowledge (68000)	
DTR	Data Terminal Ready (RS232 Port)	
E	Peripheral Enable Clock (68000)	
EXTICK	Expansion Present / RTC Tick	
FC[2:0]	Function Code (68000)	
FIRE0/1	Fire Button 0/1 (Joysticks)	
HLT	Processor Halt (68000)	
HSYNC	Horizontal Sync (Video)	
INDEX	Index Pulse (Floppy)	
INT[2,3,6]	Interrupt Request (Chips)	
IORESET	I/O Reset	
IPL[2:0]	Interrupt Priority Level (68000)	
KBCLOCK	Keyboard Clock (Keyboard)	
KBDATA	Keyboard Data (Keyboard)	
KBRESET	Keyboard Reset (Keyboard)	
LDS/UDS	Upper / Lower Data Strobes (68000)	
LED	Power On LED / Audio Filter Disable	
LEFT/RIGHT	Left Right Audio (Audio)	

SIGNAL	DESCRIPTION (AREA)	PAGES
LPEN	Light Pen Trigger (Joysticks)	
MTR	Motor On (Floppy)	
MTR0	Motor On - Drive 0 (Floppy)	
M0V/M0H	Mouse 0 Quadrature V/H (Joysticks)	
M1V/M1H	Mouse 1 Quadrature V/H (Joysticks)	
OVL	Overlay ROM over RAM	
OVR	Override System Decoding	
PIXELSW	Genlock Pixel Switch (Video)	
POT0X/0Y	Pot Lines 0 X/Y (Joysticks)	
POT1X/1Y	Pot Lines 1 X/Y (Joysticks)	
POUT	Paper Out (Parallel Port)	
PPD[7:0]	Parallel Port Data (Parallel Port)	
RAMEN	RAM Enable (Chips)	
REGEN	Chip Register Enable (Chips)	
RAS0/1	Row Address Strobe (DRAM)	
RDY	Drive Ready (Floppy)	
RESET	General Reset	
RGA[8:1]	Register Address Bus (Chips)	
R/G/B	Red / Green / Blue (Video)	
RI	Ring Indicate (RS232 Port)	
ROMEN	ROM Enable (ROM)	
RTS	Request to Send (RS232 Port)	
RST	Processor Reset (68000)	
RXD	Receive Data (RS232 Port)	
RW	Processor Read/Write (68000)	
SEL	Select (Parallel Port)	
SEL[3:0]	Drive Select (Floppy)	
SIDE	Side Select (Floppy)	
STEP	Step In/Out Command (Floppy)	
TRK0	Track Zero Sense (Floppy)	
TXD	Transmit Data (RS232 Port)	
VMA	Valid Memory Address (68000)	
VPA	Valid Peripheral Address (68000)	
VSYNC	Vertical Sync (Video)	
WE	Write Enable (DRAM)	
WPROT	Write Protect Sense (Floppy)	
XCLK	External Genlock Clock (Video)	
XCLKEN	External Clock Enable (Video)	
XRDY	External Data Ready	
	** Credit Card and IDE Stuff? **	

Key Components

REF	CHIP	DESCRIPTION	PAGE
U1	68000	68000 Processor, 8MHz	2
U2	8375	ECS Agnus A300/A500+	2
U3	8364	Paula	5
U4	8373	ECS Denise	4
U5	4145-20	Gayle Gate Array	2,8,11
U6	asst	ROM 256Kx16, 200 nS	10
U7-8	8520	Amiga VIA, 1 MHz	7
U10-11	28F10	Flash Memory 128Kx8	10
U12	CXA1145	Sony Video Encoder	4
U13	6570-36	Amiga Keyboard MPU	9
U14	NE555	Reset Timer	9
U16-17	asst	DRAM 256Kx16, 80 nS	3
U15	LF347	BiMOS Op-Amp	5
	TL084	BiMOS Op-Amp	alt
U28	1488	EIA Line Driver	7
U29	1489	EIA Line Receiver	7
X1	OSC	TTL 28.63636 MHz NTSC	2
	OSC	TTL 28.37512 MHz PAL	alt
Y451	XTAL	4.433619MHz PAL Burst	4
Y621	XTAL	3MHz Ceramic Resonator	9
X2	asst	PAL Video Modulator	4
X2B	asst	NTSC Video Modulator	4

DIRECTORIES AND REVISION HISTORY

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DESIGN BY: G. Robbins — DATE: 05/23/91
DRAW: GRR — 05/23/91
LAST: GRR — 10/22/91
CHKD:
APPR:
USED ON: C/A300 — NEXT ASSY: 315986

Commodore
Schematic A300 Rev 1
C/A300 Main Board
"June Bug"

SIZE C | 315987 | REV 1
SCALE | SHEET 1 OF 13

PATH: /project/a300/june_bug.rev1 sheet1

A600 Rev1.5 PCB

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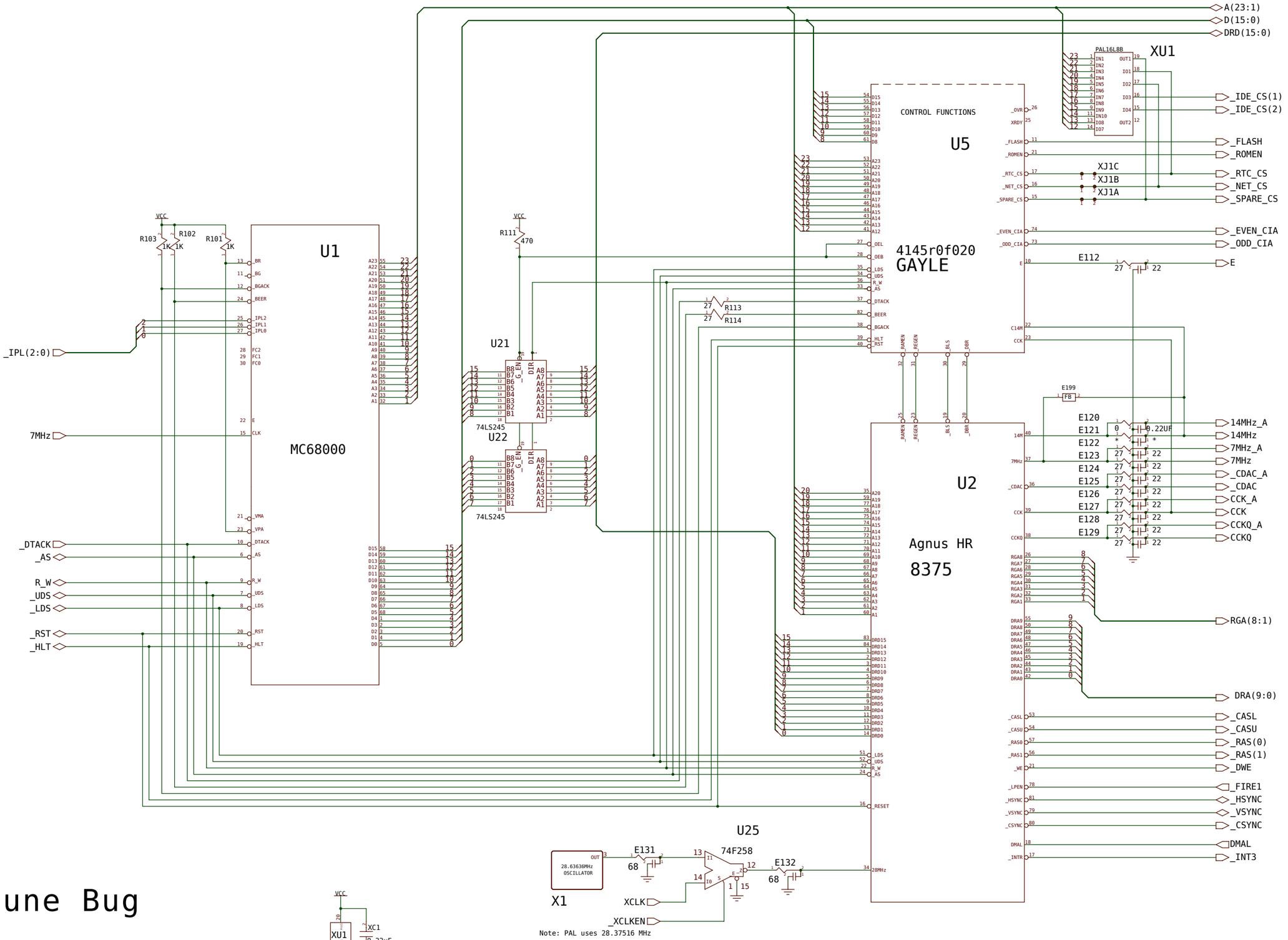
Rev.1.37 (02.09.2012)

Note: Various components are for EMI Control

and may be loaded with funny things...



June Bug

10/22/91

A600 Rev1.5 PCB

PROCESSOR AND OTHER USEFUL COMPONENTS

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DESIGN BY: G. Robbins	DATE 05/27/91	Commodore
DRAW: GRR	05/27/91	
LAST: GRR	10/22/91	Schematic A300 Rev 1 C/A300 Main Board "June Bug"
CHKD:		
APPR:		
USED ON C/A300	NEXT ASSY 315986	SIZE C 315987 REV 1
		SCALE SHEET 2 OF 13

PATH: /project/a300/june_bug_rev1 sheet2

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DRD(15:0)

DRA(9:0)

BDRA(9:0)

R151A 68
R151B 68
R151C 68
R151D 68
R151E 68
R151F 68
R151G 68
R151H 68
R152A 68

U16
DRAM
256Kx16

U17 is OPTIONAL...
U17
OPT
256Kx16

WHITE SPACE

_X1M
R162 *
_ROE
R161 470

_DWE
R152B 27
_BWE

_RAS(0)
_RAS(1)
R152C 27
R152D 27
_BRAS(0)
_BRAS(1)

_CASL
_CASU
74F139
U27
R152E 27
R152F 27
_BCASL(0)
_BCASL(1)
E152 47pF
E151 47pF

U26
74F00
U25
74F258
E150 27 47pf
R152G 27
R152H 27
_BCASU(0)
_BCASU(1)
E154 47pF
E153 47pF
KLUDGE

_XCLKEN
CCK_A

VCC
C16A 0.33uF
C16B 0.33uF
C17A 0.33uF OPT
C17B 0.33uF OPT
DECOUPLING

MEMORY AND...WELL, I USED TO REMEMBER

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DESIGN BY: G. Robbins 05/27/91
DRAW: GRR 05/27/91
LAST: GRR 10/22/91
CHKD:
APPR:
USED ON: C/A300
NEXT ASSY: 315986

Commodore
Schematic A300 Rev 1
C/A300 Main Board
"June Bug"

SIZE C 315987 REV 1
SCALE
SHEET 3 OF 13

PATH: /project/a300/june_bug.rev1 sheet3

A600 Rev1.5 PCB

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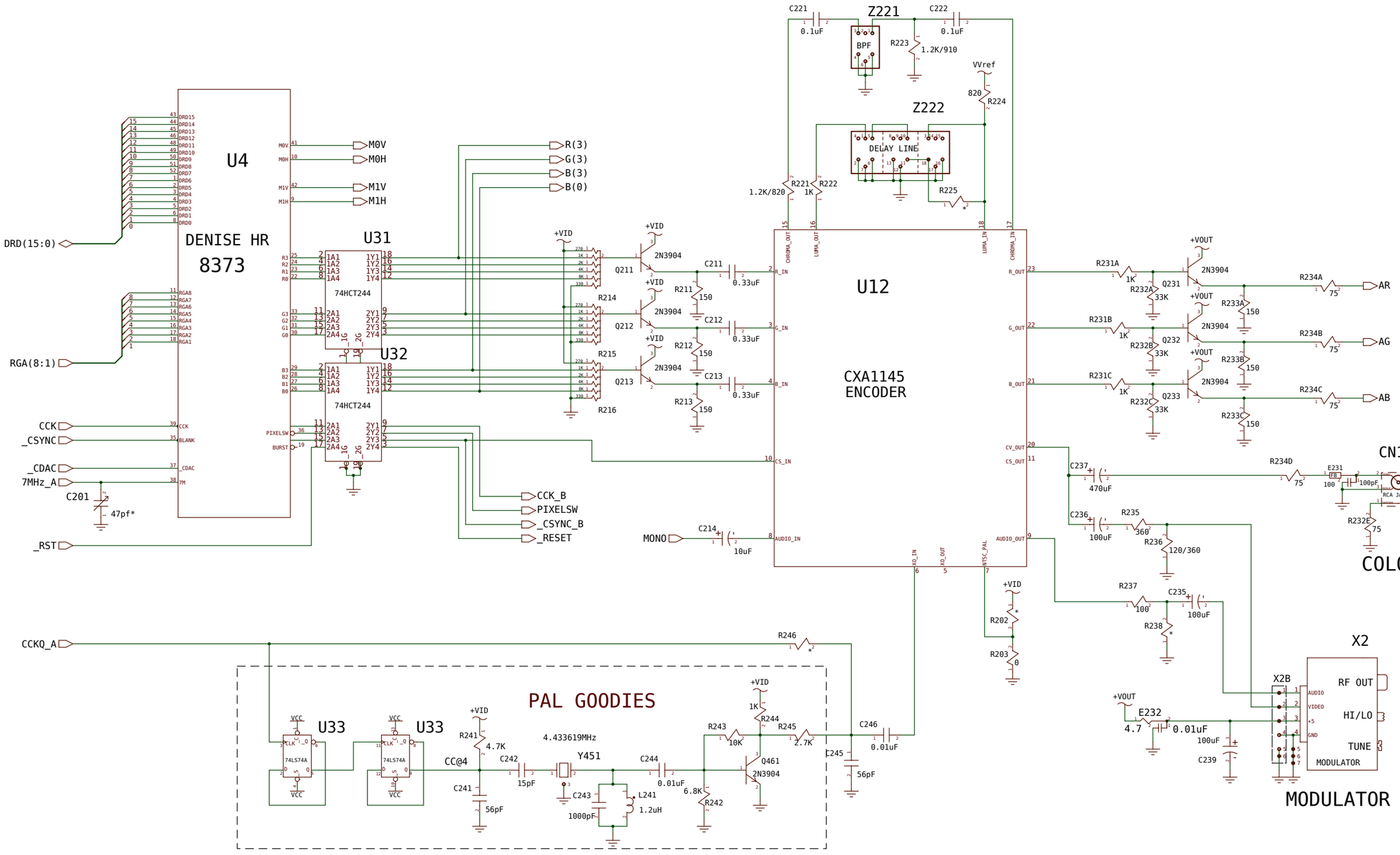

A600 Rev1.5 PCB

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Note: Components designated as Exxx may be loaded with EMI fliters, ferrite beads or resistors!

DENISE IS PRETTY MUCH INTO VIDEO...

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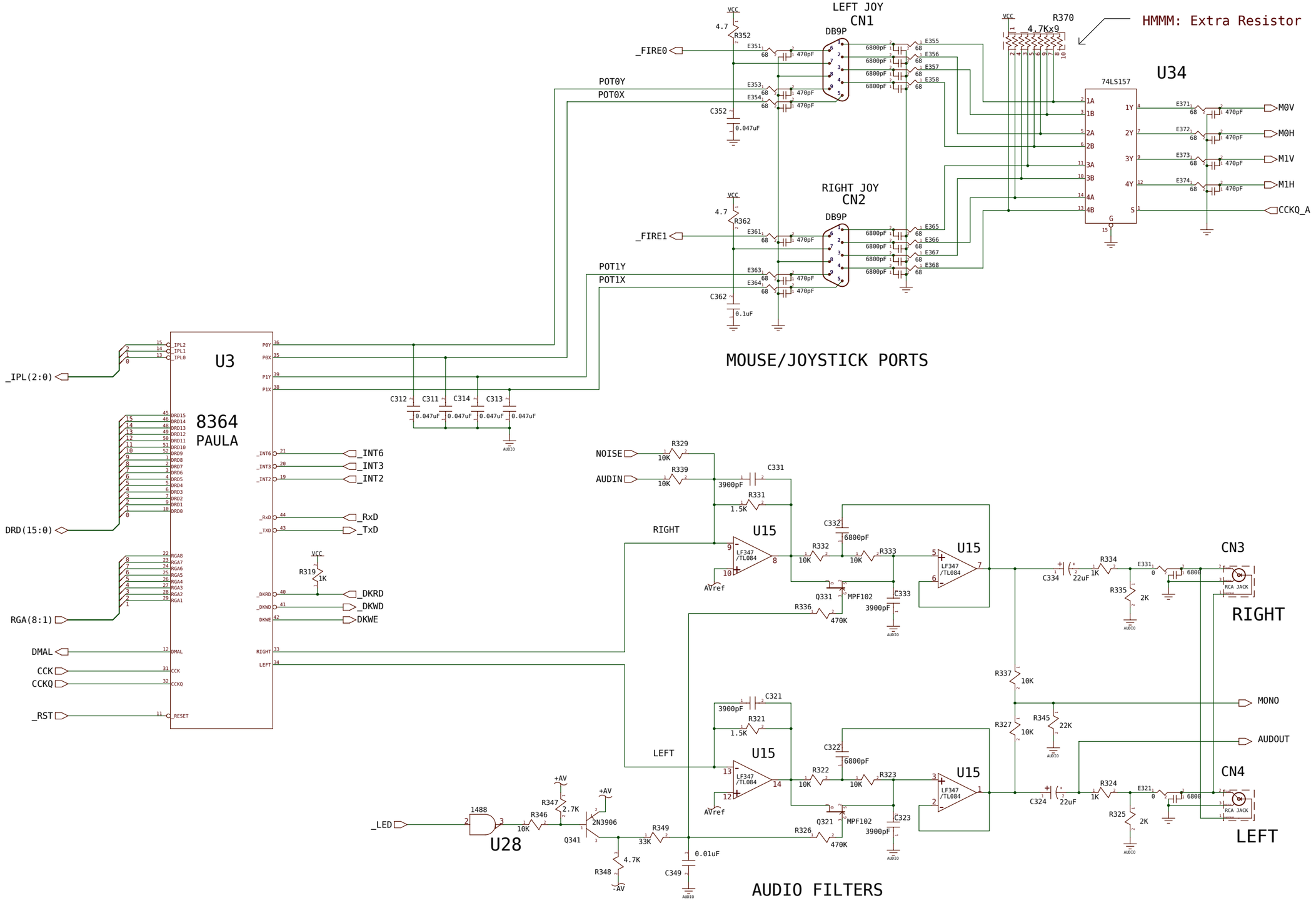
DESIGN BY: K. Robbins	DATE 04/29/91	Commodore
DRAW: GRR	05/27/91	Schematic A300 Rev 1 C/A300 Main Board "June Bug"
LAST: GRR	12/05/91	
CHKD:		
APPR:		
USED ON: C/A300	NEXT ASSY: 315986	SIZE C / 315987 / REV 1
		SCALE / SHEET 4 OF 13

PATH: /project/a300/june_bug_rev1 sheet4

Rev.1.37 (02-09-2012)



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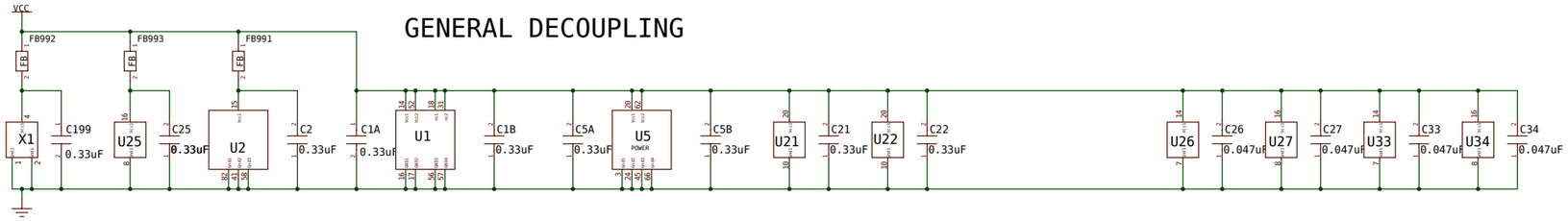
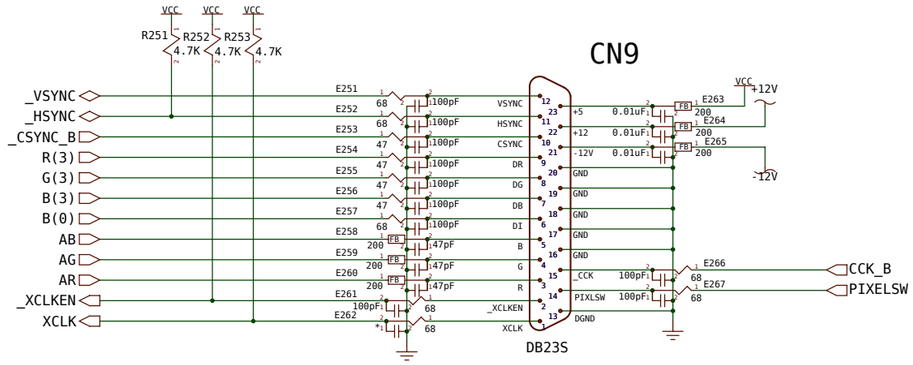
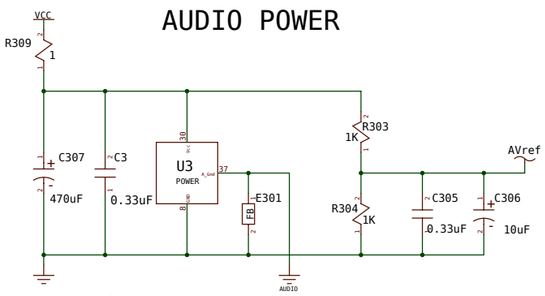
GENERAL DECOUPLING



VIDEO OUT

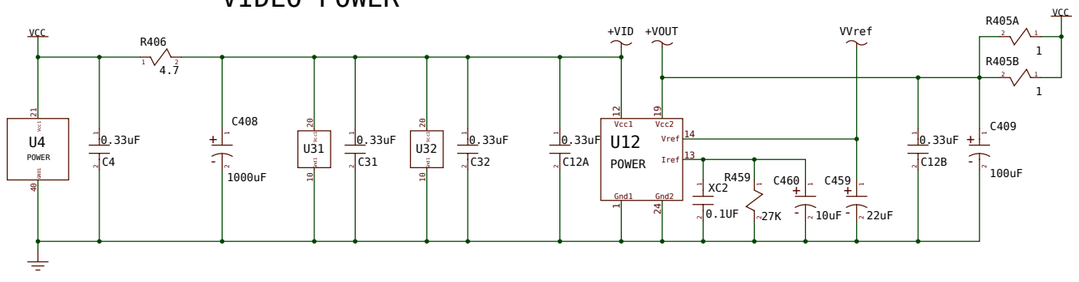


AUDIO POWER

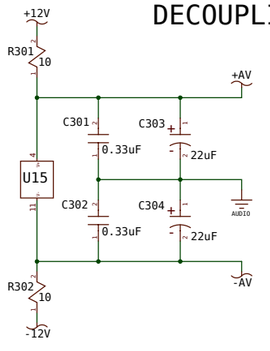


Note: Ground interconnection near audio jacks.

VIDEO POWER



DECOUPLING



A600 Rev1.5 PCB

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PARTY OUT OF BOUNDS, WHAT A MESS...

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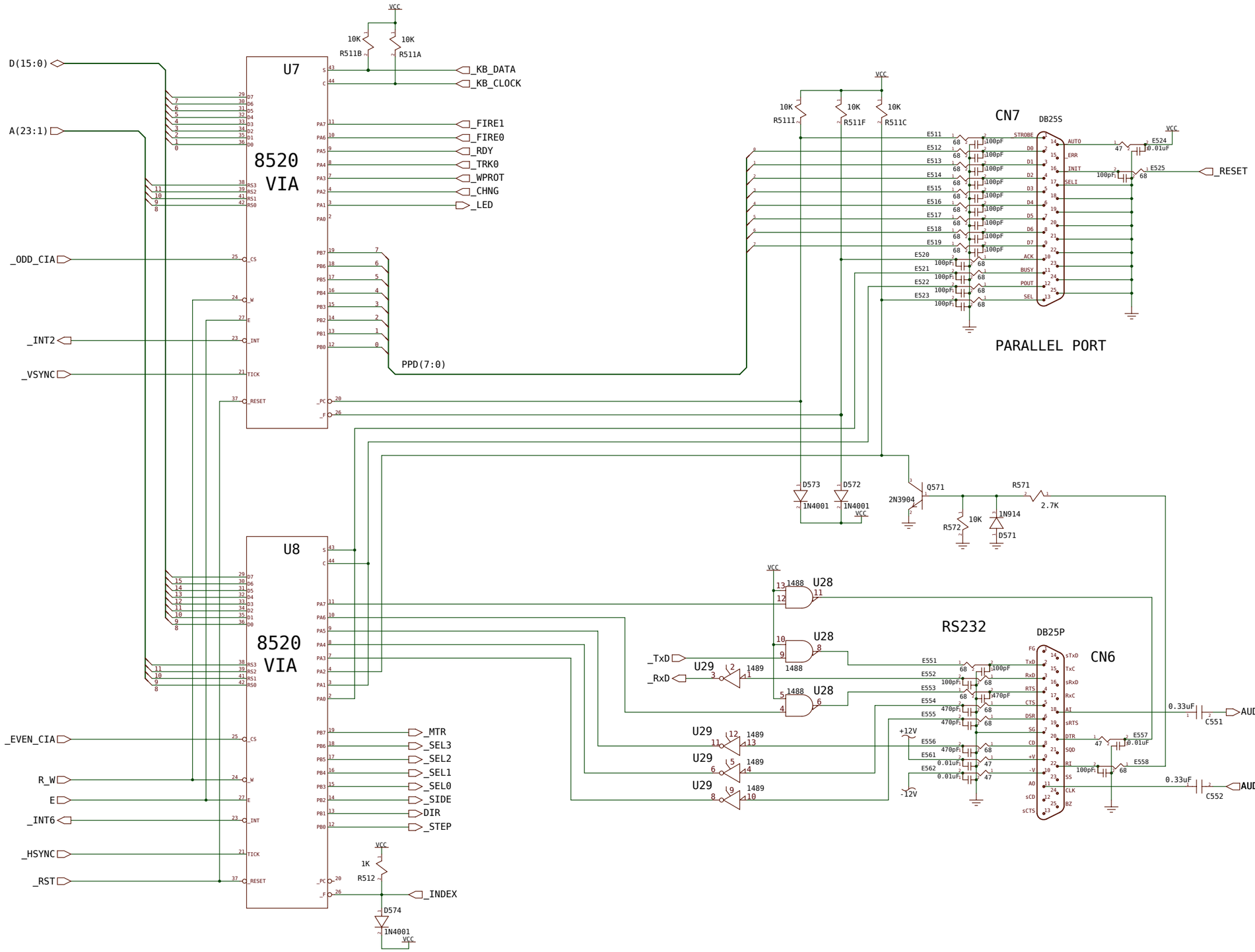
DESIGN BY: G. Robbins	DATE 04/29/93	Commodore
DRAW: GRR	05/27/97	Schematic A300 Rev 1
LAST: GRR	11/05/97	C/A300 Main Board
CHKD:		"June Bug"
APPR:		
USED ON C/A300	NEXT ASSY 315986	SIZE C 315987 REV 1
		SCALE SHEET 6 OF 13

PATH: /project/a300/june_bug.rev1 sheet6



A600 Rev1.5 PCB

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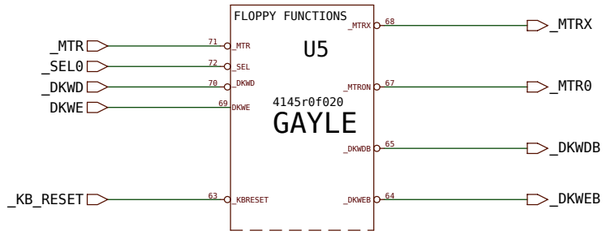
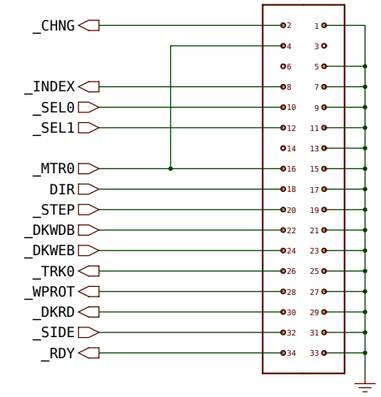
Commodore
C/A300 Main Board "June Bug"
Schematic A300 Rev 1
SIZE C 315987 REV 1
SHEET 7 OF 13
PATH: /project/a300/june_bug.rev1 sheet7

FLOPPY LOGIC

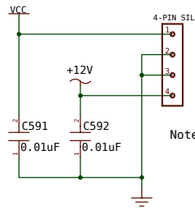


INTERNAL FLOPPY



CN11

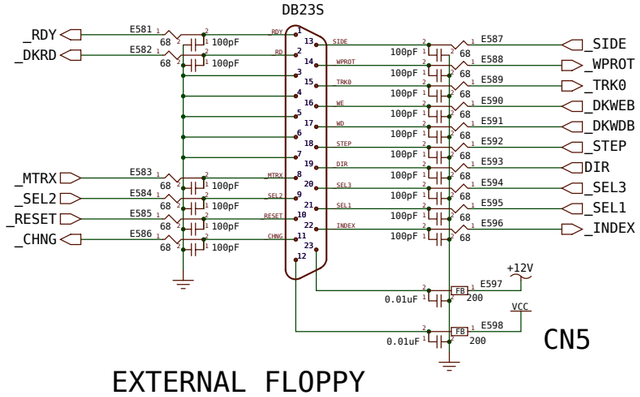
FLOPPY POWER



CN12

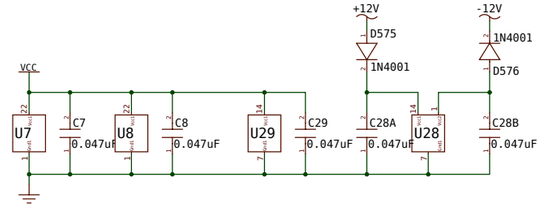
Note: Some drives are +5 only...

EXTERNAL FLOPPY



CN5

THE REST OF THE FLOPPY STUFF



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DESIGN BY: G. Robbins	DATE 05/27/91	Commodore
DRAW: GRR	05/27/91	schematic A300 Rev 1
LAST: GRR	10/22/91	C/A300 Main Board
CHKD:		"June Bug"
APPR:		
USED ON: C/A300	NEXT ASSY: 315986	SIZE C / 315987 / REV 1
		SCALE / SHEET 8 OF 13

PATH: /project/a300/june_bug.rev0 sheet8

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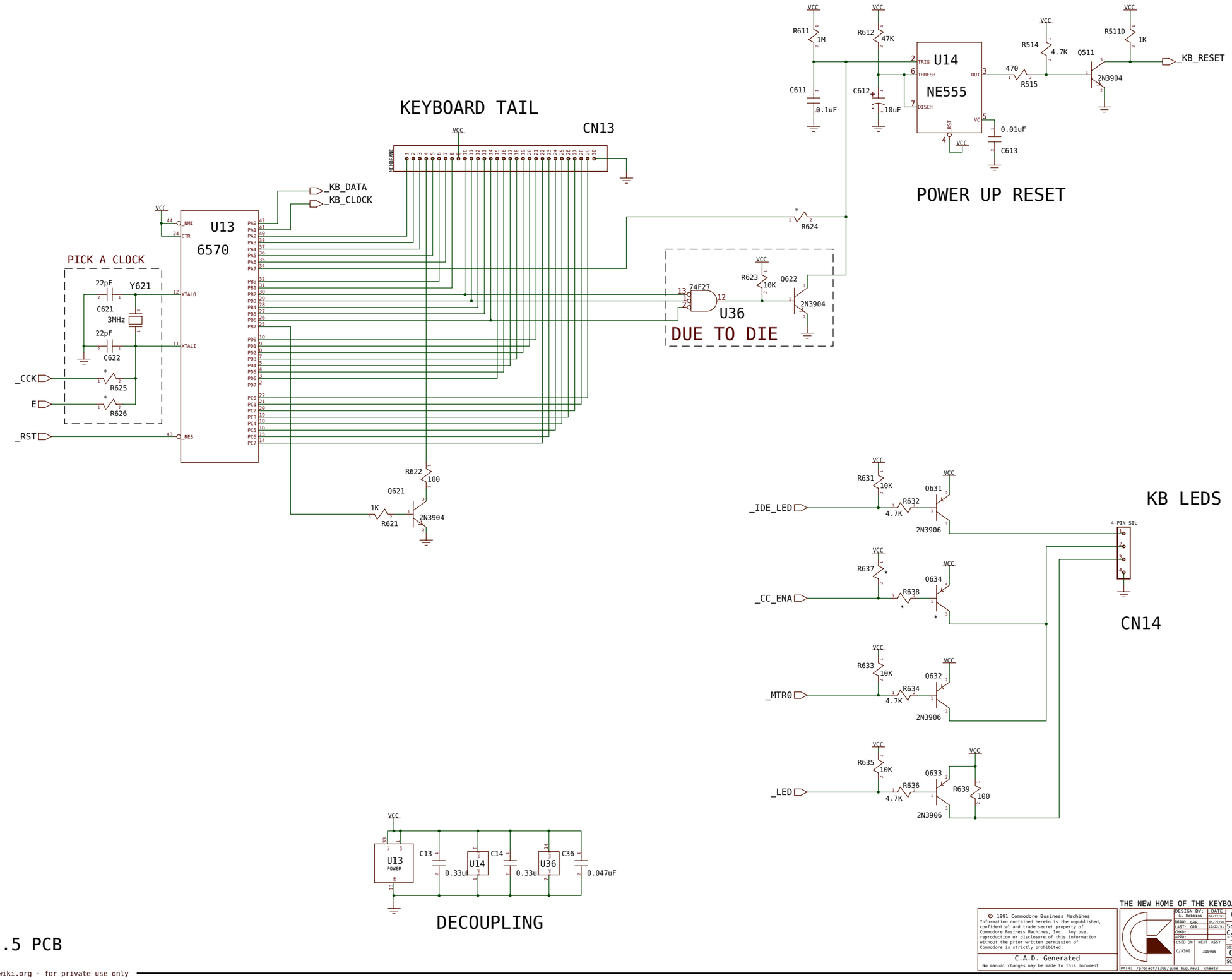

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ROM

FLASH MEMORY

A(23:1)

U6
62408
Mbyte ROM

_OE
_ROMEN
VCC
_BYTE

U10
OPT N
28F20
2 MBit FLASH

U11
OPT N
28F20
2 MBit FLASH

_WE
_OE
_CE

D(15:0)

74F139
U37
_UDS
LDS
A(18)
_FLASH

FLASH AND U37 IS OPTIONAL

PROGRAMMING VOLTAGE

+12V
R653 10K
Q652
R659 470
2N3906
VCC
R658
*
Vpp
PE12
R651 4.7K
Q651
2N3904
R652 10K
R654 1K

+12V
R657 10K
Q654
R660 470
2N3906
VCC
PE5
R655 4.7K
Q653
2N3904
R656 10K

FUNNY INVERTERS

U25
74F258
A(16)
E694 68 47pF
_A(16)

U25
74F258
CCK
_XCLKEN
E692 68 47pF
_CCK
E693 68 47pF
_CCK_A

DECOUPLING

VCC
Vpp
U6
C6 0.33uF
U37 OPT N
C37 OPT N 0.01uF
C10A OPT N 0.33uF
U10 OPT N
C10B OPT N 0.33uF
C11A OPT N 0.33uF
U11 OPT N
C11B OPT N 0.33uF

A600 Rev1.5 PCB

ROM - PLAIN AND FANCY - DODADS TOO!

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DESIGN BY: G. Robbins	DATE 05/27/91	Commodore
DRAW: GRR	05/27/91	Schematic A300 Rev 1
LAST: GRR	10/22/91	C/A300 Main Board "June Bug"
CHKD:		
APPR:		
USED ON: C/A300	NEXT ASSY 315986	SIZE C 315987 REV 1
		SCALE SHEET 10 OF 13

PATH: /project/a300/june_bug.rev1 sheet10

Rev.1.37 (02.09.2012)
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MEMORY CARD

CN15

A(23:1)
_A(16)
_REG
D(15:0)
R_W

U44 74F02

R714A 120
R714B 120

U45 74LS245
U46 74LS245
U47 74LS245
U41 74LS245
U42 74LS245

Warning:
Byte Swapped

CC_A(25:0)
CC_D(15:0)

R717 10K
R718 10K

_CC_CD(1)
_CC_CEU
_CC_CEL
_CC_OE
_CC_IORD
_CC_IOWR
_CC_WE_PGM
_CC_BUSY_IREQ
Vpp
C701 0.33uF
C702 0.33uF
_CC_RESET
_CC_WAIT
_CC_REG
_CC_BVD(2)
_CC_BVD(1)
_CC_WP
_CC_CD(2)

R716 10K
74LS245
_OE
_WE
_IORD
_IOWR
_UDS
_LDS
_REG
_CC_WAIT
_CC_OE
_CC_WE_PGM
_CC_IORD
_CC_IOWR
_CC_CEU
_CC_CEL
_CC_REG
_WAIT
U43

R719 4.7K
_CC_ENA
_FLASH
_TEST
U44 74F02

R715 10K
EEEK: EXTRA R

CARD FUNCTIONS
U5
4145r0f020
GAYLE

_CC_CD(1)
_CC_CD(2)
_CC_BVD(1)
_CC_BVD(2)
_CC_WP
_CC_BUSY_IREQ
_REG
_WAIT
_IORD
_IOWR
_OE
_WE
_CC_ENA
CC_RESET

PE5
PE12
NOISE
C711 0.33uF
_IDE_IRQ
_IDE_CS(1)
_IDE_CS(2)
XJ1D
XJ1E
_INT2
_INT6

R800 10K
R715X 4.7K

DECOUPLING

U41 C41 0.33uF
U42 C42 0.33uF
U43 C43 0.33uF
U44 C44 0.33uF
U45 C45 0.33uF
U46 C46 0.33uF
U47 C47 0.33uF

A600 Rev1.5 PCB

THE KISSY FACE CREDIT CARD MONSTER

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DESIGN BY: G. Robbins	DATE 05/27/93	Commodore
DRAW: GRR	05/27/93	Schematic A300 Rev 1 C/A300 Main Board "June Bug"
CHKD:		
APPR:		
USED ON C/A300	NEXT ASSY 315986	SIZE C 315987 REV 1
		SCALE SHEET 11 OF 13

PATH: /project/a300/june_bug.rev1 sheet11

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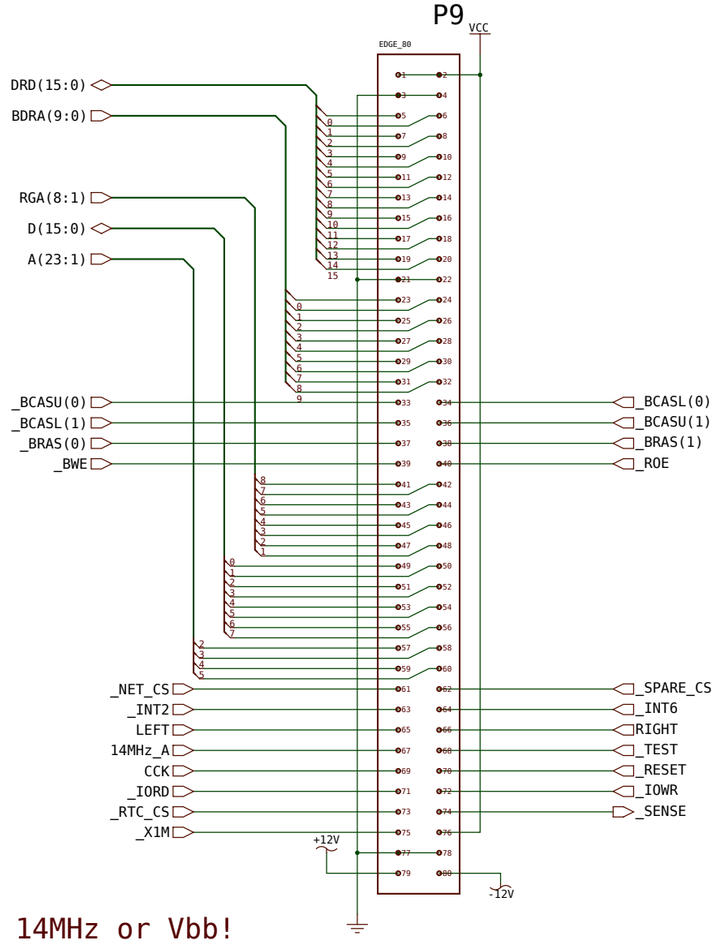
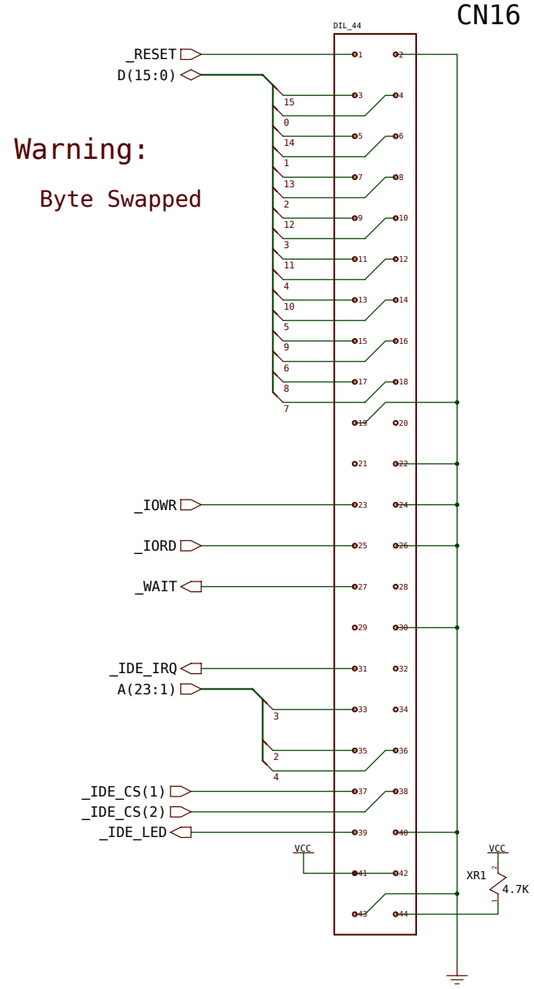
MEMORY EXPANSION



Note: 14MHz or Vbb!

IDE DRIVE



A600 Rev1.5 PCB

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MEMORY EXPANSION AND THE IDE DRIVE

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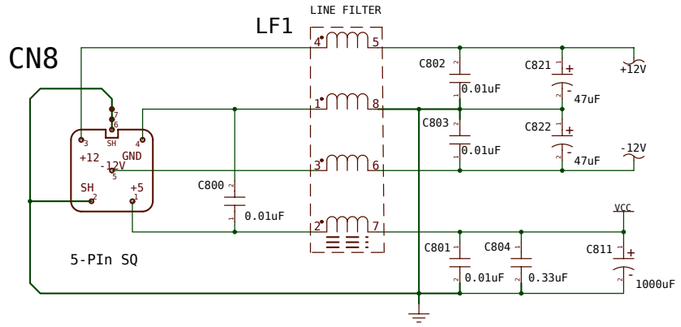
DESIGN BY: G. Robbins	DATE 05/27/91	Commodore
DRAW: GRR	05/27/91	Schematic A300 Rev 1
LAST: GRR	10/22/91	C/A300 Main Board "June Bug"
CHKD:		
APPR:		
USED ON: C/A300	NEXT ASSY: 315986	SIZE C 315987 REV 1
		SCALE SHEET 12 OF 13

PATH: /project/a300/june_bug.rev1 sheet12

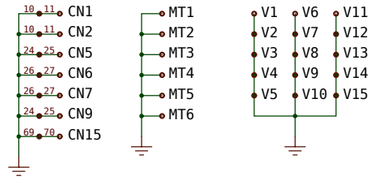
Rev.1.37 (02.09.2012)

POWER INPUT

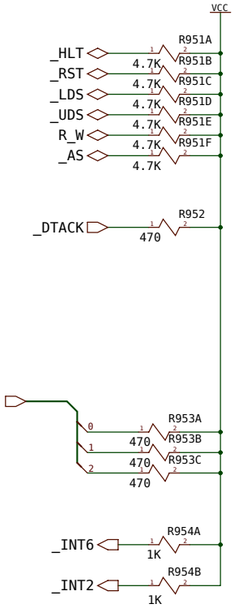


NOTE: HEAVY LINES INDICATE A
SINGLE POINT CONNECTION

GROUNDED HOLES, &c.



"BUS" TERMINATION



A600 Rev1.5 PCB

POWER DISTRIBUTION AND DECOUPLING

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DESIGN BY: G. Robbins	DATE 05/27/91	Commodore
DRAW: GRR	05/27/91	Schematic A300 Rev 1
LAST: GRR	10/22/91	C/A300 Main Board
CHKD:		"June Bug"
APPR:		
USED ON: C/A300	NEXT ASSY 315986	SIZE C 315987 REV 1
		SCALE SHEET 13 OF 13

PATH: /project/a300/june_bug_rev1 sheet13

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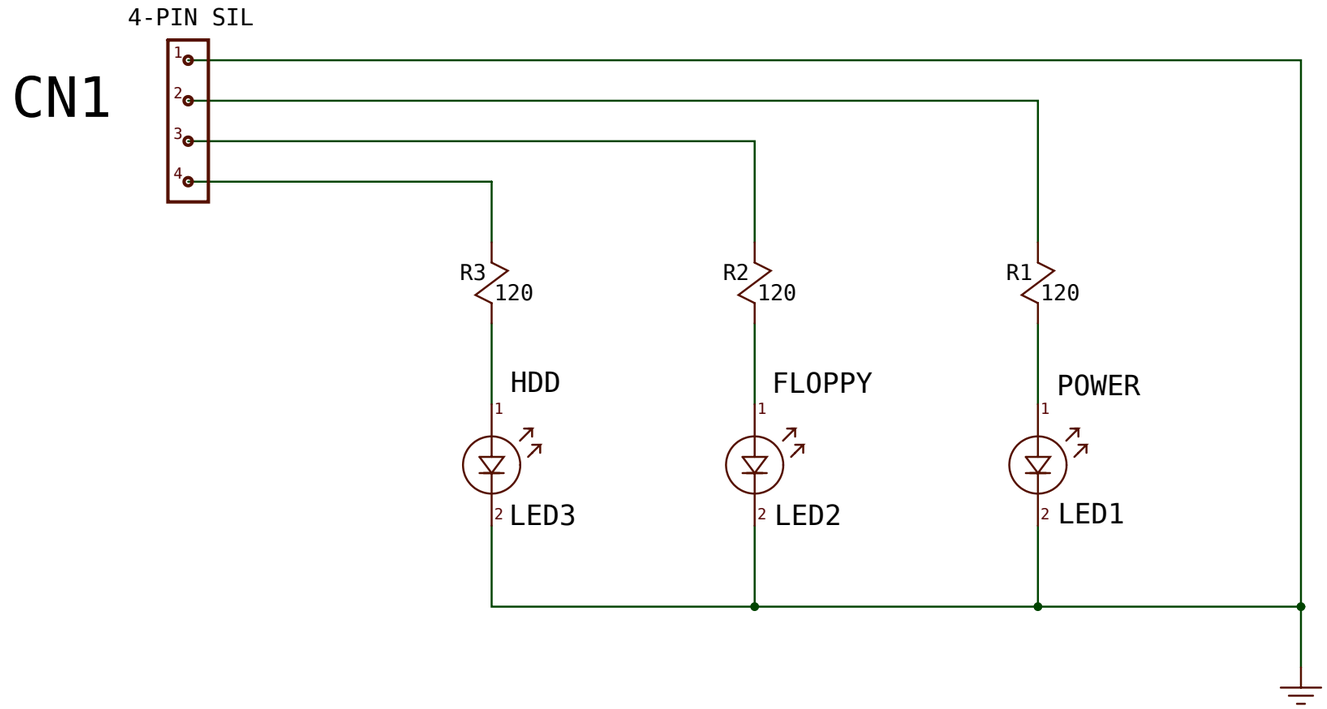
	REVISIONS			
REV	DESCRIPTION	DATE	APRVL	MANAGER
A	PILOT PRODUCTION RELEASE			



SHINE ON, SHINE ON

A300 PCB ASSEMBLY REV1

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DESIGN BY:	DATE
B. FENIMORE	11/19/91
DRAW: BAF	11/19/91
LAST: BAF	11/19/91
CHKD:	
APPR:	

USED ON	NEXT ASSY
A300	315992

Commodore
SCHEMATIC
A300 LED ASSY

SIZE		REV
A	364075	A

SCALE | SHEET 1 OF 1

PATH: /user/fenimore/A300/led_assy sheet1

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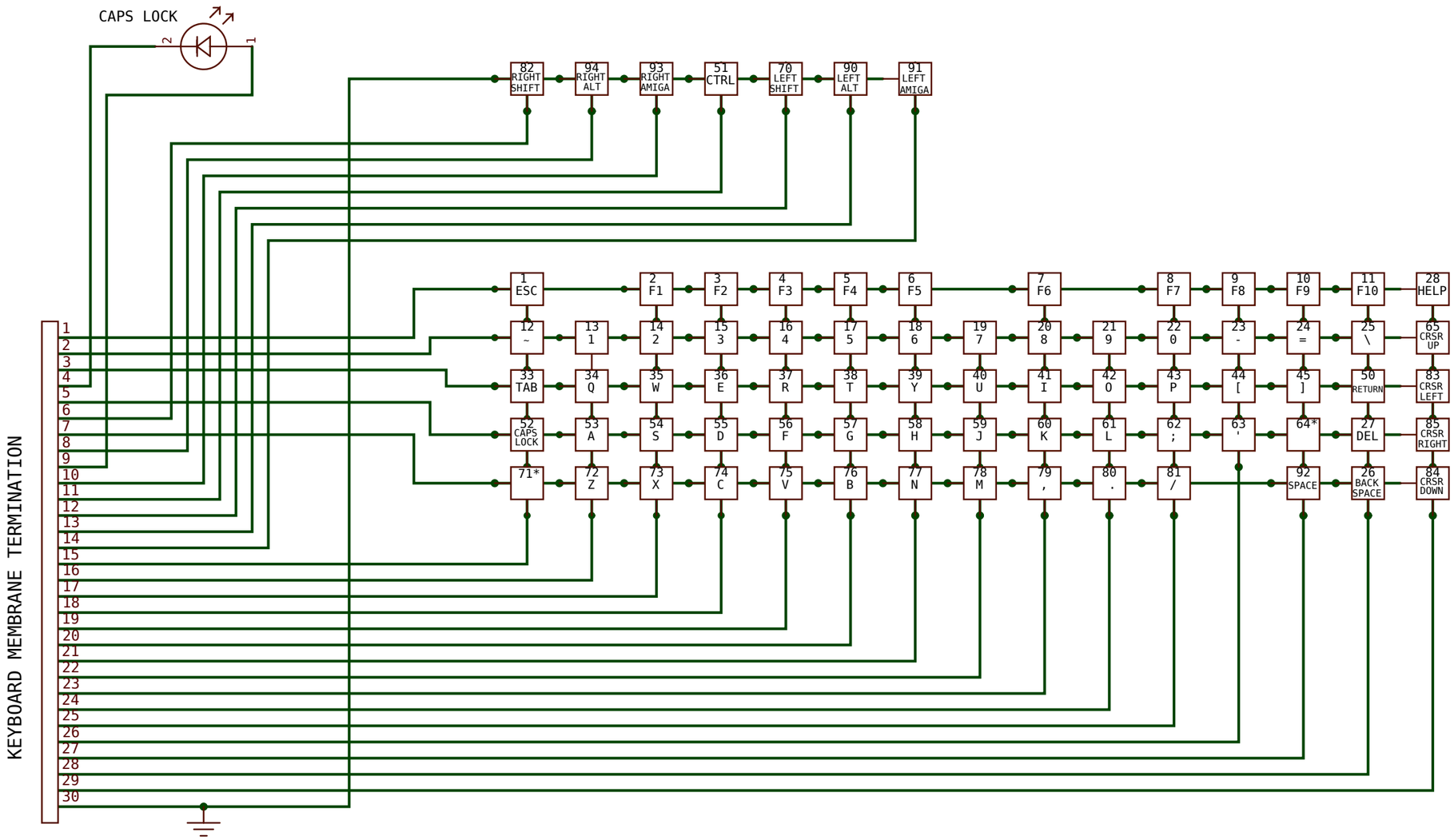

FIGURE 1

NOTES: 1)NUMBER AT TOP CENTER OF EACH BLOCK CORRESPONDS
TO KEY NUMBER IN ASSEMBLY DRAWING.
2)KEY NUMBERS 64 & 71 ARE ACTIVE ON EUROPEAN
KEYBOARDS ONLY.
3)PIN 30 OF TERMINATION CONNECTED TO GROUND FOR
EMI/RFI EMISSION REQUIREMENTS.

US VERSION (-01) SHOWN

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DRAWN BY: B.FENIMORE	DATE 3/21/91	Commodore
CHKD:		A300
ENGR:GRR/BAF		KEYBOARD MEMBRANE MATRIX
APPR:		
USED ON	NEXT ASSY	SIZE A · 363748 · REV 1
		SCALE · SHEET 1 OF 1

PATH:/USER/FENIMORE/A300/A300KEYMATRIX

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