Amiga A600_R2

Rev.1.37 (02.09.2012)



Jumpers and Stuff

REF	TYPE	DESCRIPTION	PAGE		
R246	SMT	NTSC Color Burst	4		
R202	SMT	PAL Color Burst	4		
R625	SMT	Keyboard MPU Clock	9		
R624	SMT	Keyboard/System Reset	9		
		·			
		· ·			

Connectors

REF	TYPE	DESCRIPTION	PAGE
CN1	DB9P	Mouse/Joystick 1	5
CN2	DB9P	Mouse/Joystick 2	5
CN3	RCA-J	Right Audio Output	5
CN4	RCA-J	Left Audio Output	5
CN5	DB23S	External Floppy	8
CN6	DB25P	RS232 Serial Port	7
CN7	DB25S	Parallel Printer Port	7
CN8	SQ DIN	Power Supply Connector	13
CN9	DB23P	Video Output	6
CN10	RCA-J	Composite Video	4
CN11	DIL-34	Internal Floppy Signal	8
CN12	SIL-4	Internal Floppy Power	8
CN13	MEM-30	Keyboard Membrane	9
CN14	SIL-4	Internal Floppy Power	8
CN13	MEM-30	Keyboard Membrane	9
CN14	SIL-4	Keyboard Status LED's	9
CN15	PCMCIA	PC"Memory Card"	11
		-	
P9	EDGE-80	Memory Bus Expansion	12
		•	

Revision History

REV	DESCRIPTION	DATE	APRVL	MANAGER
0	Engineering Prototype	08/01/91	GRR	
1	Pilot Production	10/22/91	GRR	
2	FCC/FTZ Production Version	04/09/92	GRR	

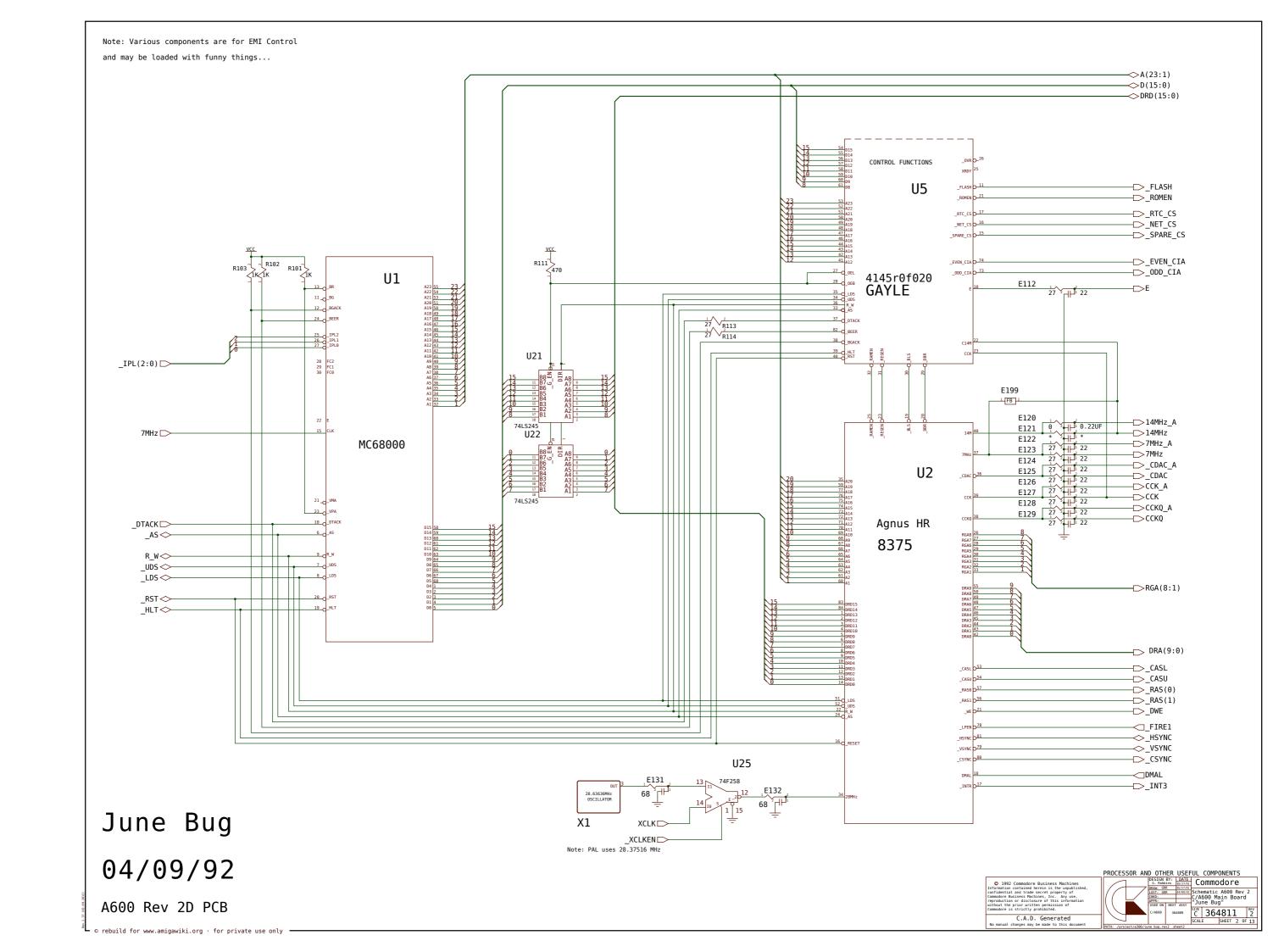
Signal Glossary

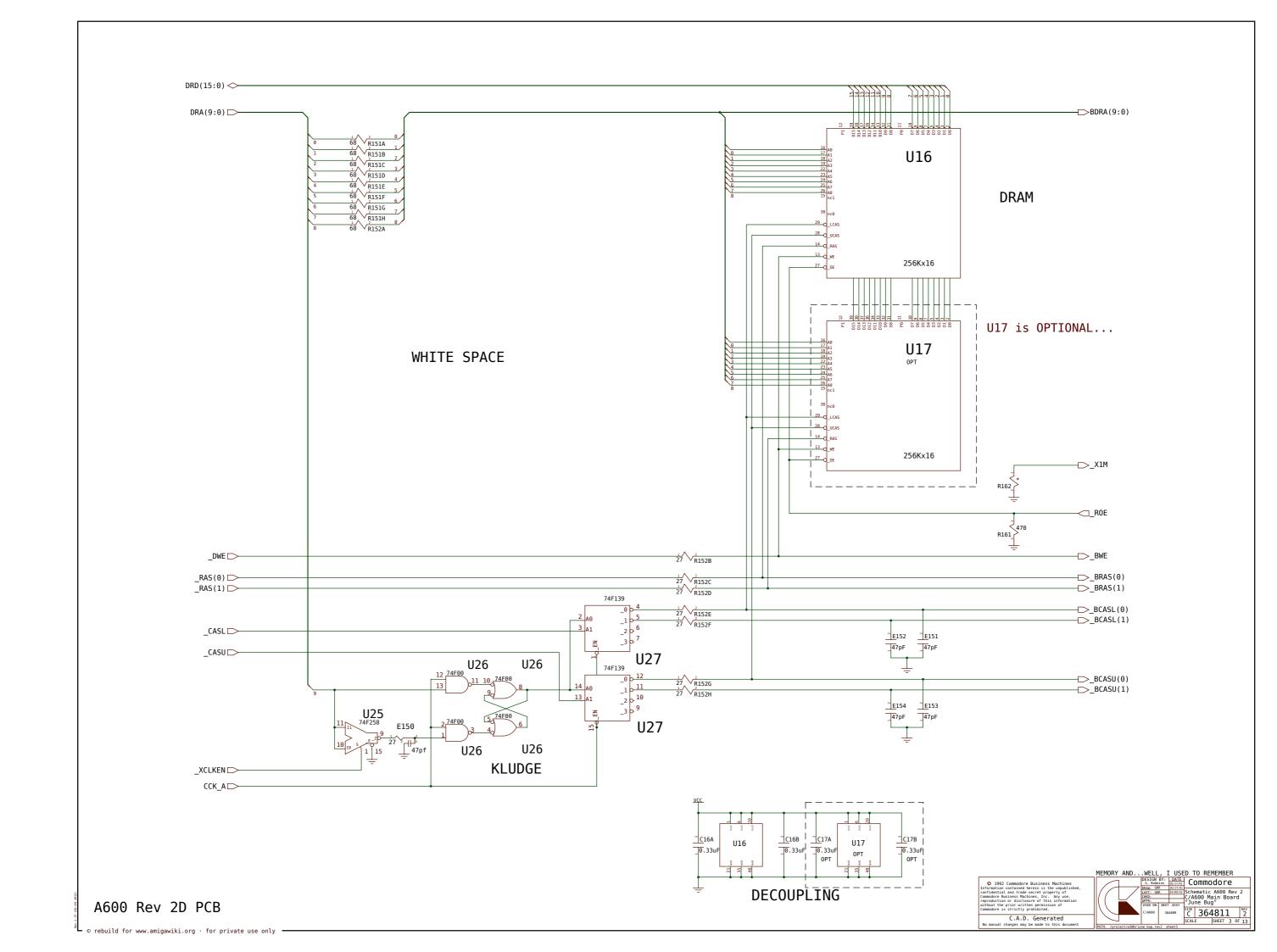
SIGNAL	DESCRIPTION (AREA)	PAGES
28MHZ	28.63636 MHz Master Clock	
7MHZ	7.15909 MHz Processor Clock	
A[23:1]	Processor Address Bus (68000)	
ACK	Data Acknowledge (Parallel Port)	
AS	Address Strobe (68000)	
AUDIN	Audio Input (RS232 Port)	
AUDOUT	Audio Output (RS232 Jack)	
BEER	Bus Error (68000)	
BG	Bus Grant (68000)	
BGACK	Bus Grant Acknowledge (68000)	
BLISS	Blitter Slowdown (Chips)	
BLIT	Chip Memory Access (Chips)	
BR	Bus Request (68000)	
BUSY	Device Busy (Parallel Port)	
CASL/U	Column Address Strobe (DRAM)	
CCK/CCK0	Color Clock / Quadrature (Chips)	
CDAC	7.15909 MHz Quadrature Clock (Chips)	
CHNG	Media Change (Floppy)	
CLKRD/WR	Read-Time Clock Read / Write (RTC)	
COMP	Monochrome Composite Video (Video)	
CSYNC	Composite Sync (Video)	
CTS	Clear to Send (RS232 Port)	
D[15:0]	Processor Data Bus (68000)	
DIR	Step Direction (Floppy)	
DKRD	Disk Read Data (Floppy)	
DKWD	Disk Write Data (Floppy)	
DKWE	Disk Write Enable (Floppy)	
DMAL	Chip DMA Request Line (Chips)	
DRA[8:0]	DRAM Address Bus (DRAM)	
DRD[15:0]	DRAM Data Bus (DRAM)	
DSR	Data Set Ready (RS232 Port)	
DTACK	Data Transfer Acknowledge (68000)	
DTR	Data Terminal Ready (RS232 Port)	
E	Peripheral Enable Clock (68000)	
EXTICK	Expansion Present / RTC Tick	
FC[2:0]	Function Code (68000)	
FIRE0/1	Fire Button 0/1 (Joysticks)	
HLT	Processor Halt (68000)	
HSYNC	Horizontal Sync (Video)	
INDEX	Index Pulse (Floppy)	
INT[2,3,6]	Interrupt Request (Chips)	
IORESET	I/O Reset	
IPL[2:0]	Interrupt Priority Level (68000)	
KBCLOCK	Keyboard Clock (Keyboard)	
KBDATA	Keyboard Data (Keyboard)	
KBRESET	Keyboard Reset (Keyboard)	
LDS/UDS	Upper / Lower Data Strobes (68000)	
	Power On LED / Audio Filter Disable	
LED (DICUT		
LEFT/RIGHT	Left Right Audio (Audio)	

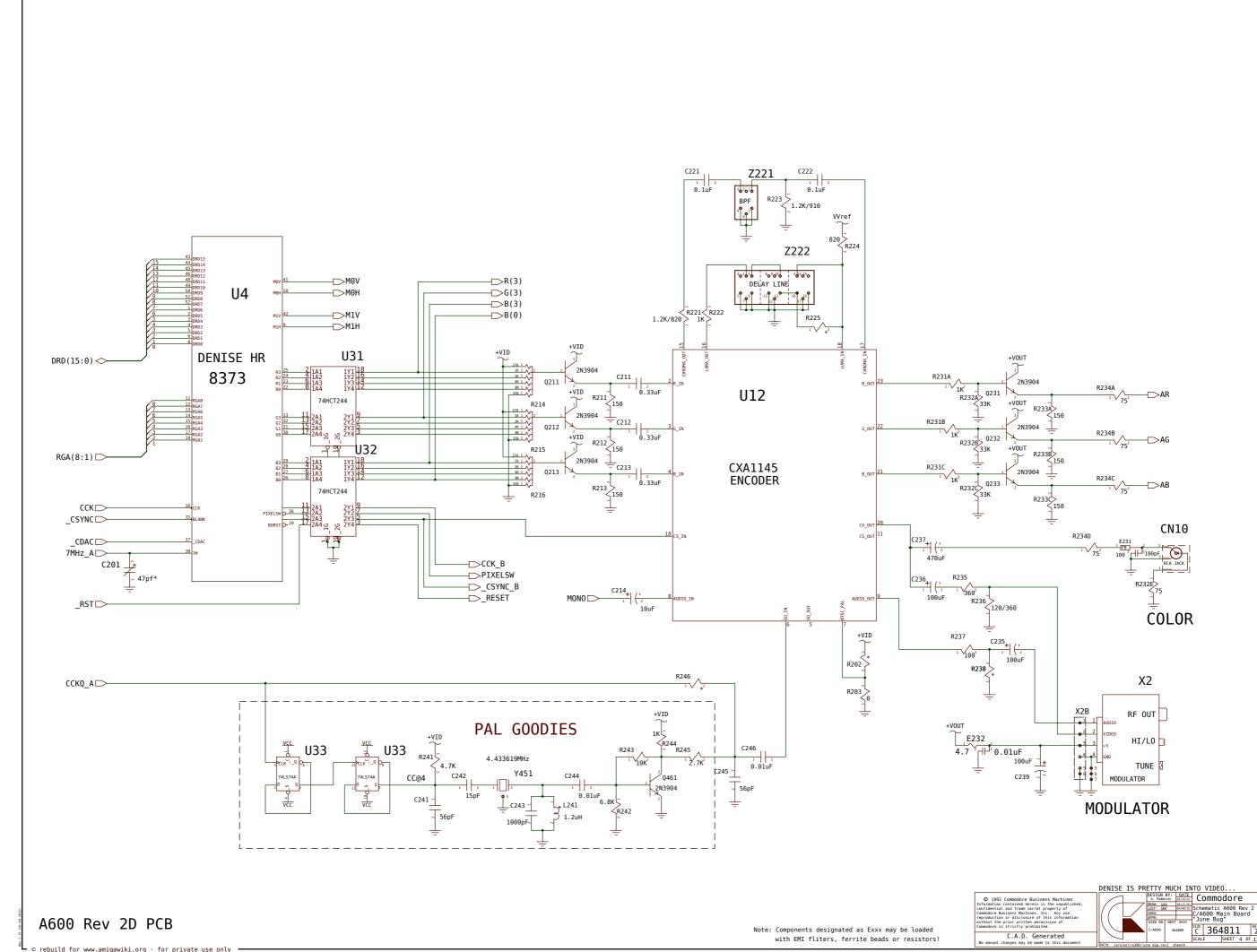
SIGNAL	DESCRIPTION (AREA)	PAGES
LPEN	Light Pen Trigger (Joysticks)	
MTR	Motor On (Floppy)	
MTR0	Motor On - Drive O (Floppy)	
MOV/MOH	Mouse 0 Quadrature V/H (Joysticks)	
M1V/M1H	Mouse 1 Quadrature V/H (Joysticks)	
OVL	Overlay ROM over RAM	
OVR	Override System Decoding	
PIXELSW	Genlock Pixel Switch (Video)	
POTOX/OY	Pot Lines 0 X/Y (Joysticks)	
POT1X/1Y	Pot Lines 1 X/Y (Joysticks)	
POUT	Paper Out (Parallel Port)	
PPD[7:01	Parallel Port Data (Parallel Port)	
RAMEN	RAM Enable (Chips)	
REGEN	Chip Register Enable (Chips)	
RAS0/1	Row Address Strobe (DRAM)	
RDY	Drive Ready (Floppy)	
RESET	General Reset	
RGA[8:1]	Register Address Bus (Chips)	
R/G/B	Red / Green / Blue (Video)	
RT	Ring Indicate (RS232 Port)	
ROMEN	ROM Enable (ROM)	
RTS	Request to Send (RS232 Port)	
RST	Processor Reset (68000)	
RXD	Receive Data (RS232 Port)	
RW	Processor Read/Write (68000)	
SEL	Select (Parallel Port)	
SEL[3:0]	Drive Select (Floppy)	
SIDE	Side Select (Floppy)	
STEP	Step In/Out Command (Floppy)	
TRK0	Track Zero Sense (Floppy)	
TXD	Transmit Data (RS232 Port)	
VMA	Valid Memory Address (68000)	
VPA	Valid Peripheral Address (68000)	
VSYNC	Vertical Sync (Video)	
WE	Write Enable (DRAM)	
WPROT	Write Protect Sense (Floppy)	
XCLK	External Genlock Clock (Video)	
XCLKEN	External Clock Enable (Video)	
XRDY	External Data Ready	
ANDI	LXCEITIAC Data Neady	
<u> </u>		
	** Credit Card and IDE Stuff? **	

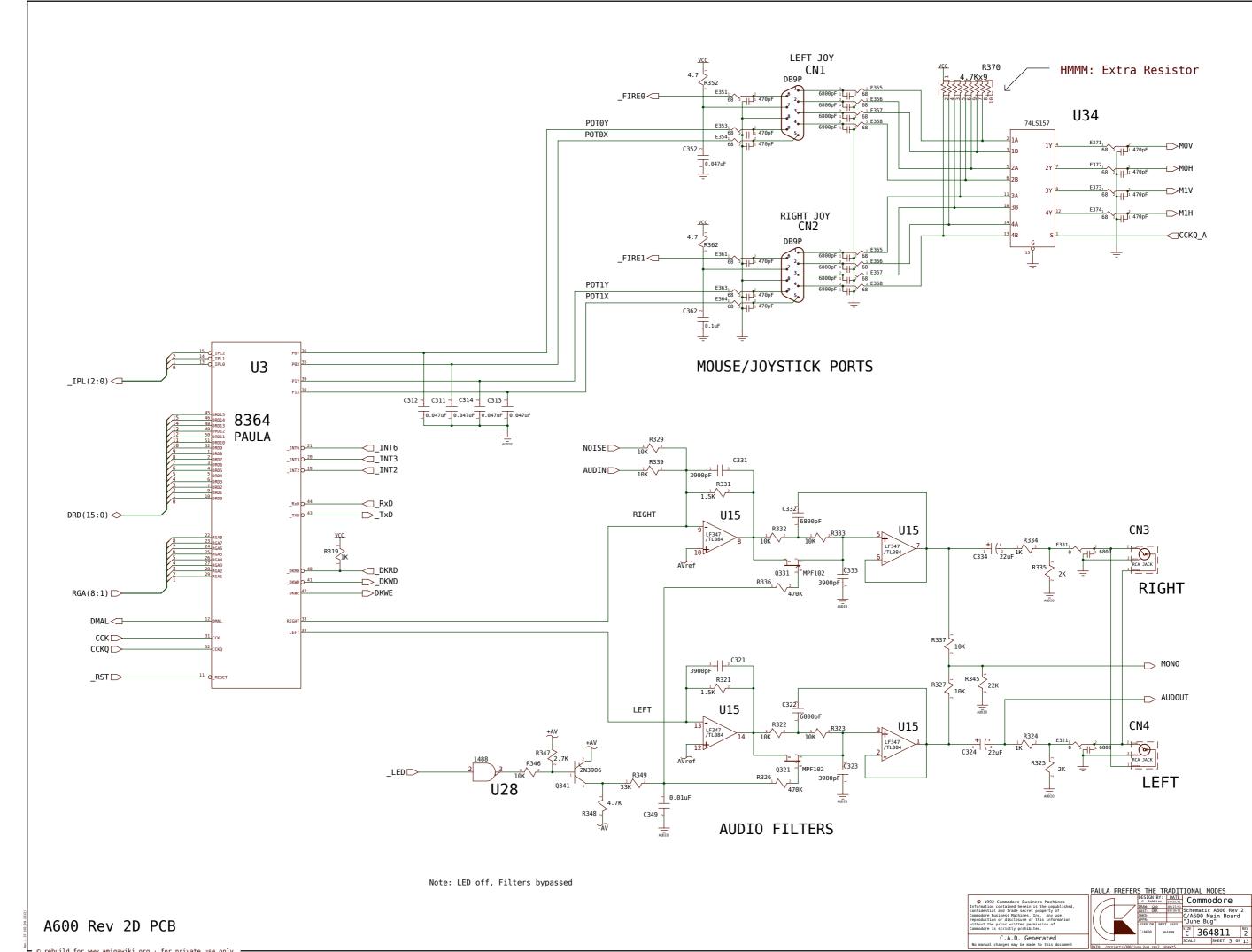
Key Components

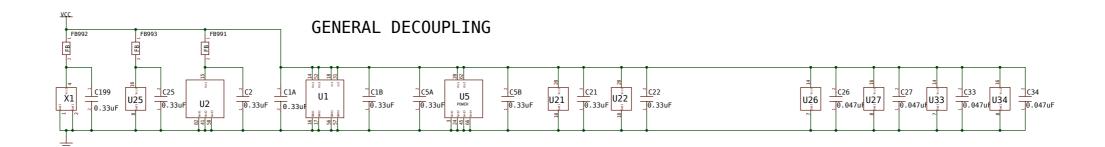
REF	CHIP	PAGE	
U1	68000	68000 Processor, 8MHz	2
U2	8375	ECS Agnus A300/A500+	2
U3	8364	Paula	5
U4	8373	ECS Denise	4
U5	4145-20	Gayle Gate Array	2,8,11
U6	asst	ROM 256Kx16, 200 nS	10
U7-8	8520	Amiga VIA, 1 MHz	7
U10-11	28F10	Flash Memory 128Kx8	10
U12		Sony Video Encoder	4
U13	6570-36	Amgia Keyboard MPU	9
U14	NE555	Reset Timer	9
U16-17	asst	DRAM 256Kx16, 120 nS	3
U15	LF347	BiMOS Op-Amp	5
013	TL084	BiMOS Op-Amp	alt
U28	1488	EIA Line Driver	7
U29	1489	EIA Line Receiver	7
029	1409	LIA LINE RECEIVE	
X1	0SC	TTL 28.63636 MHz NTSC	2
7.2	OSC	TTL 28.37512 MHz PAL	alt
Y451	XTAL	4.43619MHz PAL Burst	4
Y621	XTAL	3MHz Ceramic Resonator	9
X2	asst	PAL Video Modulator	4
	asst	NTSC Video Modulator	4



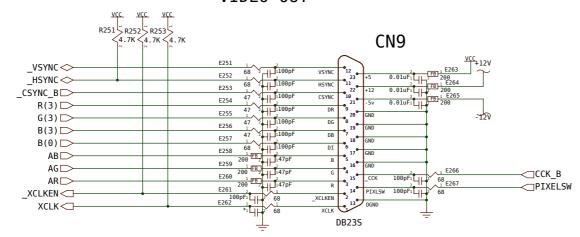


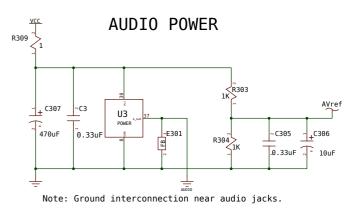


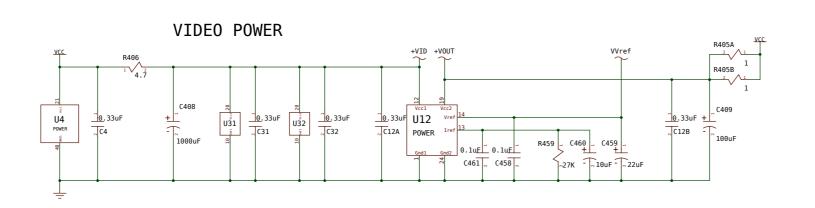


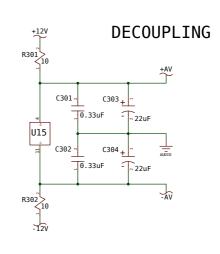


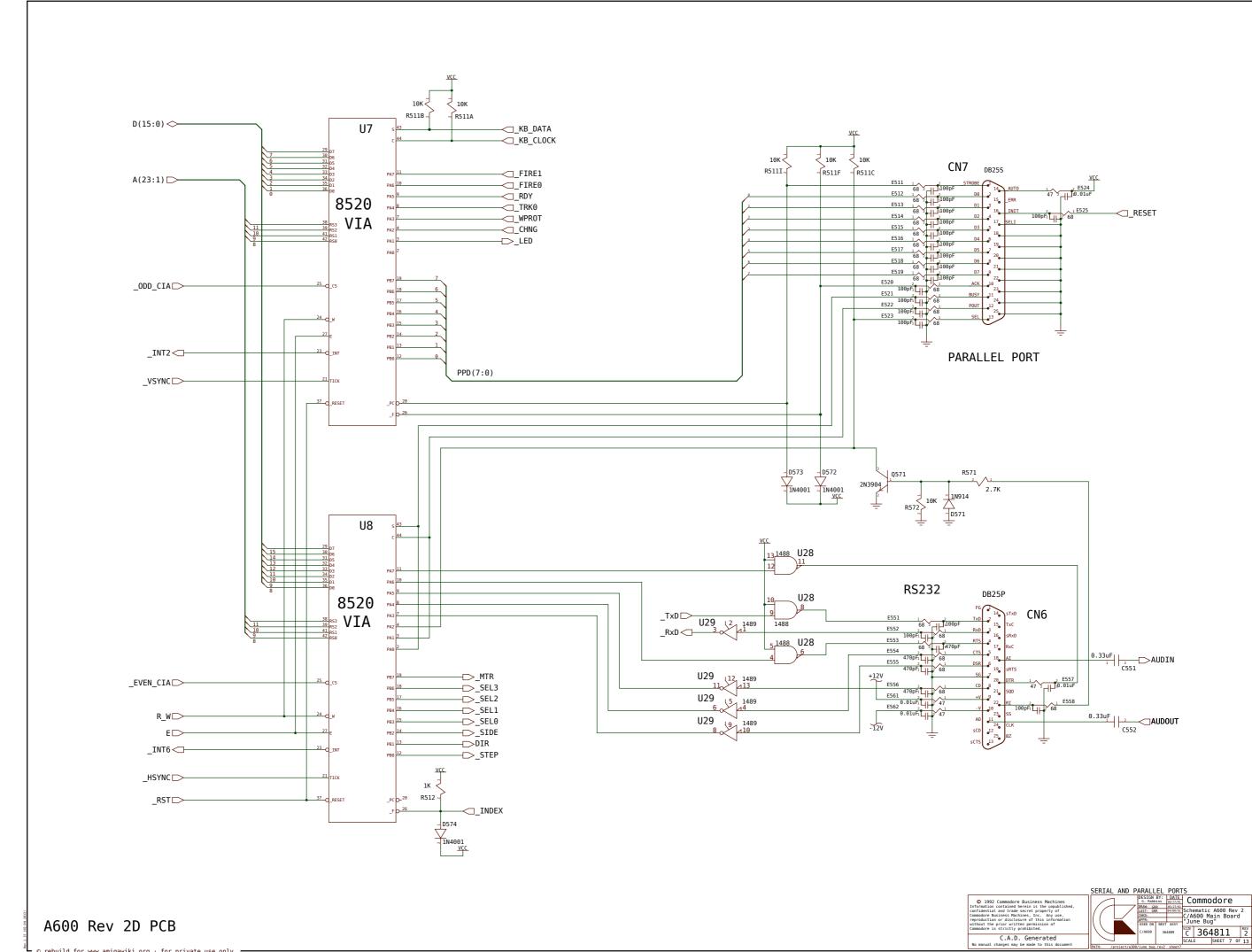
VIDEO OUT



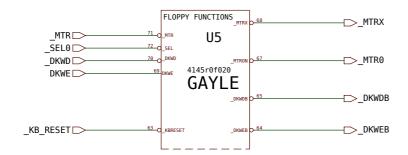




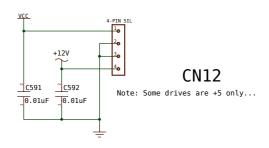




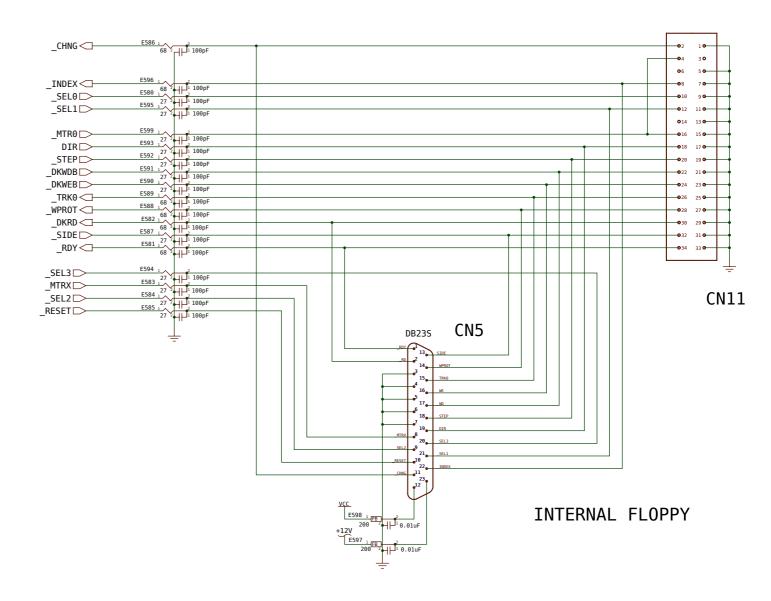
FLOPPY LOGIC

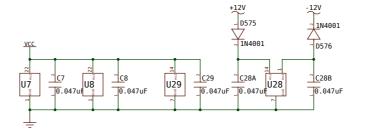


FLOPPY POWER



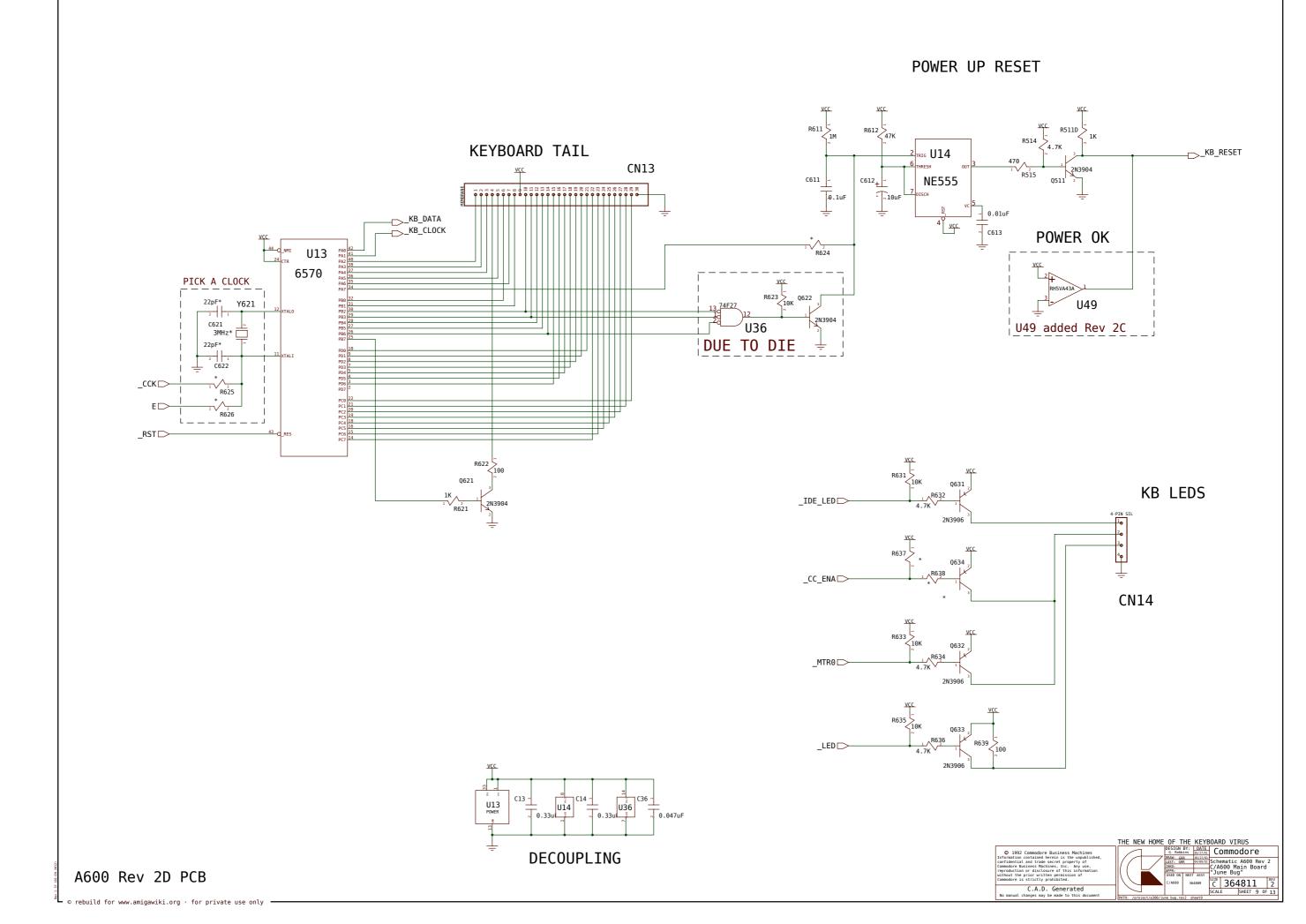
EXTERNAL FLOPPY

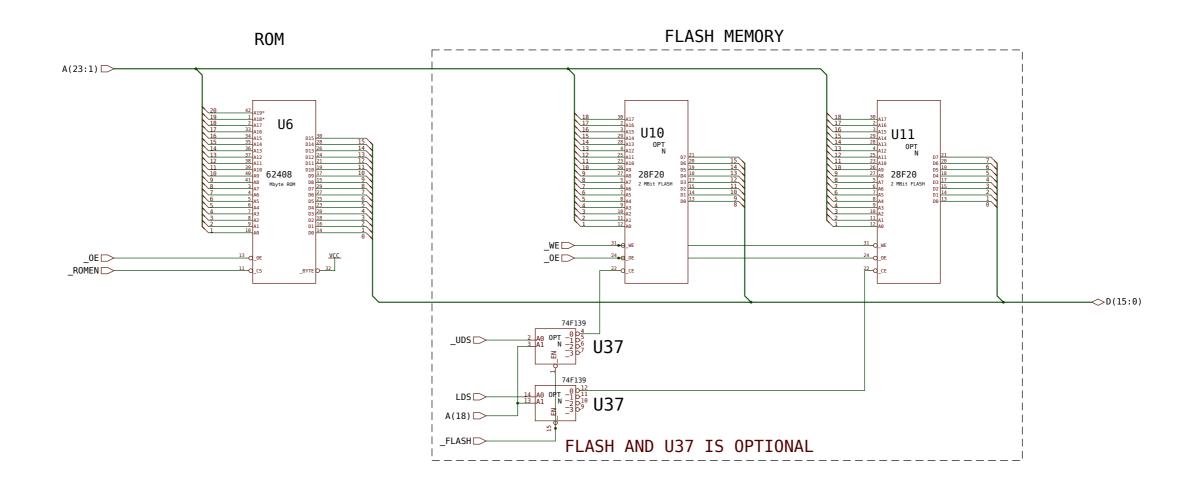


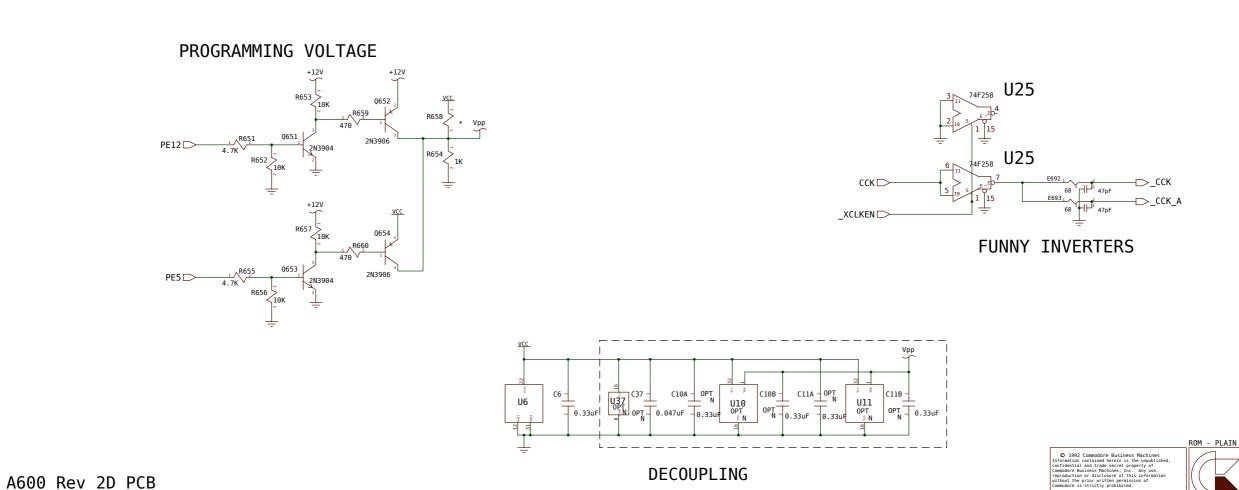


O 1992 Commodore Business Machines
Information contained herein is the empolitime,
confidential and trade secret property of
Commodore Business Machines, Inc. Any use,
reproduction or disclosure of this information
of the commodore is strictly prohibited.

C.A.D. Generated
No manual changes may be made to this document



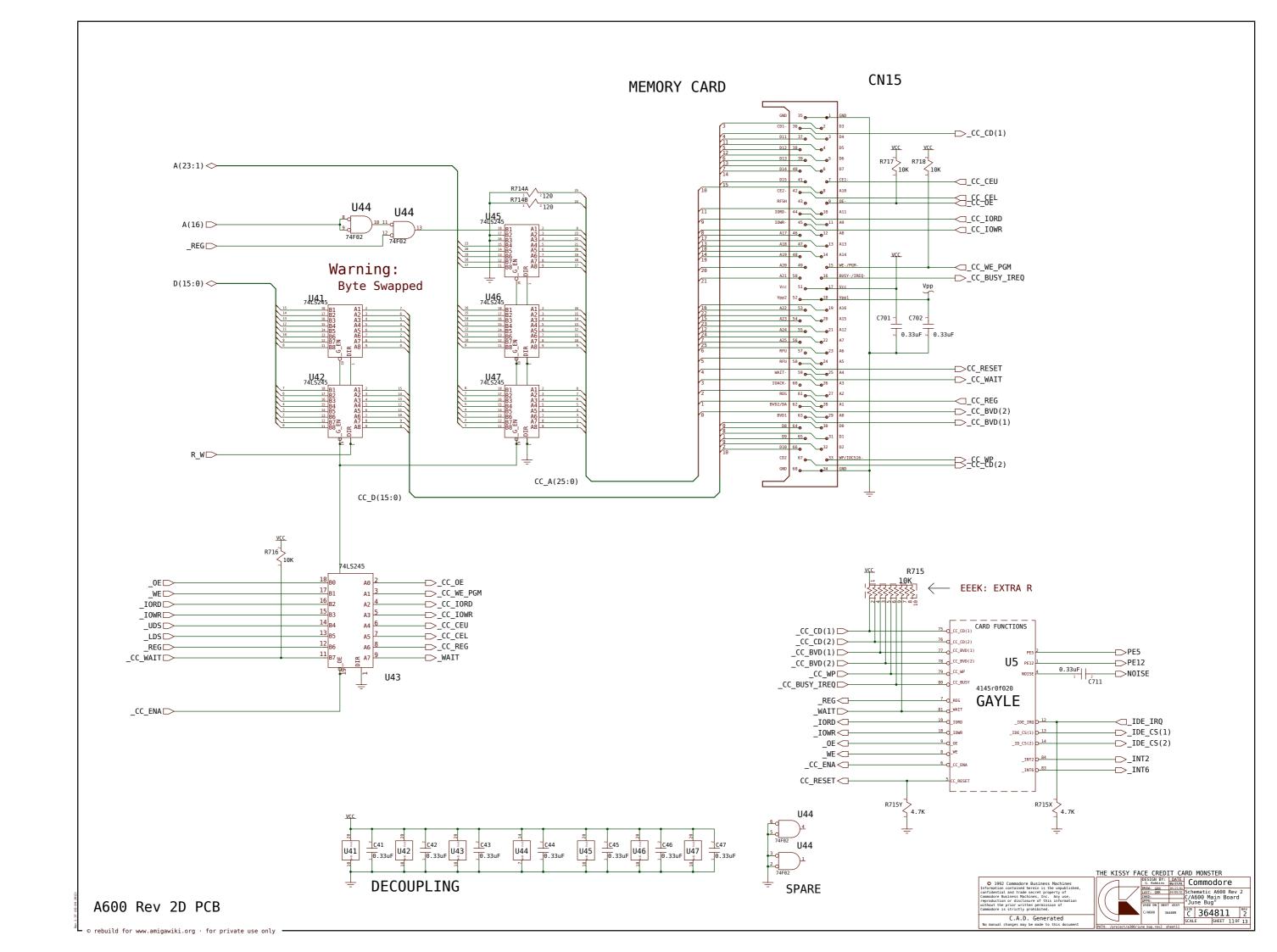




 $\ensuremath{\text{\ensuremath{\text{o}}}}$ rebuild for www.amigawiki.org \cdot for private use only -

Schematic A600 Rev C/A600 Main Board "June Bug" SIZE 364811 SCALE SHEET 10 0F

C.A.D. Generated changes may be made to this d

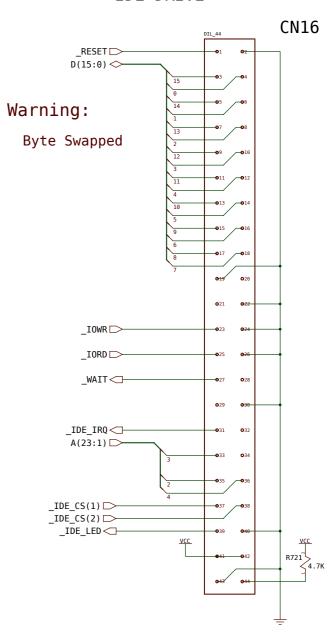


MEMORY EXPANSION

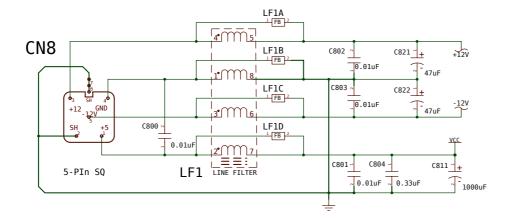
Р9_{усс} DRD(15:0) <> BDRA(9:0) □> RGA(8:1) D(15:0) <>--A(23:1) > BCASL(0) BCASU(1) _BCASU(0) D _BCASL(1) D _BRAS(0) -_____BRAS(1) _BWE _> R0E SPARE_CS _NET_CS 🗅 _INT2 🗁 __INT6 LEFT RIGHT ____TEST 14MHz_A □ RESET CCK▷ _IORD 🗁 ____IOWR ____SENSE _RTC_CS _> _X1M

Note: 14MHz or Vbb!

IDE DRIVE

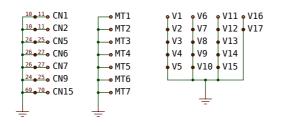


POWER INPUT

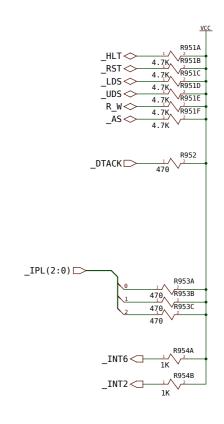


NOTE: HEAVY LINES INDICATE A SINGLE POINT CONNECTION LF1/LF1A... DUAL FOOTPRINT

GROUNDED HOLES, &c.



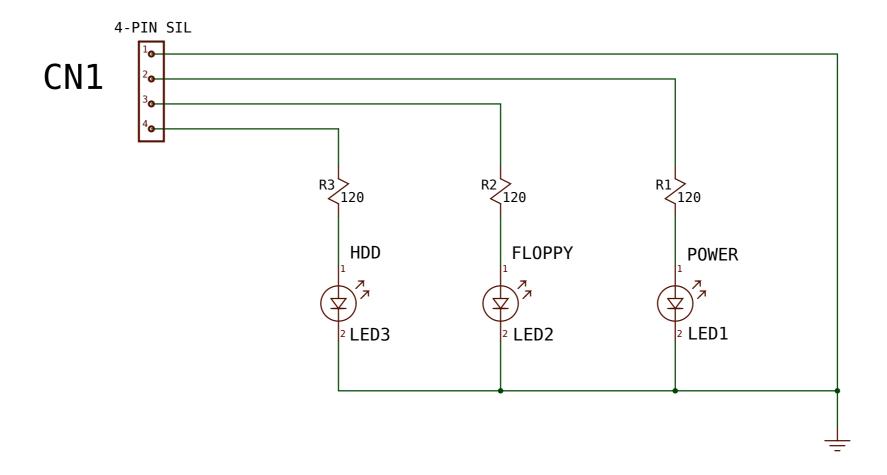
"BUS" TERMINATION



POWER DISTRIBUTION AND DECOUPLING

| O 1992 Commodore Business Machines | Information contained herein is the unpublished, confidential and trade serier property of Commodore Business Machines, Inc. Any use, to confidential and trade serier property of Commodore Business Machines, Inc. Any use, to commodore Business Machines | Commodore Business | Commod

	REVISIONS			
REV	DESCRIPTION	DATE	APRVL	MANAGER
Α	PILOT PRODUCTION RELEASE			



SHINE ON, SHINE ON

A300 PCB ASSEMBLY REV1

© 1991 Commodore Business Machines
Information contained herein is the unpublished,
confidential and trade secret property of
Commodore Business Machines, Inc. Any use,
reproduction or disclosure of this information
without the prior written permission of
Commodore is strictly prohibited.

C.A.D. Generated

No manual changes may be made to this document

						ommo	dore		
		DRAW: BA LAST: BA		11/19/91 11/19/91	- CCUENATEC				
l/ / L		CHKD:			A300 LED ASSY				
=	=	APPR:			M300 EED M331				
		USED ON	NEXT	ASSY	SY .				
	A300	31	5992	^{SIZE} 364075				REV A	
					SCAL	E	SHEET 1	0F	1
PATH: /user/fenimore/A300/led_assy sheet1									

Rev.1.37 (02.09.2012)

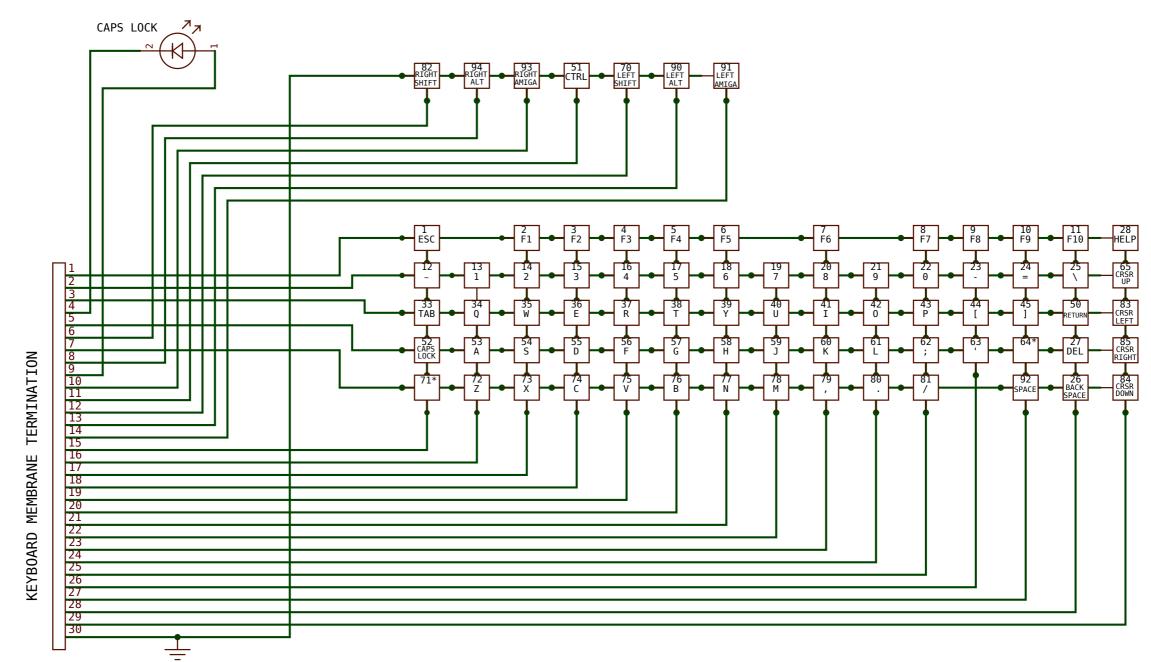
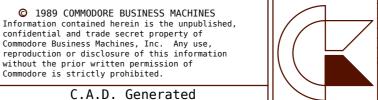


FIGURE 1

NOTES: 1) NUMBER AT TOP CENTER OF EACH BLOCK CORRESPONDS TO KEY NUMBER IN ASSEMBLY DRAWING.

- 2)KEY NUMBERS 64 & 71 ARE ACTIVE ON EUROPEAN KEYBOARDS ONLY.
- 3)PIN 30 OF TERMINATION CONNECTED TO GROUND FOR EMI/RFI EMISSION REQUIREMENTS.

US VERSION (-01) SHOWN



No manual changes may be made to this document

