# Amiga **CD32\_R4**

Rev.1.43 (27.09.2015)



#### Jumpers and Stuff

	1-0	1	1
REF	TYPE	DESCRIPTION	PAGE
R203	SMT	PAL/NTSC COMPOSITE	4
R205	SMT	M/N-PAL COMPOSITE	4
R245	SMT	PAL SUBCARRIER	4
R246	SMT	NTSC SUBCARRIER	4
R596-9	SMT	ROM SIZE/WIDTH	3
R765	SMT	CD POWER BYPASS	6
XJ1	SMT	32 BIT ROM OPTION	3
SW1	PTH	POWER SWITCH	9
		·	

#### Connectors

REF	TYPE	DESCRIPTION	PAGE
CN1	DB9P	Game Controller #1	5
CN2	DB9P	Mouse Controller #2	5
CN3	RCA-J	Right Audio Output	7
CN4	RCA-J	Left Audio Output	7
CN8	DIN-4	Power Connector	9
CN9	M.DIN-4	S-Video	4
CN10	RCA-J	Composite Video	4
CN13	M.DIN-6	Keyboard	5
CN14	2mm10x1	LED/Headphone PCB	6
CN17	Flex-23	CD Drive	6
P1	Edge182	Expansion Connector	8
		•	
X2	RCA	Modulator/RF	4

## Revision History

REV	DESCRIPTION	DATE	APRVL	MANAGER
Α	Production Release	08/12/93		
В	Revised per ECO 930277	09/14/93		
С	Revised per ECO 930305	10/18/93		

#### Signal Glossary

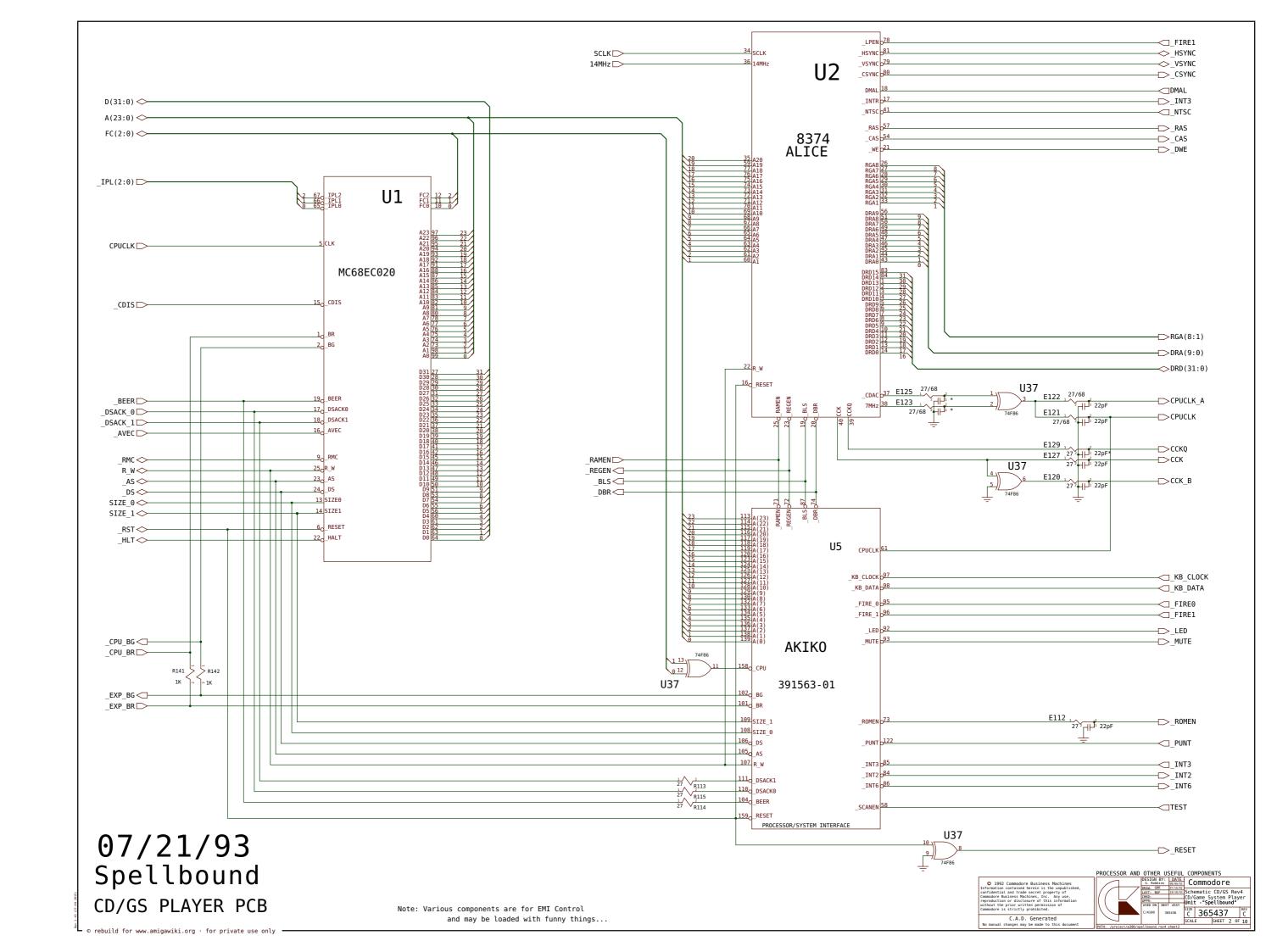
SIGNAL	DESCRIPTION (AREA)	PAGES
28MHZ	28.63636 MHz Master Clock	
7MHZ	7.15909 MHz Processor Clock	
A[23:1]	Processor Address Bus (68000)	
ACK	Data Acknowledge (Parallel Port)	
AS	Address Strobe (68000)	
AUDIN	Audio Input (RS232 Port)	
AUDOUT	Audio Output (RS232 Jack)	
BEER	Bus Error (68000)	
BG	Bus Grant (68000)	
BGACK	Bus Grant Acknowledge (68000)	
BLISS	Blitter Slowdown (Chips)	
BLIT	Chip Memory Access (Chips)	
BR	Bus Request (68000)	
BUSY	Device Busy (Parallel Port)	
CASL/U	Column Address Strobe (DRAM)	
CCK/CCK0	Color Clock / Quadrature (Chips)	
CDAC	7.15909 MHz Quadrature Clock (Chips)	
CHNG	Media Change (Floppy)	
CLKRD/WR	Read-Time Clock Read / Write (RTC)	
COMP	Monochrome Composite Video (Video)	
CSYNC	Composite Sync (Video)	
CTS	Clear to Send (RS232 Port)	
D[15:0]	Processor Data Bus (68000)	
DIR	Step Direction (Floppy)	
DKRD	Disk Read Data (Floppy)	
DKWD	Disk Write Data (Floppy)	
DKWE	Disk Write Enable (Floopy)	
DMAL	Chip DMA Request Line (Chips)	
DRA[8:0]	DRAM Address Bus (DRAM)	
DRD[15:0]	DRAM Data Bus (DRAM)	
DSR DSR	Data Set Ready (RS232 Port)	
DTACK	Data Transfer Acknowledge (68000)	
DTR	Data Terminal Ready (RS232 Port)	
E	Peripheral Enable Clock (68000)	
EXTICK	Expansion Present / RTC Tick	
FC[2:0]	Function Code (68000)	
FIRE0/1	Fire Button 0/1 (Joysticks)	
HLT	Processor Halt (68000)	
HSYNC	Horizontal Sync (Video)	
INDEX	Index Pulse (Floppy)	
INT[2,3,6]	Interrupt Request (Chips)	
IORESET	I/O Reset	
IPL[2:0]	Interrupt Priority Level (68000)	
KBCL0CK	Keyboard Clock (Keyboard)	
KBDATA	Keyboard Data (Keyboard)	
KBRESET	Keyboard Reset (Keyboard)	
LDS/UDS	Upper / Lower Data Strobes (68000)	
LED LED	Power On LED / Audio Filter Disable	
LEFT/RIGHT	Left Right Audio (Audio)	
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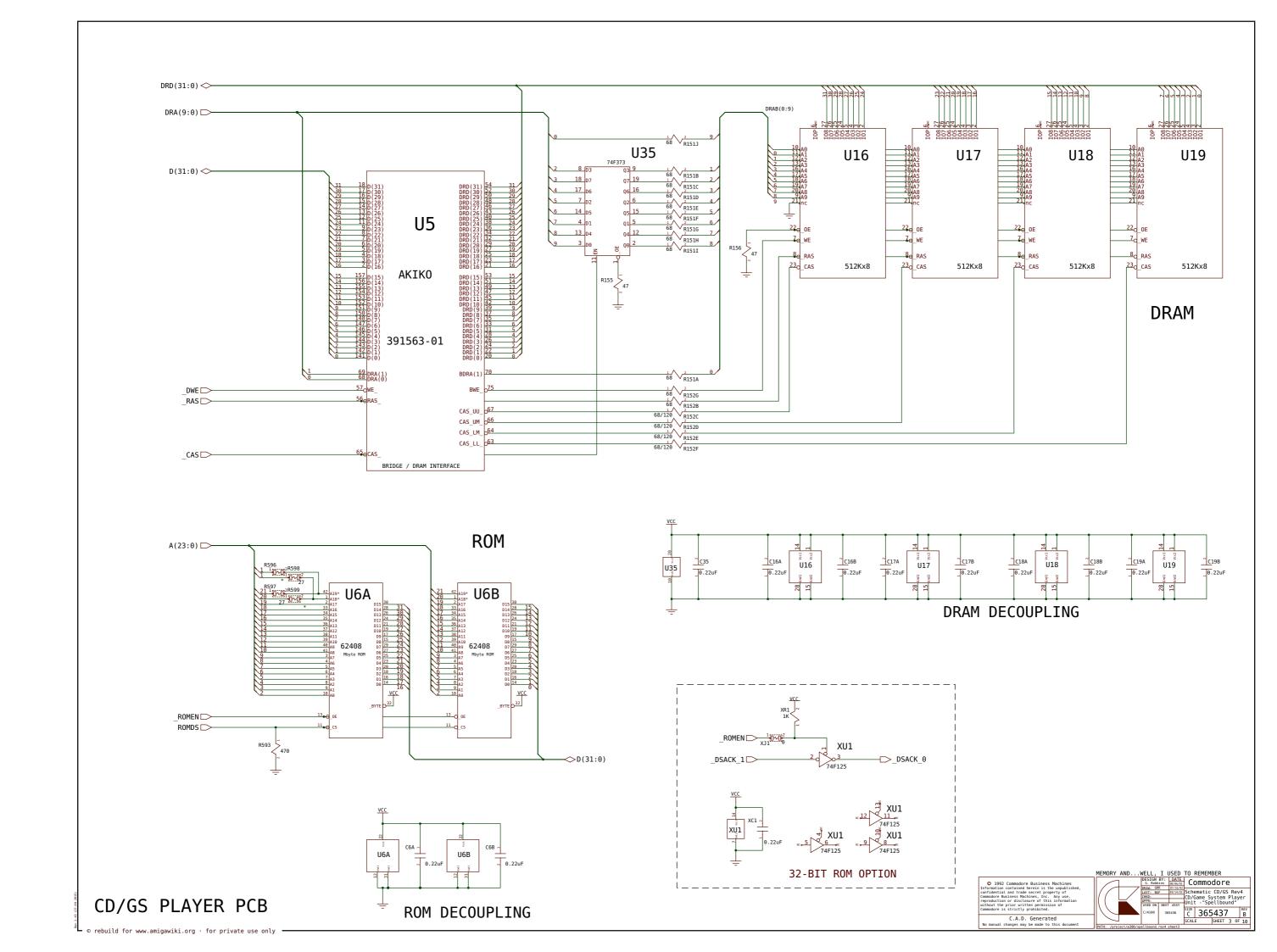
SIGNAL	DESCRIPTION (AREA)	PAGES	
LPEN	Light Pen Trigger (Joysticks)		
MTR	Motor On (Floppy)		
MTR0	Motor On - Drive 0 (Floppy)		
MOV/MOH	Mouse 0 Quadrature V/H (Joysticks)		
M1V/M1H	Mouse 1 Quadrature V/H (Joysticks)		
OVL	Overlay ROM over RAM		
OVR	Override System Decoding		
PIXELSW	Genlock Pixel Switch (Video)		
POTOX/OY	Pot Lines 0 X/Y (Joysticks)		
POT1X/1Y	Pot Lines 1 X/Y (Joysticks)		
POUT	Paper Out (Parallel Port)		
PPD[7:0]	Parallel Port Data (Parallel Port)		
RAMEN	RAM Enable (Chips)		
REGEN	Chip Register Enable (Chips)		
RAS0/1	Row Address Strobe (DRAM)		
RDY	Drive Ready (Floppy)		
RESET	General Reset		
RGA[8:1]	Register Address Bus (Chips)		
R/G/B	Red / Green / Blue (Video)		
RI	Ring Indicate (RS232 Port)		
ROMEN	ROM Enable (ROM)		
RTS	Request to Send (RS232 Port)		
RST	Processor Reset (68000)		
RXD	Receive Data (RS232 Port)		
RW	Processor Read/Write (68000)		
SEL	Select (Parallel Port)		
SEL[3:0]	Drive Select (Floppy)		
SIDE	Side Select (Floppy)		
STEP	Step In/Out Command (Floppy)		
TRK0	Track Zero Sense (Floppy)		
TXD	Transmit Data (RS232 Port)		
VMA	Valid Memory Address (68000)		
VPA	Valid Peripheral Address (68000)		
VSYNC	Vertical Sync (Video)		
WE	Write Enable (DRAM)		
WPROT			
XCLK	Write Protect Sense (Floppy) External Genlock Clock (Video)		
XCLKEN	External Clock Enable (Video)		
XRDY	External Data Ready		
ARUT	External Data Reduy		
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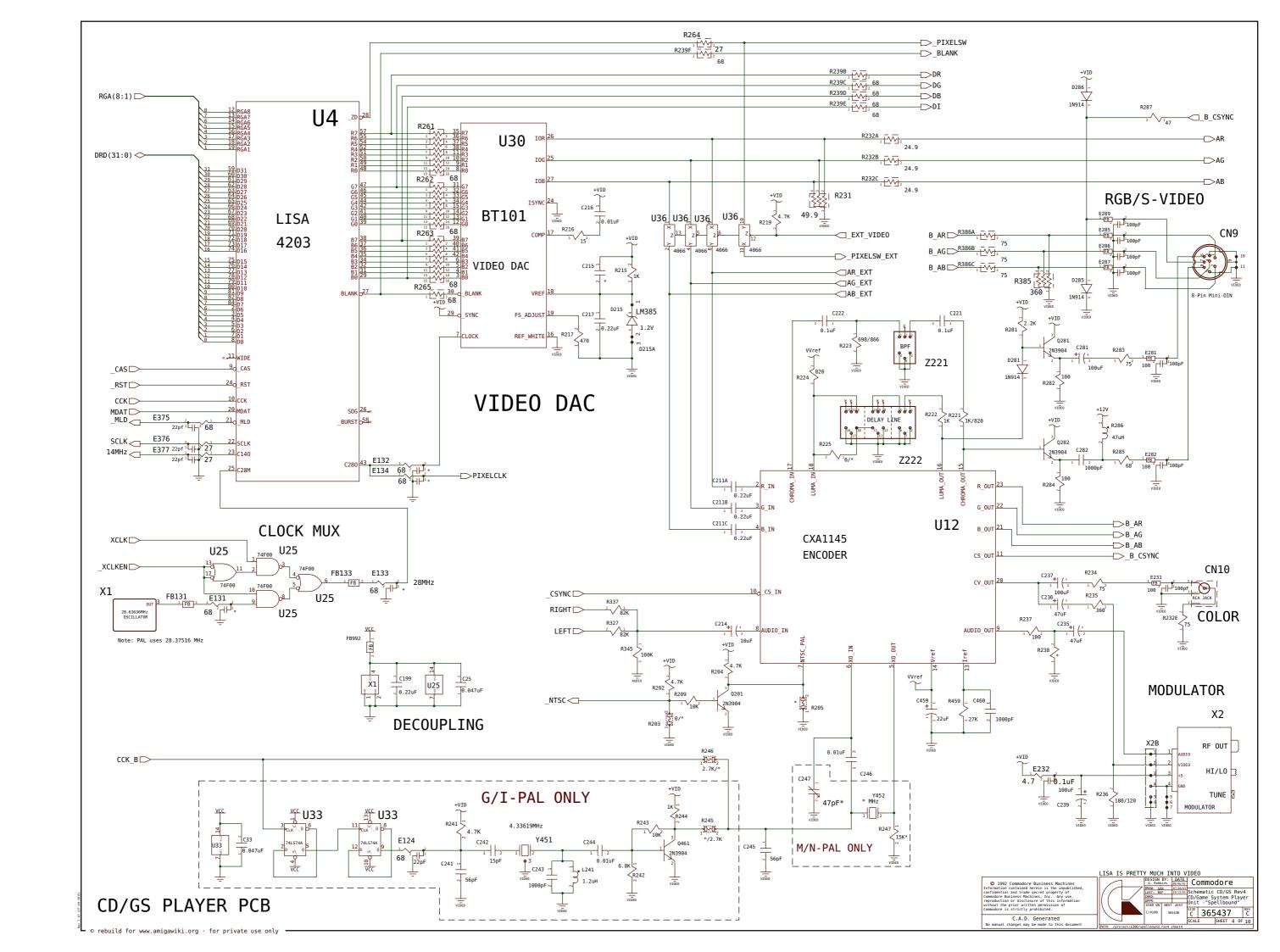
#### Key Components

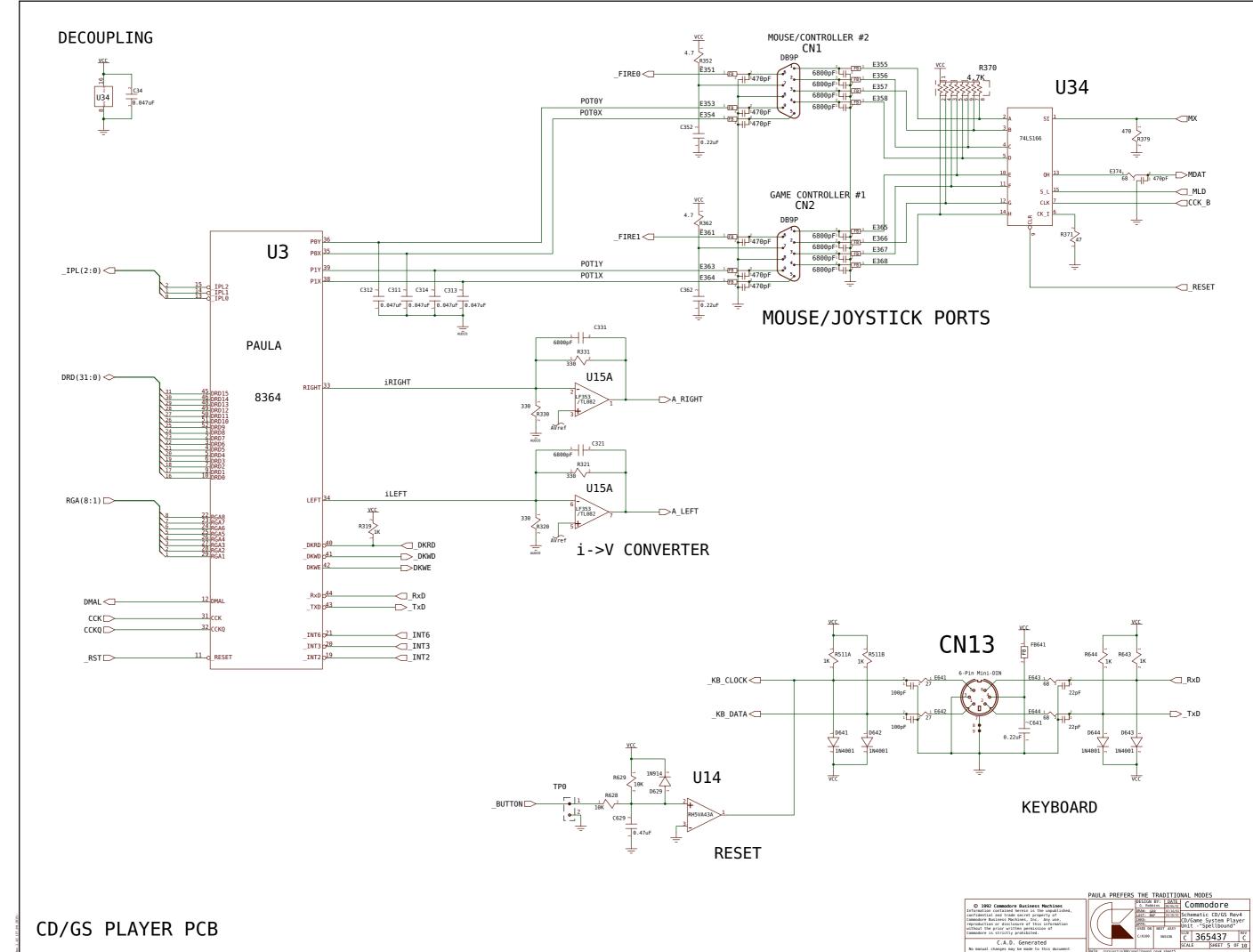
REF	CHIP	DESCRIPTION	PAGE
U1	68EC020	68EC020 Proc. 16MHz	2
U2	8374	Alice	2
U3	8364	Paula	5
U4	4203	Lisa	4
U5	391563	AKIKO	2,3,6
U6	27C8000	CD32 ROM 256Kx16,120nS	3
U9	24C08	Serial NVRAM	6
U12	CXA1145	Composite Encoder	4
U14,49	RH5VA43	Voltage Sense IC	5,7
U16-19	514800	DRAM 512Kx8, 80nS	3
U30	BT101	Triple 8-bit Video DAC	4
U31	LC78835	16-bit Audio DAC	7
U39	CXA1553	Headphone Amplifier	7
D215	LM385	DAC Reference Diode	4
X1	TTL-0SC	28.63636 MHz (NTSC)	4
	TTL-0SC	28.37516 MHz (PAL)	4
X2	VA3424	RF Modulator (NTSC)	4
	UD3626	RF Modulator (PAL)	4
Х3	TTL-0SC	16.9344 MHz	6
Y451	XTAL	4.433619 MHz (PAL)	4
Y452	XTAL	M/N-PAL	4
Z221	BPF	Chroma Bandpass Filter	4
Z221 Z222	Delav	Luma Delav Line	4
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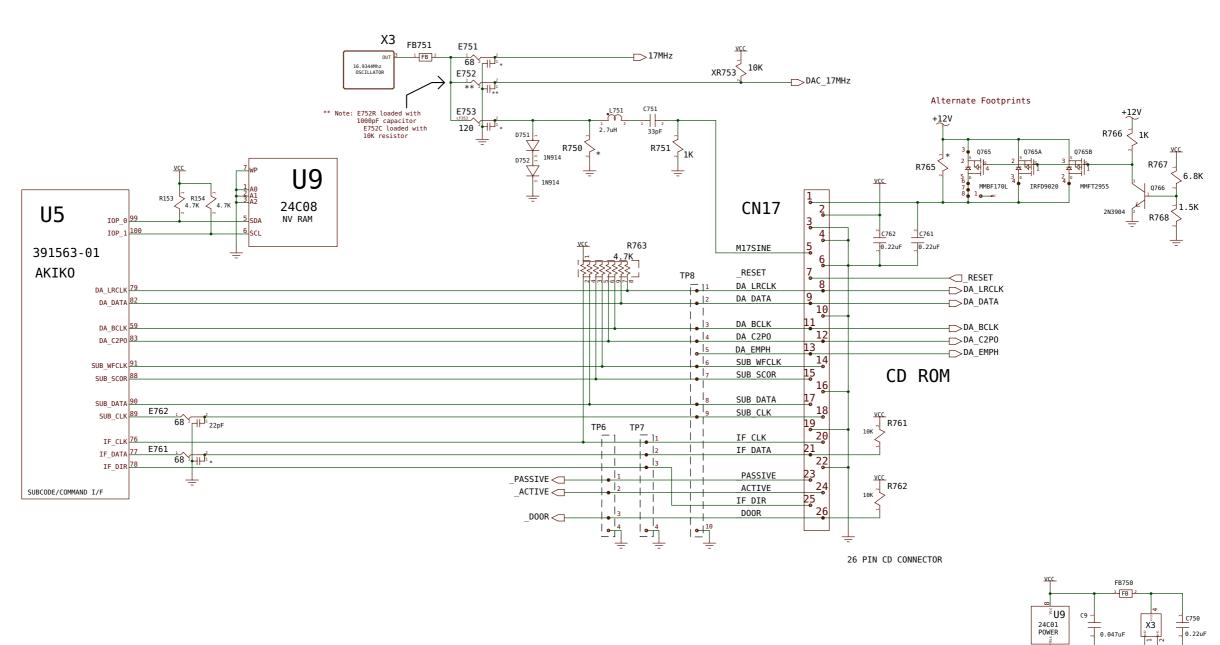
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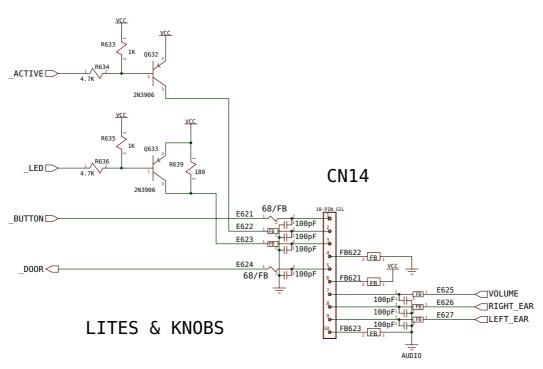


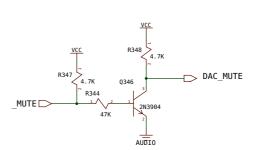








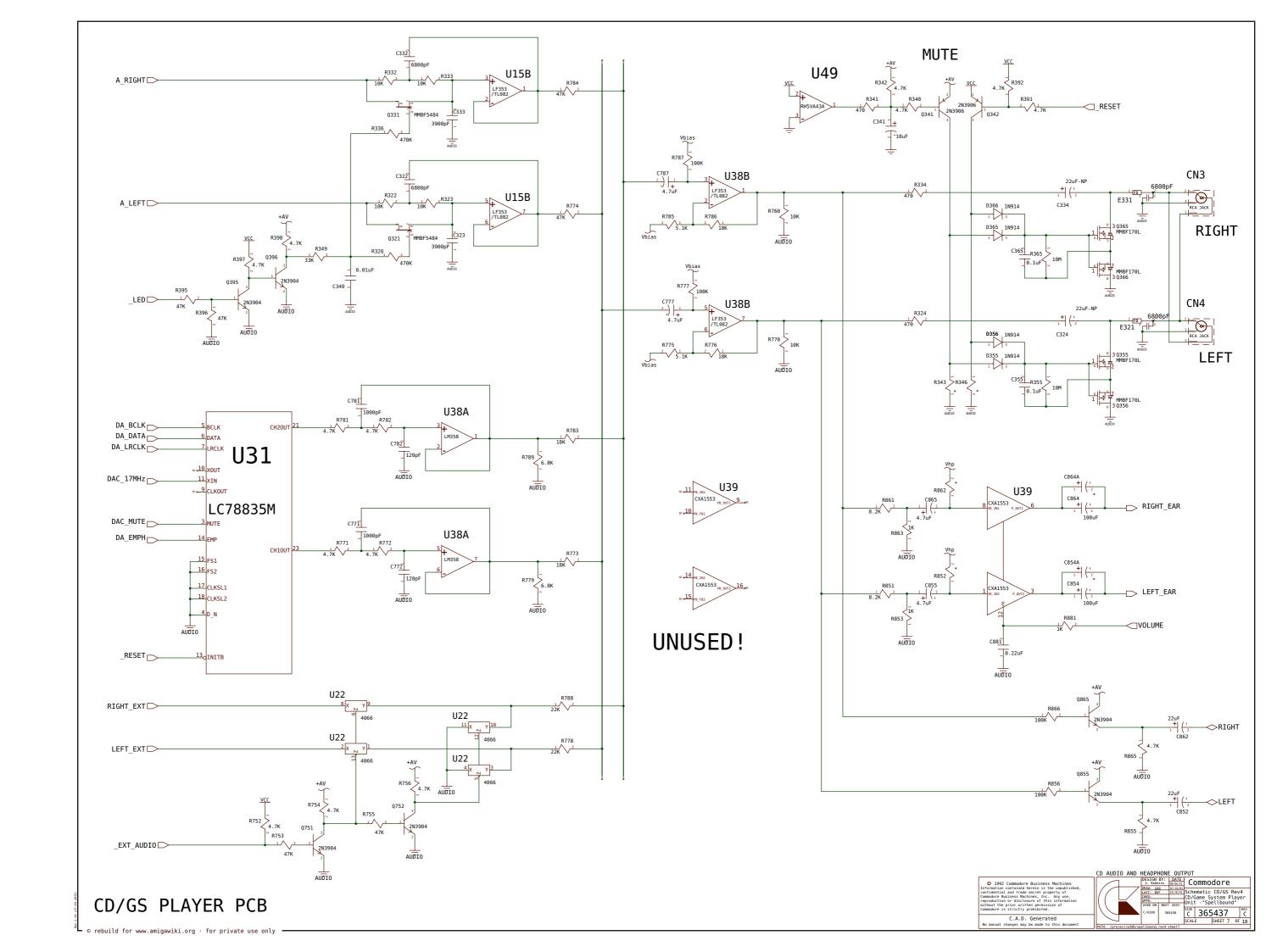




INVERTER

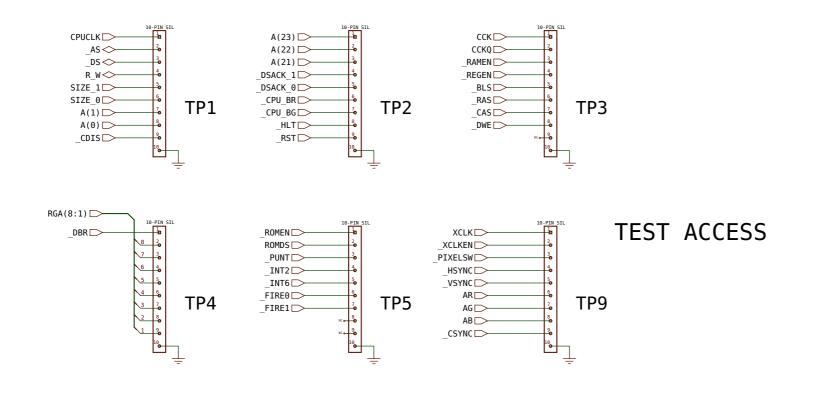


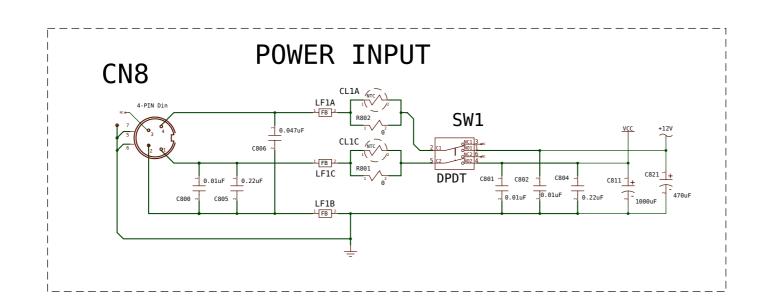
**DECOUPLING** 

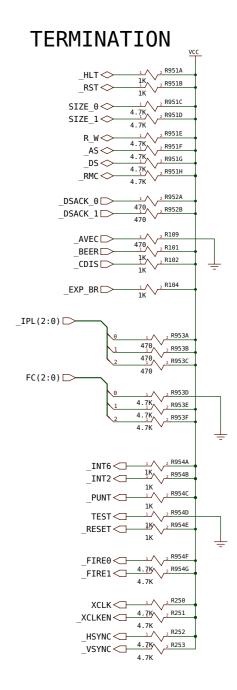


#### **EXPANSION CONNECTOR** A(31:0) <> D(31:0) <> P1 **WARNING:** Pin numbers are backwards \_IPL(2:0) 🗁 FC(2:0) \_ IPEND \_RST 🗁 \_ECS \*\*• SIZE\_1 SIZE\_0 \_\_\_DS \_AS 🗁 \_\_\_BEER $R_W \triangleright$ \_\_\_AVEC \_STERM \*\* \_DSACK\_1 🗁 \_\_\_\_DSACK\_0 CPUCLK\_A □ **0**101 \_\_RMC \_CIIN \* **•**107 ⊸ \_CIOUT \_CBREQ \*\*• --≪ \_CBACK \_CPU\_BR 🗁 \_\_\_\_EXP\_BG \_CPU\_BG < \_\_\_\_EXP\_BR CPU BGACK **™**• ⊸ \_EXP\_BGACK **•**115 RESET PUNT 🗀 **•**117 \_\_INT6 INT2 \_\_\_\_KB\_DATA \_KB\_CL0CK 🗁 FIRE0 \_\_\_\_FIRE1 \_LED < \_\_\_\_ACTIVE **•**125 TxD RxD 🗀 \_\_\_\_DKWD \_DKRD 🗁 **0**129 SYSTEM -DKWE **9**131 \_CONFIG\_OUT \_\_\_\_CONFIG\_IN **•**133 **0**135 \_\_\_\_EXT\_AUDIO DA\_DATA **•**141 DA\_BCLK DA\_LRCLK **•**143 0144 **0**145 0146 DR < –**D**G DB < \_\_ —DI PIXELSW PIXELCLK \_PIXELSW\_EXT< **•**151 \_BLANK \_> **0**153 **0**155 -⇔CCK B \_CSYNC <--**9**157 **0**150 —<>\_VSYNC \_HSYNC 🗁 **•**159 AR\_EXT > –<mark>□></mark>AR AG\_EXT □ –**□**>AG **•**165 AB\_EXT –**⊳**AB **G**168 €167 \_\_\_XCLKEN \_NTSC < **0**171 0172 \_\_\_\_EXT\_VIDEO XCLK \_\_\_ **•**173 <del>0178</del> **•**177 LEFT EXT LEFT **•**179 RIGHT\_EXT RIGHT •181 •<del>182</del> | CATABLE / GPS | SET | CD/GS PLAYER PCB C.A.D. Generated manual changes may be made to this

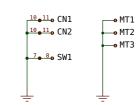
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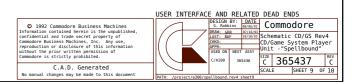




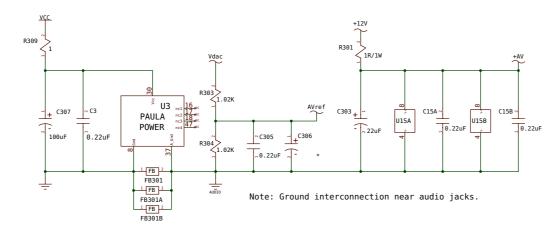


#### HOLES &c.

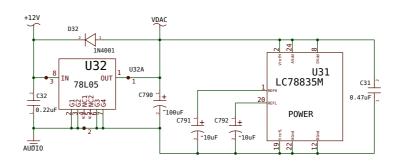




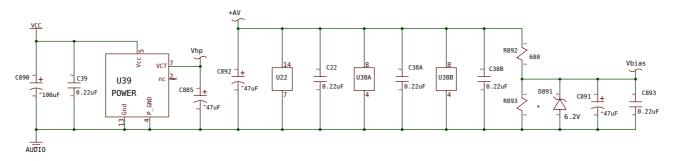
#### PAULA/AUDIO DECOUPLING



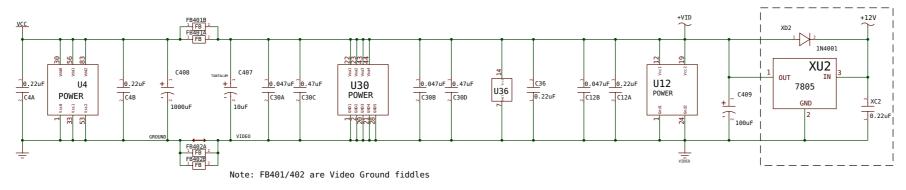
### CD/AUDIO DAC DECOUPLING



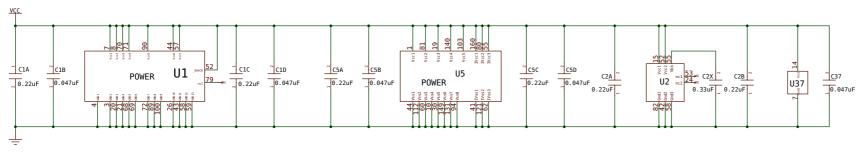
#### HEADPHONE/AUDIO DECOUPLING



#### VIDEO DECOUPLING



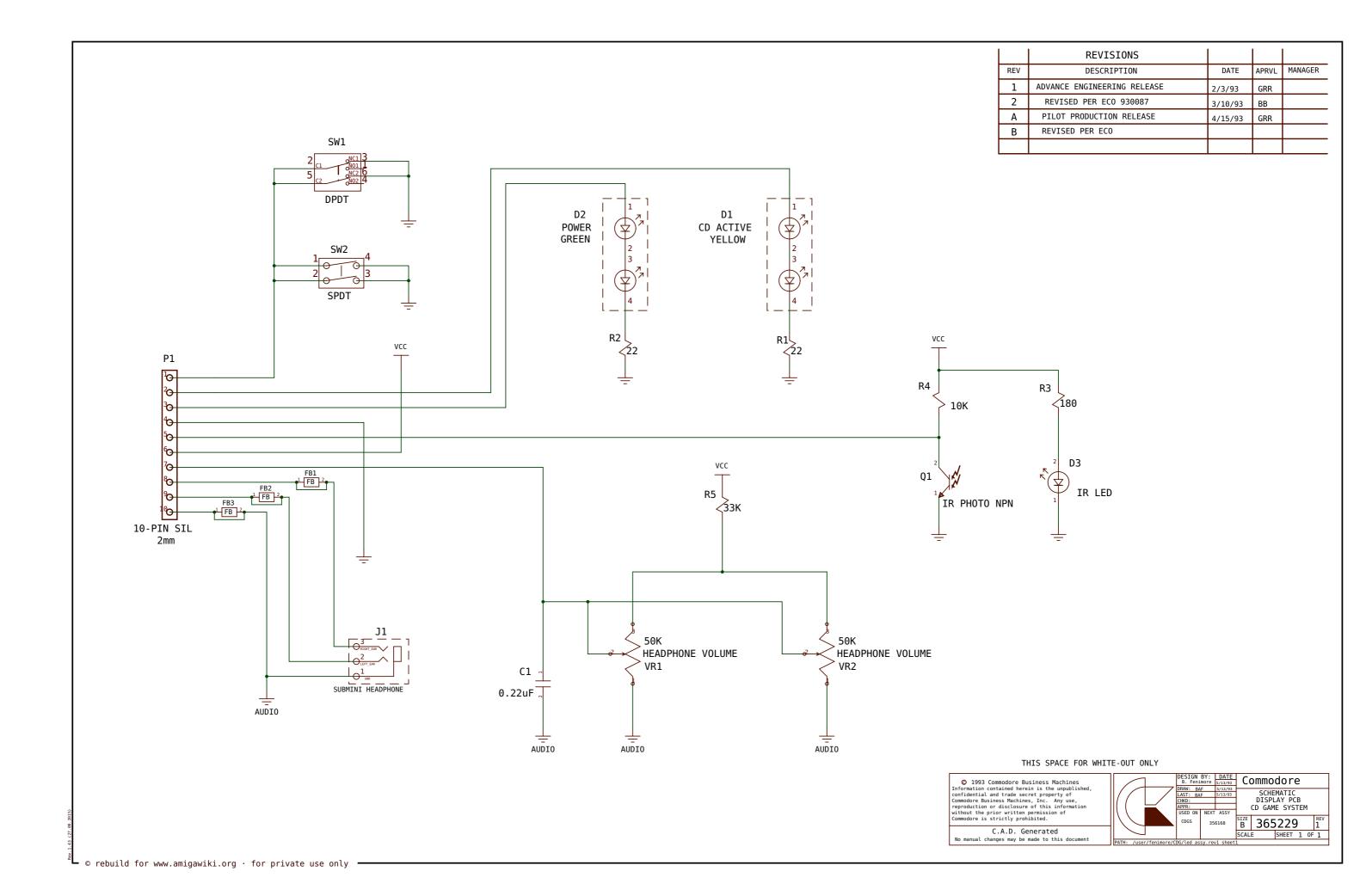
#### PROCESSOR/AKIKO/ALICE DECOUPLING

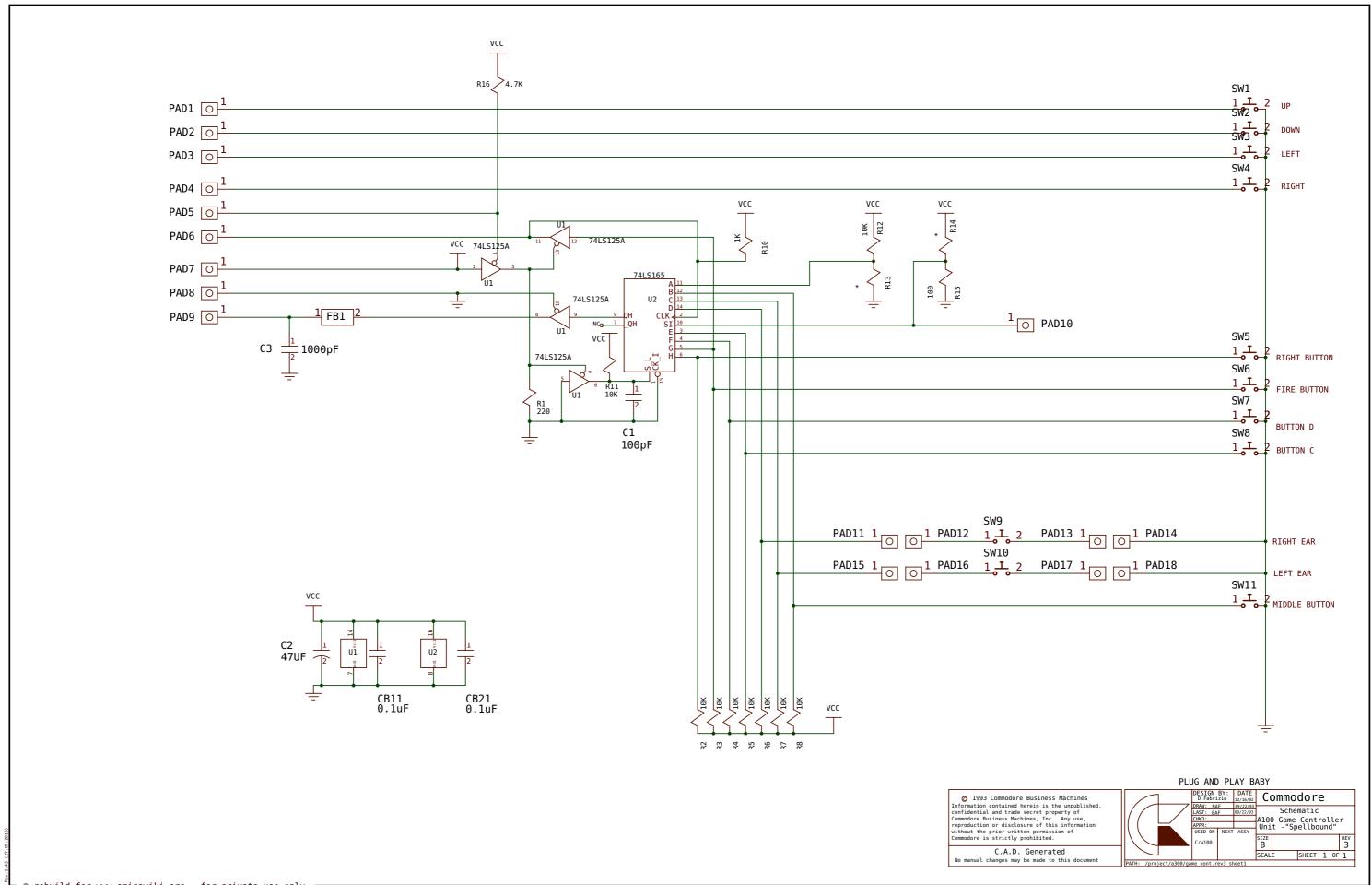


CD/GS PLAYER PCB

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