Amiga

A1200_R2

Rev.1.38 (06.09.2012)

Revision History

REV	DESCRIPTION	DATE	APRVL	MANAGER
0	Engineering Prototype	03/13/92	GRR	
1	Advance Engineering Release	06/29/92	GRR	
A	Production Release			

Jumpers and Stuff

REF	TYPE	DESCRIPTION	PAGE
R246	SMT	NTSC Color Burst	4
R202	SMT	PAL Color Burst	4
R625	SMT	Keyboard MPU Clock	9
R624	SMT	Keyboard/System Reset	9

Connectors

REF	TYPE	DESCRIPTION	PAGE
CN1	DB9P	Mouse/Joystick 1	5
CN2	DB9P	Mouse/Joystick 2	5
CN3	RCA-J	Right Audio Output	5
CN4	RCA-J	Left Audio Output	5
CN5	DB23S	External Floppy	8
CN6	DB25P	RS232 Serial Port	7
CN7	DB25S	Parallel Printer Port	7
CN8	SQ DIN	Power Supply Connector	13
CN9	DB23P	Video Output	6
CN10	RCA-J	Composite Video	4
CN11	DIL-34	Internal Floppy Signal	8
CN12	SIL-4	Internal Floppy Power	8
CN13	MEM-30	Keyboard Membrane	9
CN14	SIL-4	Internal Floppy Power	8
CN13	MEM-30	Keyboard Membrane	9
CN14	SIL-4	Keyboard Status LED's	9
CN15	PCMCIA	PC"Memory Card"	11
P9	EDGE-80	Memory Bus Expansion	12

Signal Glossary

SIGNAL	DESCRIPTION (AREA)	PAGES
28MHZ	28.63636 MHz Master Clock	
7MHZ	7.15909 MHz Processor Clock	
A[23:1]	Processor Address Bus (68000)	
ACK	Data Acknowledge (Parallel Port)	
AS	Address Strobe (68000)	
AUDIN	Audio Input (RS232 Port)	
AUDOUT	Audio Output (RS232 Jack)	
BEER	Bus Error (68000)	
BG	Bus Grant (68000)	
BGACK	Bus Grant Acknowledge (68000)	
BLISS	Blitter Slowdown (Chips)	
BLIT	Chip Memory Access (Chips)	
BR	Bus Request (68000)	
BUSY	Device Busy (Parallel Port)	
CASL/U	Column Address Strobe (DRAM)	
CCK/CCKQ	Color Clock / Quadrature (Chips)	
CDAC	7.15909 MHz Quadrature Clock (Chips)	
CHNG	Media Change (Floppy)	
CLKRD/WR	Read-Time Clock Read / Write (RTC)	
COMP	Monochrome Composite Video (Video)	
CSYNC	Composite Sync (Video)	
CTS	Clear to Send (RS232 Port)	
D[15:0]	Processor Data Bus (68000)	
DIR	Step Direction (Floppy)	
DKRD	Disk Read Data (Floppy)	
DKWD	Disk Write Data (Floppy)	
DKWE	Disk Write Enable (Floppy)	
DMAL	Chip DMA Request Line (Chips)	
DRA[8:0]	DRAM Address Bus (DRAM)	
DRD[15:0]	DRAM Data Bus (DRAM)	
DSR	Data Set Ready (RS232 Port)	
DTACK	Data Transfer Acknowledge (68000)	
DTR	Data Terminal Ready (RS232 Port)	
E	Peripheral Enable Clock (68000)	
EXTICK	Expansion Present / RTC Tick	
FC[2:0]	Function Code (68000)	
FIRE0/1	Fire Button 0/1 (Joysticks)	
HLT	Processor Halt (68000)	
HSYNC	Horizontal Sync (Video)	
INDEX	Index Pulse (Floppy)	
INT[2,3,6]	Interrupt Request (Chips)	
IORESET	I/O Reset	
IPL[2:0]	Interrupt Priority Level (68000)	
KBCLOCK	Keyboard Clock (Keyboard)	
KBDATA	Keyboard Data (Keyboard)	
KBRESET	Keyboard Reset (Keyboard)	
LDS/UDS	Upper / Lower Data Strobes (68000)	
LED	Power On LED / Audio Filter Disable	
LEFT/RIGHT	Left Right Audio (Audio)	
LPEN	Light Pen Trigger (Joysticks)	
MTR	Motor On (Floppy)	
MTR0	Motor On - Drive 0 (Floppy)	
M0V/M0H	Mouse 0 Quadrature V/H (Joysticks)	
M1V/M1H	Mouse 1 Quadrature V/H (Joysticks)	
OVL	Overlay ROM over RAM	
OVR	Override System Decoding	
PIXELSW	Genlock Pixel Switch (Video)	
POT0X/0Y	Pot Lines 0 X/Y (Joysticks)	
POT1X/1Y	Pot Lines 1 X/Y (Joysticks)	
POUT	Paper Out (Parallel Port)	
PPD[7:0]	Parallel Port Data (Parallel Port)	
RAMEN	RAM Enable (Chips)	
REGEN	Chip Register Enable (Chips)	
RAS0/1	Row Address Strobe (DRAM)	
RDY	Drive Ready (Floppy)	
RESET	General Reset	
RGA[8:1]	Register Address Bus (Chips)	
R/G/B	Red / Green / Blue (Video)	
RI	Ring Indicate (RS232 Port)	
ROMEN	ROM Enable (ROM)	
RTS	Request to Send (RS232 Port)	
RST	Processor Reset (68000)	
RXD	Receive Data (RS232 Port)	
RW	Processor Read/Write (68000)	
SEL	Select (Parallel Port)	
SEL[3:0]	Drive Select (Floppy)	
SIDE	Side Select (Floppy)	
STEP	Step In/Out Command (Floppy)	
TRK0	Track Zero Sense (Floppy)	
TXD	Transmit Data (RS232 Port)	
VMA	Valid Memory Address (68000)	
VPA	Valid Peripheral Address (68000)	
VSYNC	Vertical Sync (Video)	
WE	Write Enable (DRAM)	
WPROT	Write Protect Sense (Floppy)	
XCLK	External Genlock Clock (Video)	
XCLKEN	External Clock Enable (Video)	
XRDY	External Data Ready	
	** Credit Card and IDE Stuff? **	

Key Components

REF	CHIP	DESCRIPTION	PAGE
U1	68EC020	68EC020 uP/16MHz	2
U2	8374	Alice (AA Agnus)	2
U3	8364	Paula	5
U4	4203	Lisa (AA Denise)	4
U5	f0022x	AA Gayle (CBM ASIC)	2,8,11
U6A-B	asst	ROM 512Kx16, 150 nS	10
U7-8	8520	Amiga VIA, 1 MHz	7
U10-11	28F400	4Mbit FLASH Memory	10
U12	CXA1145	Sony Video Encoder	4
U13	6570-36	Amiga Keyboard MPU	9
U14	NE555	Reset Timer	9
U15	LF347	BiMOS Op-Amp	5
	TL084	BiCMOS Op-Amp	alt
U16-17	Asst	DRAM 512Kx8, 80nS	3
U18-19	Asst	DRAM 512Kx8, optional	3
U20	391???	Bridgette (NCR ASIC)	2
U28	1488	EIA Line Driver	7
U29	1489	EIA Line Receiver	7
U30	BT101	Triple 8-bit Video DAC	4
X1	OSC	TTL 28.63636 MHz NTSC	2
	OSC	TTL 28.37512 MHz PAL	alt
Y451	XTAL	4.433619MHz PAL Burst	4
Y621	XTAL	3MHz Ceramic Resonator	9
X2	UD3626	PAL Video Modulator	4
	VA3424	NTSC Video Modulator	4

A1200 Rev 2 PCB

DIRECTIONS AND REVISION HISTORY

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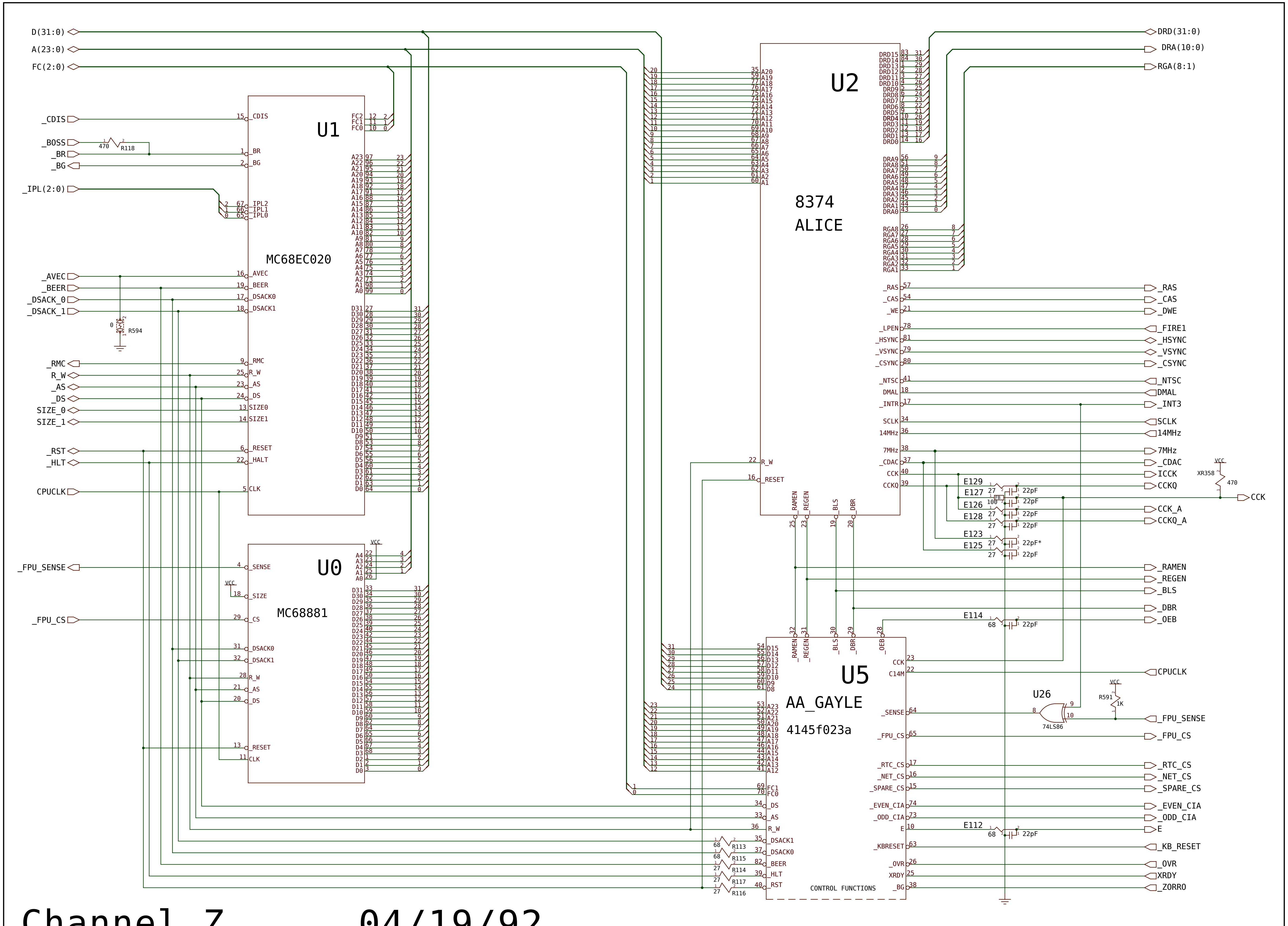
DESIGN BY: G. Robbins	DATE 03/13/92	Commodore	
DRAW: GRR	03/13/92	Schematic A1200 R2 C/A1200 Main Board "Channel Z"	
LAST: BAF	01/11/93		
CHKD:			
APPR:			
USED ON C/A1200	NEXT ASSY 365132	SIZE C	365133 REV A
		SCALE	SHEET 1 OF 13

PATH: /project/a300/channel_z.rev2 sheet1

Rev.1.38 (06.09.2012)


D(31:0)
A(23:0)
FC(2:0)
_CDIS
_BOSS
_BR
_BG
_IPL(2:0)
470
R118
_AVEC
_BEER
_DSACK_0
_DSACK_1
0
R594
_RMC
R_W
_AS
_DS
SIZE_0
SIZE_1
_RST
_HLT
CPUCLK
_FPU_SENSE
_FPU_CS
U1
MC68EC020
_CDIS
_BR
_BG
IPL2
IPL1
IPL0
_AVEC
_BEER
_DSACK0
_DSACK1
_RMC
R_W
_AS
_DS
SIZE0
SIZE1
_RESET
_HALT
CLK
FC2
FC1
FC0
U0
MC68881
VCC
_SENSE
_SIZE
_CS
_DSACK0
_DSACK1
R_W
_AS
_DS
_RESET
CLK
U2
8374
ALICE
R_W
_RESET
_RAMEN
_REGEN
_BLS
_DBR
_RAS
_CAS
_WE
_LPEN
_HSYNC
_VSYNC
_CSYNC
_NTSC
DMAL
_INTR
SCLK
14MHz
7MHz
_CDAC
CCK
CCKQ
DRD(31:0)
DRA(10:0)
RGA(8:1)
_RAS
_CAS
_DWE
_FIRE1
_HSYNC
_VSYNC
_CSYNC
_NTSC
DMAL
_INT3
SCLK
14MHz
7MHz
_CDAC
ICCK
CCKQ
VCC
XR358
470
CCK
E129
E127
E126
E128
E123
E125
22pF
22pF*
CCK_A
CCKQ_A
_RAMEN
_REGEN
_BLS
_DBR
_OEB
E114
68
U5
AA_GAYLE
4145f023a
CCK
C14M
_SENSE
_FPU_CS
_RTC_CS
_NET_CS
_SPARE_CS
_EVEN_CIA
_ODD_CIA
E
_KBRESET
_OVR
XRDY
_BG
FC1
FC0
_DS
_AS
R_W
_DSACK1
_DSACK0
_BEER
HLT
RST
CONTROL FUNCTIONS
R113
R115
R114
R117
R116
E112
U26
74LS86
VCC
R591
1K
CPUCLK
_FPU_SENSE
_FPU_CS
_RTC_CS
_NET_CS
_SPARE_CS
_EVEN_CIA
_ODD_CIA
E
_KB_RESET
_OVR
XRDY
_ZORRO

Channel Z

04/19/92

A1200 Rev 2 PCB

Note: Various components are for EMI Control
and may be loaded with funny things...

PROCESSOR AND OTHER USEFUL COMPONENTS

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DESIGN BY:	DATE
G. Robbins	03/13/92
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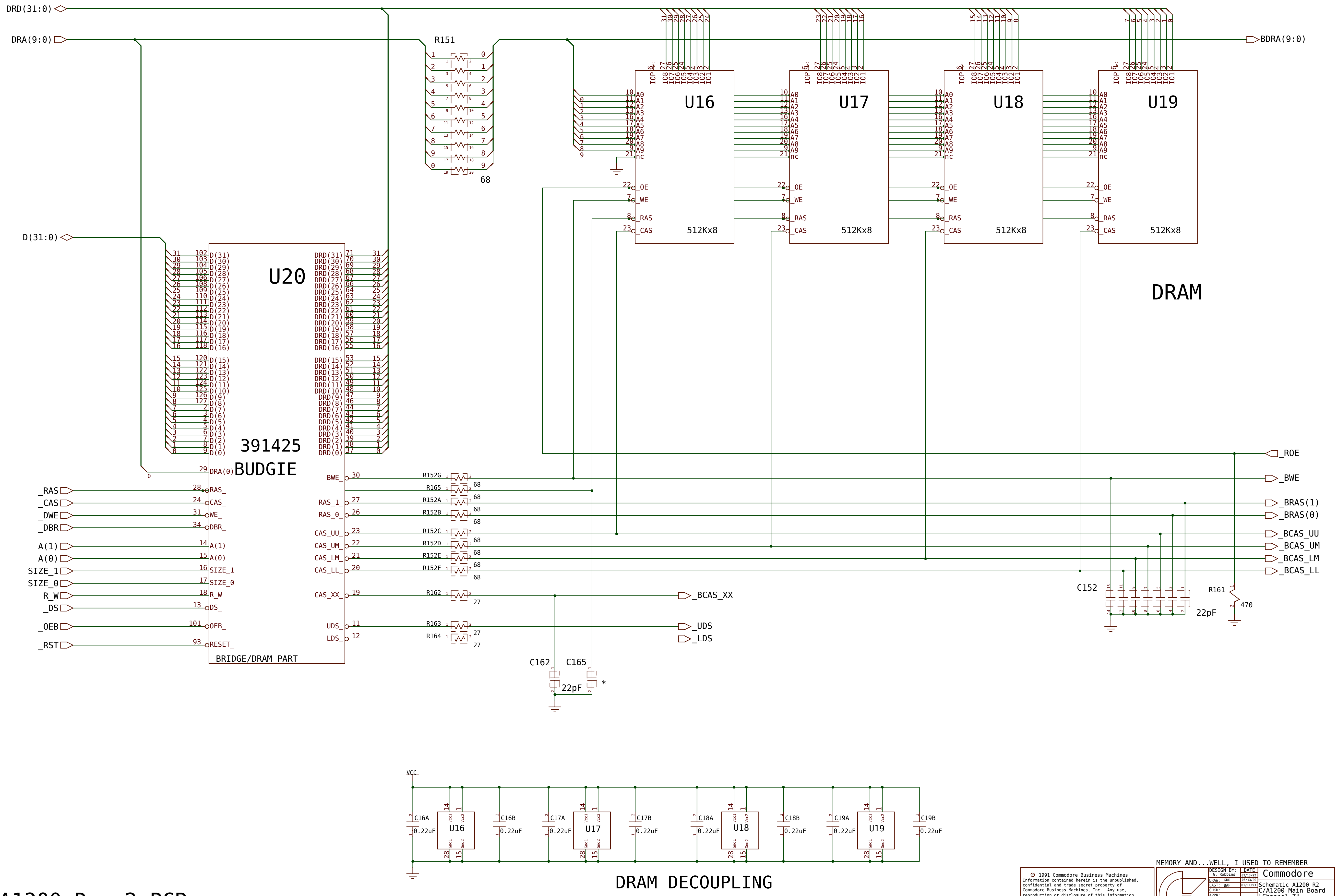
APPR:	

USED ON: C/A1200
NEXT ASSY: 365132

Commodore
Schematic A1200 R2
C/A1200 Main Board
"Channel Z"

SIZE C
365133
REV A
SCALE
SHEET 2 OF 13
PATH: /project/a300/channel_z.rev2 sheet2


DRD(31:0)
DRA(9:0)
D(31:0)
BDRA(9:0)
R151
68
U16
U17
U18
U19
512Kx8
DRAM
U20
391425
BUDGIE
BRIDGE/DRAM PART
_RAS
_CAS
_DWE
_DBR
A(1)
A(0)
SIZE_1
SIZE_0
R_W
_DS
_OEB
_RST
BWE_
RAS_1
RAS_0
CAS_UU
CAS_UM
CAS_LM
CAS_LL
CAS_XX
UDS_
LDS_
R152G
R165
R152A
R152B
R152C
R152D
R152E
R152F
R162
R163
R164
27
_ROE
_BWE
_BRAS(1)
_BRAS(0)
_BCAS_UU
_BCAS_UM
_BCAS_LM
_BCAS_LL
_BCAS_XX
_UDS
_LDS
C152
22pF
R161
470
C162
C165
*
VCC
C16A
C16B
C17A
C17B
C18A
C18B
C19A
C19B
0.22uF
DRAM DECOUPLING

MEMORY AND...WELL, I USED TO REMEMBER

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DESIGN BY:	DATE
G. Robbins	03/13/92
DRAW: GRR	03/13/92
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CHKD:	
APPR:	

USED ON	NEXT ASSY
C/A1200	365132

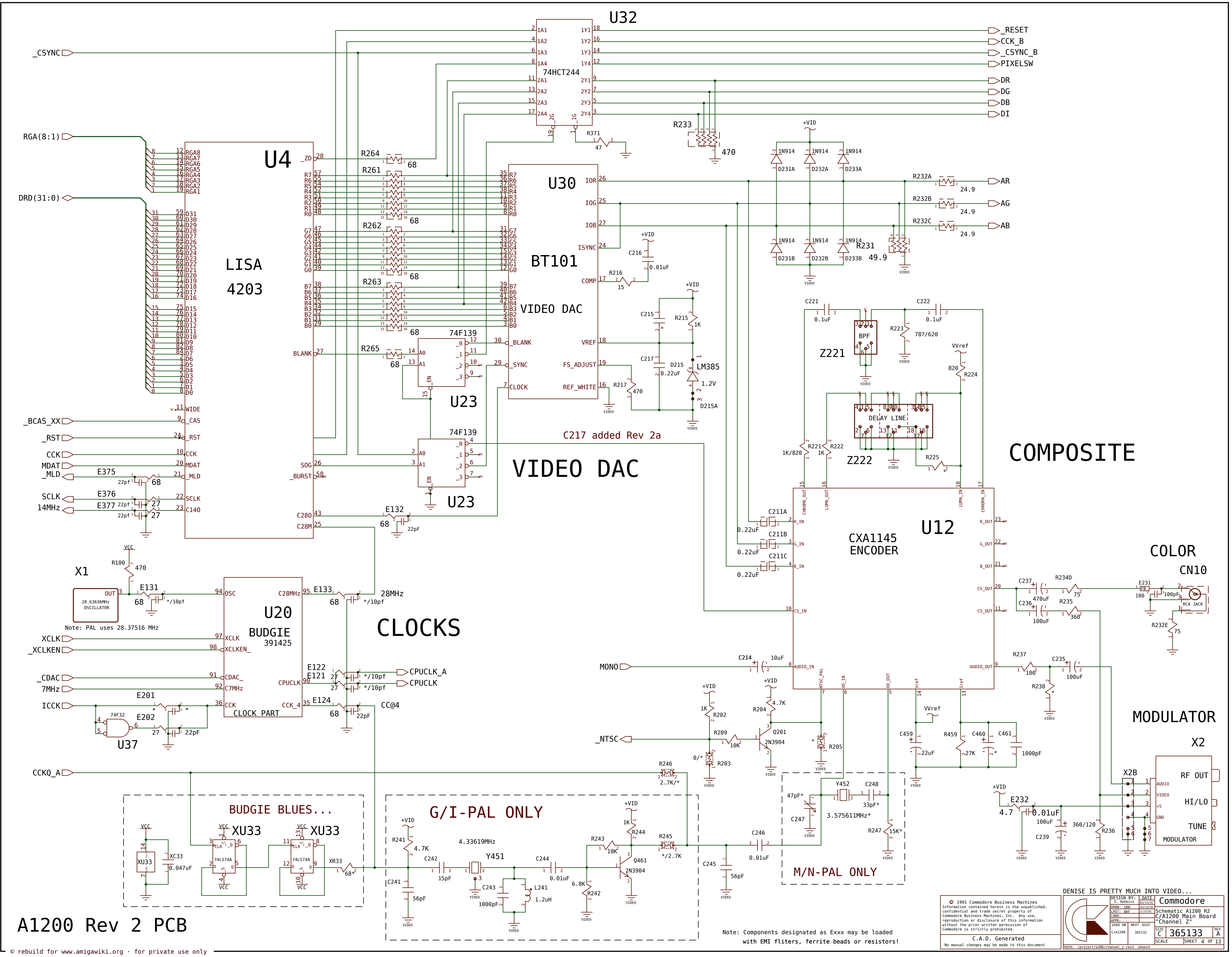
Commodore
Schematic A1200 R2
C/A1200 Main Board
"Channel Z"

SIZE C
365133
REV A
SCALE
SHEET 3 OF 13

PATH: /project/a300/channel_z.rev2 sheet3

A1200 Rev 2 PCB

Rev.1.38 (06.09.2012)


U32
74HCT244
_RESET
CCK_B
_CSYNC_B
PIXELSW
DR
DG
DB
DI
_CSYNC
RGA(8:1)
DRD(31:0)
U4
LISA
4203
_ZD
BLANK
SOG
_BURST
C280
C28M
_BCAS_XX
_RST
CCK
MDAT
_MLD
SCLK
14MHz
E375
E376
E377
R264
R261
R262
R263
R265
R371
R233
470
U30
BT101
VIDEO DAC
IOR
IOG
IOB
ISYNC
COMP
VREF
FS_ADJUST
REF_WHITE
_BLANK
_SYNC
CLOCK
74F139
U23
LM385
1.2V
D215A
C217 added Rev 2a
1N914
D231A
D232A
D233A
D231B
D232B
D233B
R232A
R232B
R232C
24.9
R231
49.9
AR
AG
AB
+VID
VIDEO
BPF
Z221
DELAY LINE
Z222
COMPOSITE
U12
CXA1145
ENCODER
R_IN
G_IN
B_IN
CS_IN
CV_OUT
CS_OUT
AUDIO_IN
AUDIO_OUT
NTSC_PAL
XO_IN
XO_OUT
VVref
COLOR
CN10
RCA JACK
MODULATOR
X2
X2B
RF OUT
HI/LO
TUNE
MONO
_NTSC
Q201
2N3904
X1
28.63636MHz OSCILLATOR
Note: PAL uses 28.37516 MHz
VCC
R100
E131
U20
BUDGIE
391425
CLOCK PART
OSC
C28MHz
XCLK
XCLKEN_
_CDAC
7MHz
ICCK
CPUCLK
CCK_4
E133
28MHz
CLOCKS
E122
E121
CPUCLK_A
E124
CC@4
E201
E202
74F32
U37
CCKQ_A
BUDGIE BLUES...
XU33
74LS74A
XC33
0.047uF
XR33
G/I-PAL ONLY
4.33619MHz
Y451
L241
1.2uH
Q461
M/N-PAL ONLY
Y452
3.575611MHz*
A1200 Rev 2 PCB
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Note: Components designated as Exxx may be loaded with EMI fliters, ferrite beads or resistors!

DENISE IS PRETTY MUCH INTO VIDEO...

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DESIGN BY: G. Robbins	DATE 03/13/92
DRAW: GRR	03/13/92
LAST: BAF	2/23/93
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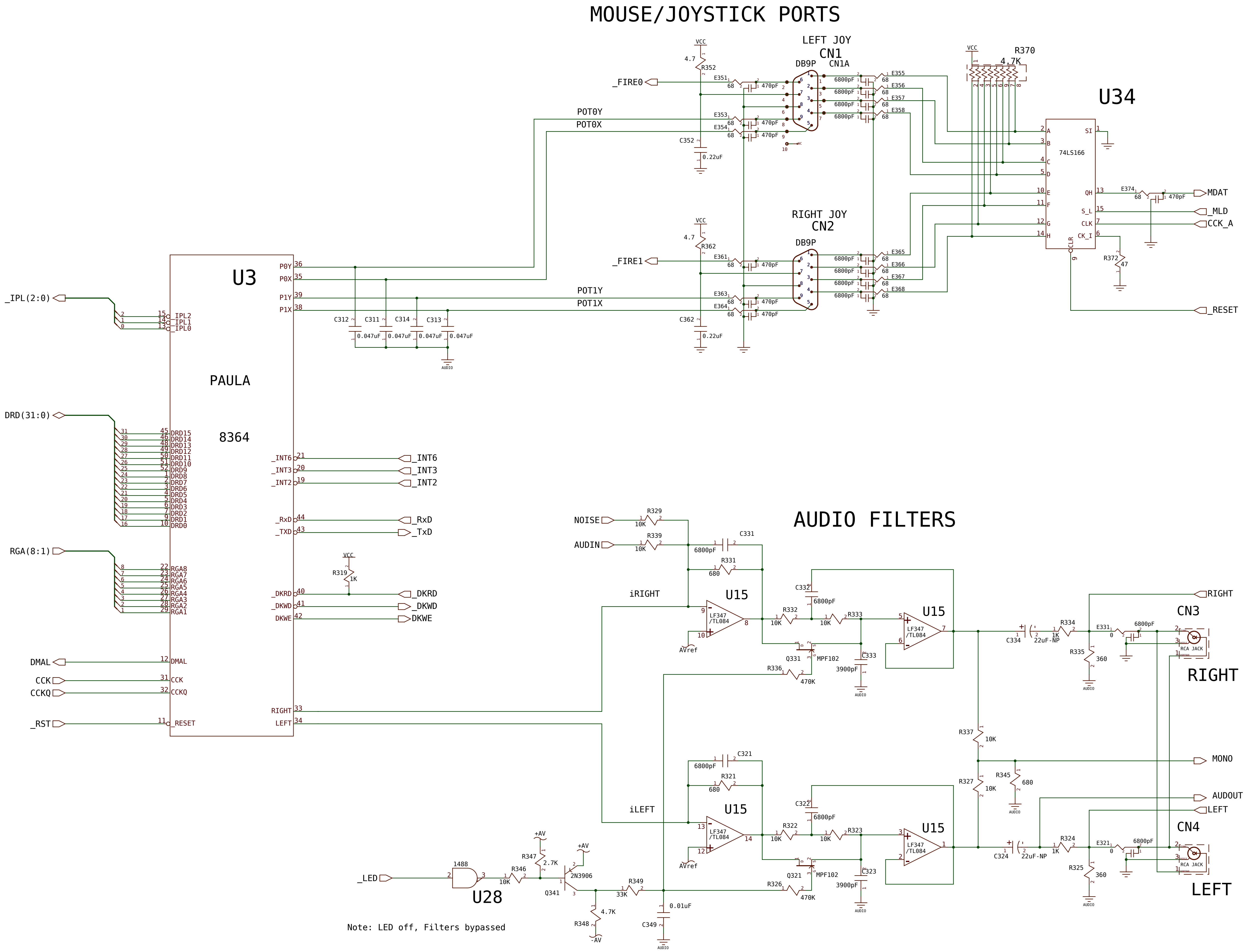
APPR:	

USED ON: C/A1200
NEXT ASSY: 365132

Commodore
Schematic A1200 R2
C/A1200 Main Board
"Channel Z"
SIZE C 365133 REV A
SCALE SHEET 4 OF 13
PATH: /project/a300/channel_z.rev2 sheet4


MOUSE/JOYSTICK PORTS
LEFT JOY
CN1
CN1A
DB9P
RIGHT JOY
CN2
DB9P
_FIRE0
_FIRE1
POT0Y
POT0X
POT1Y
POT1X
VCC
4.7
R352
R362
E351
E353
E354
E361
E363
E364
68
470pF
C352
C362
0.22uF
E355
E356
E357
E358
E365
E366
E367
E368
6800pF
R370
4.7K
U34
74LS166
SI
QH
S_L
CLK
CK_I
CLR
E374
MDAT
_MLD
CCK_A
R372
47
_RESET
U3
PAULA
8364
P0Y
P0X
P1Y
P1X
C312
C311
C314
C313
0.047uF
AUDIO
_IPL(2:0)
IPL2
IPL1
IPL0
DRD(31:0)
DRD15
DRD14
DRD13
DRD12
DRD11
DRD10
DRD9
DRD8
DRD7
DRD6
DRD5
DRD4
DRD3
DRD2
DRD1
DRD0
RGA(8:1)
RGA8
RGA7
RGA6
RGA5
RGA4
RGA3
RGA2
RGA1
DMAL
CCK
CCKQ
_RST
_RESET
_INT6
_INT3
_INT2
_RxD
_TxD
_DKRD
_DKWD
DKWE
R319
1K
RIGHT
LEFT
AUDIO FILTERS
NOISE
AUDIN
R329
R339
10K
C331
6800pF
R331
680
iRIGHT
U15
LF347
/TL084
AVref
C332
R332
R333
Q331
MPF102
C333
3900pF
R336
470K
C334
22uF-NP
R334
1K
R335
360
E331
0
CN3
RCA JACK
RIGHT
R337
R327
10K
R345
680
MONO
AUDOUT
LEFT
C321
R321
iLEFT
C322
R322
R323
Q321
C323
R326
C324
R324
R325
E321
CN4
LEFT
_LED
1488
U28
R346
10K
+AV
R347
2.7K
2N3906
Q341
R349
33K
R348
4.7K
-AV
C349
0.01uF
Note: LED off, Filters bypassed

PAULA PREFERS THE TRADITIONAL MODES

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DESIGN BY:	DATE
G. Robbins	03/13/92
DRAW: GRR	03/13/92
LAST: BAF	01/11/93
CHKD:	
APPR:	

USED ON	NEXT ASSY
C/A1200	365132

Commodore

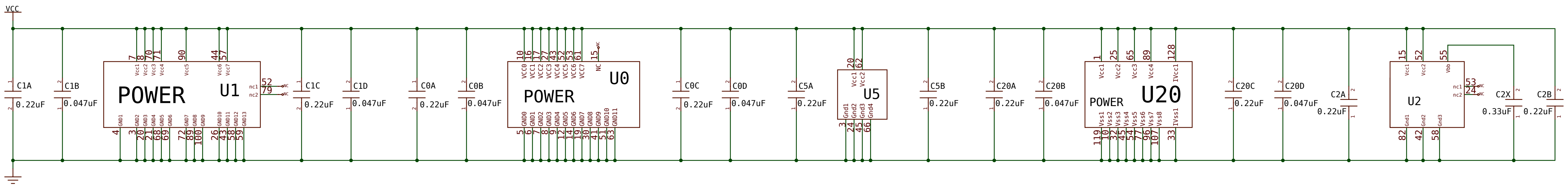
Schematic A1200 R2
C/A1200 Main Board
"Channel Z"

SIZE C 365133 REV A
SCALE SHEET 5 OF 13

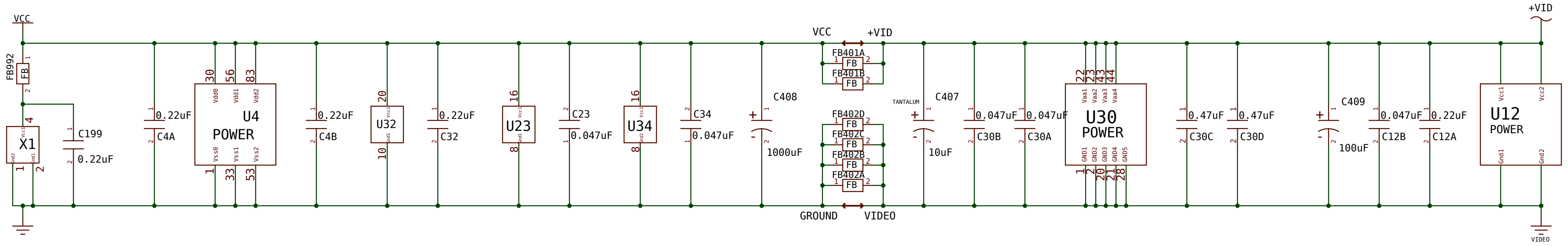
PATH: /project/a300/channel_z.rev2 sheet5

A1200 Rev 2 PCB

GENERAL DECOUPLING

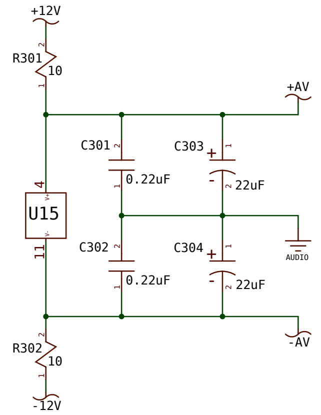

VCC
C1A
0.22uF
C1B
0.047uF
POWER
U1
C1C
0.22uF
C1D
0.047uF
C0A
0.22uF
C0B
0.047uF
POWER
U0
C0C
0.22uF
C0D
0.047uF
C5A
0.22uF
U5
C5B
0.22uF
C20A
0.22uF
C20B
0.047uF
POWER
U20
C20C
0.22uF
C20D
0.047uF
C2A
0.22uF
U2
C2X
0.33uF
C2B
0.22uF

VIDEO DECOUPLING

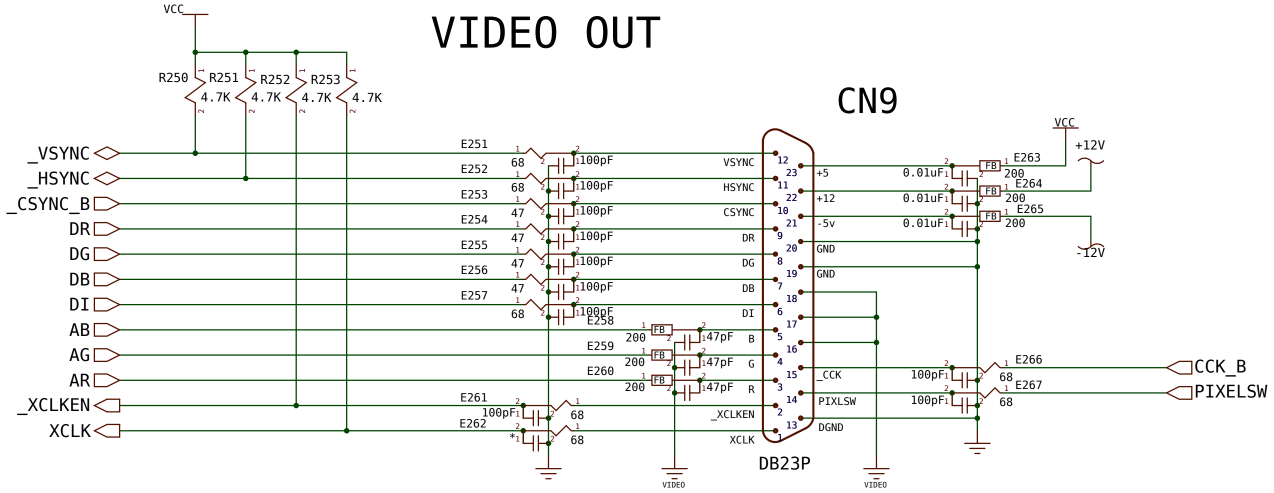

VCC
FB992
FB
X1
C199
0.22uF
0.22uF
C4A
U4
POWER
0.22uF
C4B
U32
0.22uF
C32
U23
C23
0.047uF
U34
C34
0.047uF
C408
1000uF
VCC
+VID
FB401A
FB401B
FB402D
FB402C
FB402B
FB402A
FB
GROUND
VIDEO
TANTALUM
C407
10uF
0.047uF
C30B
0.047uF
C30A
U30
POWER
0.47uF
C30C
0.47uF
C30D
C409
100uF
0.047uF
C12B
0.22uF
C12A
U12
POWER
+VID
VIDEO

Note: Common Ground at DAC

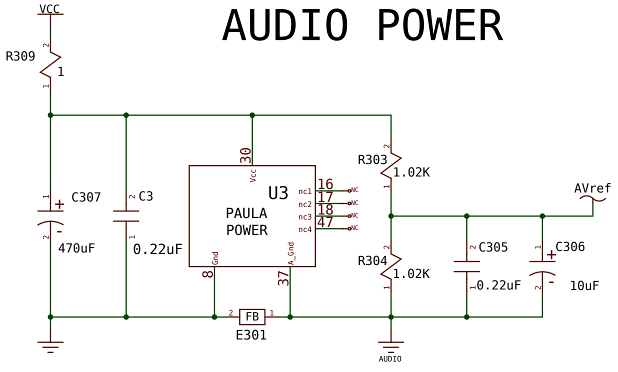
AUDIO DECOUPLING


+12V
R301
10
+AV
C301
0.22uF
C303
22uF
U15
C302
0.22uF
C304
22uF
AUDIO
R302
10
-AV
-12V

VIDEO OUT


VCC
R250
R251
4.7K
R252
4.7K
R253
4.7K
4.7K
_VSYNC
_HSYNC
_CSYNC_B
DR
DG
DB
DI
AB
AG
AR
_XCLKEN
XCLK
E251
E252
E253
E254
E255
E256
E257
68
68
47
47
47
47
68
100pF
E258
E259
E260
200
FB
47pF
E261
E262
100pF
68
68
CN9
VSYNC
HSYNC
CSYNC
DR
DG
DB
DI
B
G
R
_XCLKEN
XCLK
+5
+12
-5v
GND
GND
_CCK
PIXLSW
DGND
DB23P
VIDEO
VIDEO
VCC
+12V
0.01uF
E263
E264
E265
200
-12V
100pF
E266
E267
68
CCK_B
PIXELSW

AUDIO POWER


VCC
R309
1
C307
470uF
C3
0.22uF
U3
PAULA
POWER
E301
FB
R303
1.02K
R304
1.02K
AVref
C305
0.22uF
C306
10uF
AUDIO

Note: Common Ground near Jacks

A1200 Rev 2 PCB

PARTY OUT OF BOUNDS, WHAT A MESS...

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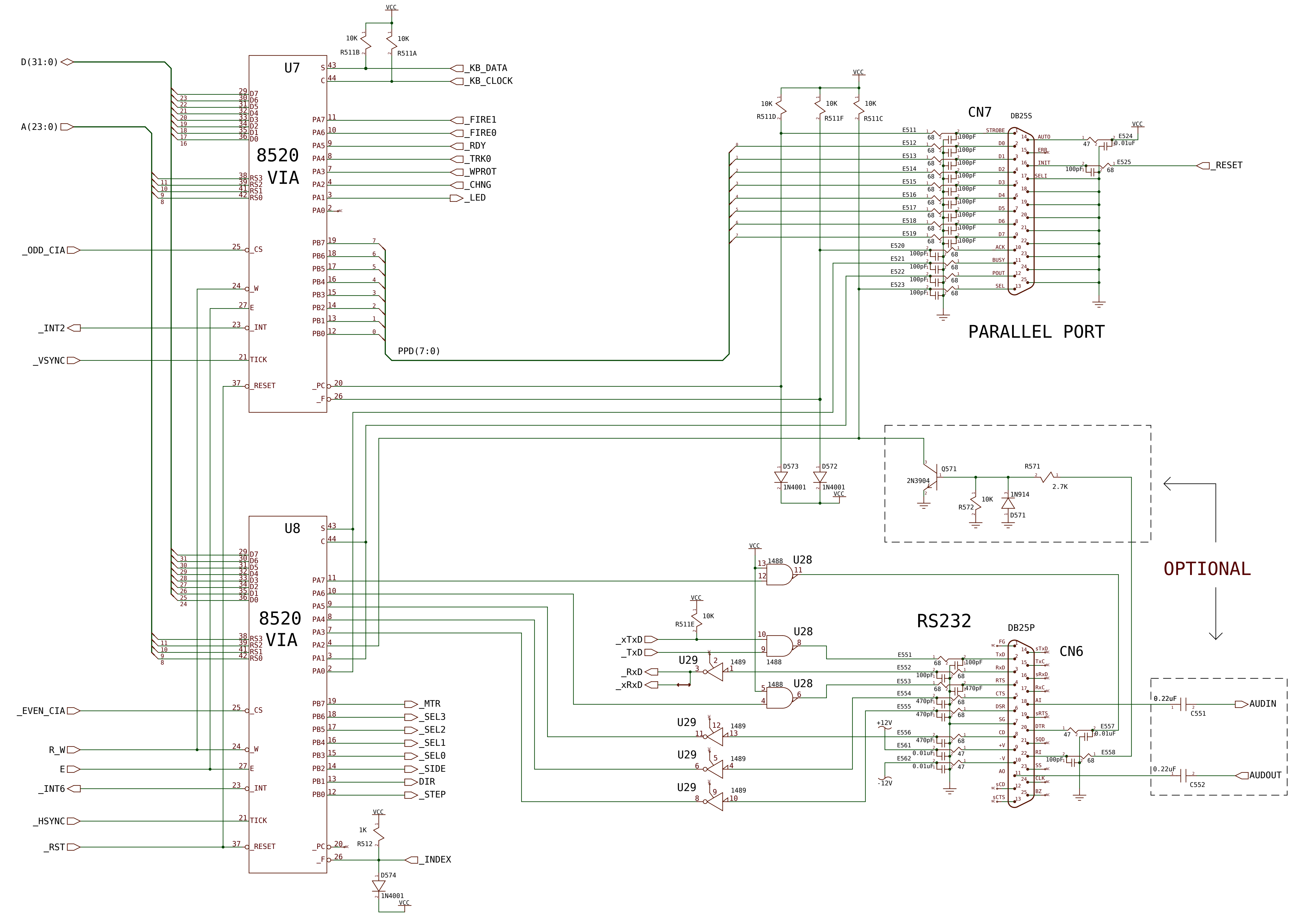
DESIGN BY: G. Robbins	DATE 03/13/92
DRAW: GRR	03/13/92
LAST: BAF	01/11/93
CHKD:	
APPR:	

USED ON	NEXT ASSY
C/A1200	365132

Commodore
Schematic A1200 R2
C/A1200 Main Board
"Channel Z"
SIZE C 365133 REV A
SCALE SHEET 6 OF 13
PATH: /project/a300/channel_z.rev2 sheet6

Rev.1.38 (06.09.2012)


D(31:0)
A(23:0)
U7
8520
VIA
_ODD_CIA
_INT2
_VSYNC
_KB_DATA
_KB_CLOCK
_FIRE1
_FIRE0
_RDY
_TRK0
_WPROT
_CHNG
_LED
PPD(7:0)
VCC
10K
R511B
R511A
R511D
R511F
R511C
CN7
DB25S
PARALLEL PORT
STROBE
ACK
BUSY
POUT
SEL
AUTO
ERR
INIT
SELI
E511
E512
E513
E514
E515
E516
E517
E518
E519
E520
E521
E522
E523
E524
E525
100pF
68
47
0.01uF
_RESET
D573
D572
1N4001
Q571
2N3904
R571
2.7K
R572
10K
1N914
D571
OPTIONAL
U8
_EVEN_CIA
R_W
E
_INT6
_HSYNC
_RST
_MTR
_SEL3
_SEL2
_SEL1
_SEL0
_SIDE
DIR
_STEP
_INDEX
R512
1K
D574
U28
1488
U29
1489
R511E
_xTxD
_TxD
_RxD
_xRxD
RS232
DB25P
CN6
FG
TxD
RxD
RTS
CTS
DSR
SG
CD
+V
-V
AO
sCD
sCTS
sTxD
TxC
sRxD
RxC
AI
sRTS
DTR
SQD
RI
SS
CLK
BZ
E551
E552
E553
E554
E555
E556
E561
E562
E557
E558
470pF
+12V
-12V
0.22uF
C551
C552
AUDIN
AUDOUT

SERIAL AND PARALLEL PORTS

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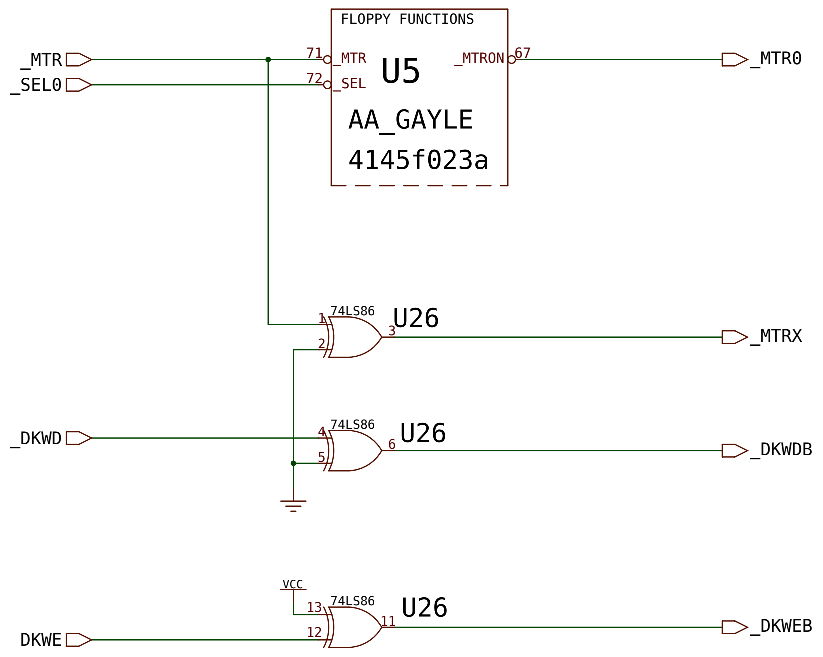
DESIGN BY:	DATE
G. Robbins	03/13/92
DRAW: GRR	03/13/92
LAST: BAF	01/11/93
CHKD:	
APPR:	

USED ON	NEXT ASSY
C/A1200	365132

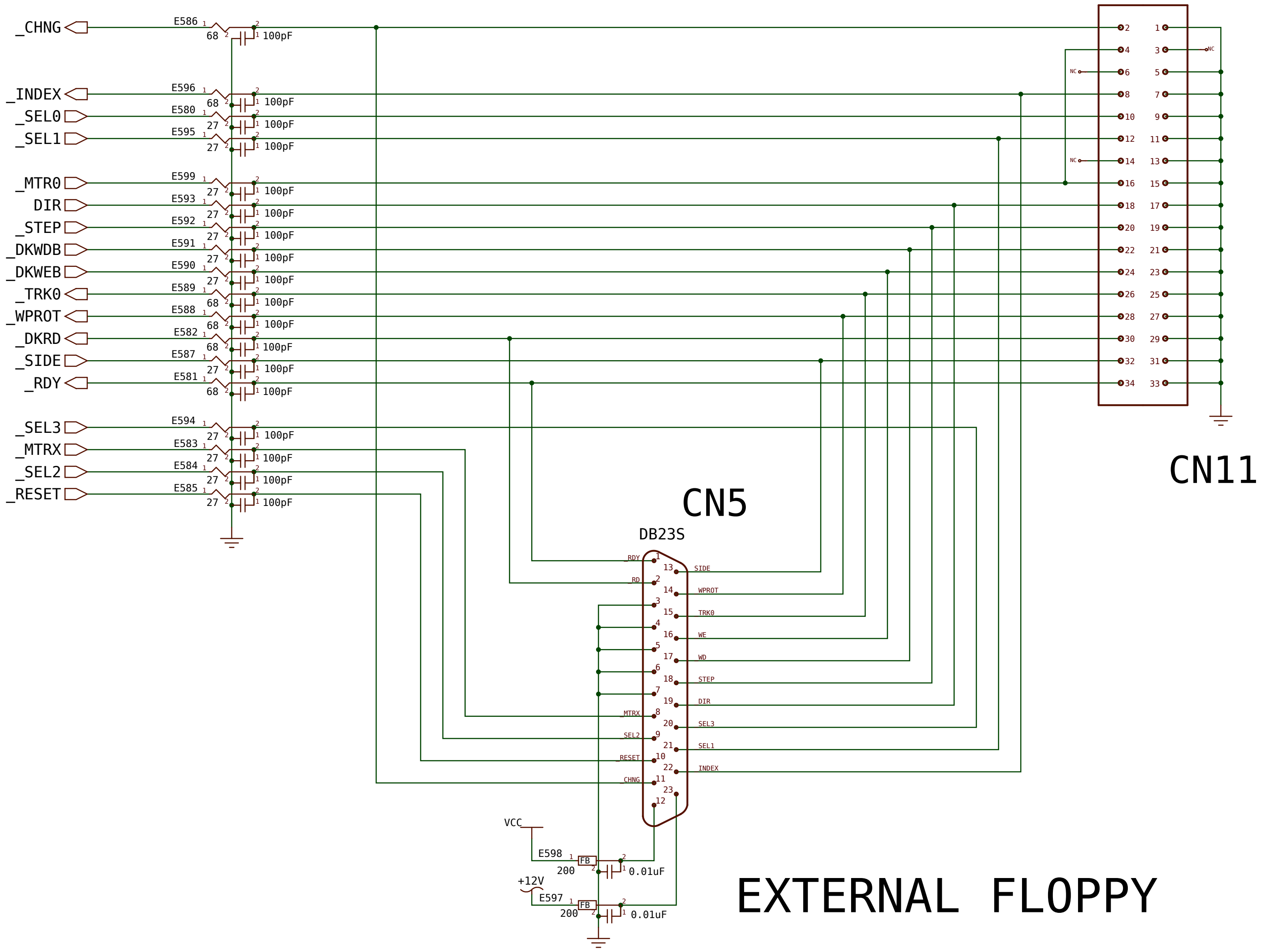
Commodore
Schematic A1200 R2
C/A1200 Main Board
"Channel Z"
SIZE C 365133 REV A
SCALE SHEET 7 OF 13
PATH: /project/a300/channel_z.rev2 sheet7

A1200 Rev 2 PCB

FLOPPY LOGIC

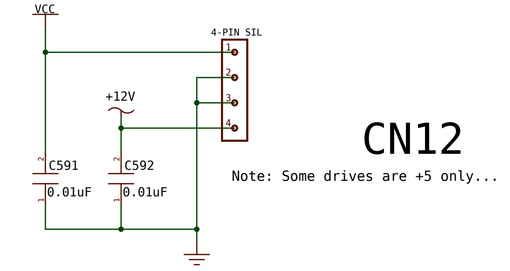

FLOPPY FUNCTIONS
U5
AA_GAYLE
4145f023a
_MTR
_SEL0
71 _MTR
72 _SEL
_MTRON 67
_MTR0
74LS86
U26
_MTRX
_DKWD
_DKWDB
VCC
DKWE
_DKWEB

INTERNAL FLOPPY

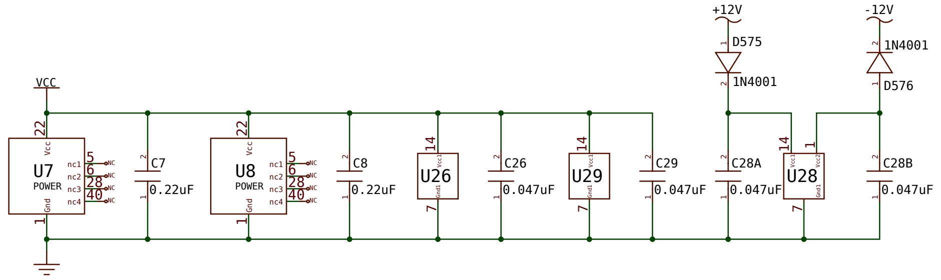

_CHNG
_INDEX
_SEL0
_SEL1
_MTR0
DIR
_STEP
_DKWDB
_DKWEB
_TRK0
_WPROT
_DKRD
_SIDE
_RDY
_SEL3
_MTRX
_SEL2
_RESET
E586 68
E596 68
E580 27
E595 27
E599 27
E593 27
E592 27
E591 27
E590 27
E589 68
E588 68
E582 68
E587 27
E581 68
E594 27
E583 27
E584 27
E585 27
100pF
CN11
CN5
DB23S
_RDY
_RD
_MTRX
_SEL2
_RESET
_CHNG
SIDE
_WPROT
_TRK0
_WE
_WD
_STEP
_DIR
_SEL3
_SEL1
_INDEX
VCC
E598
FB
200
0.01uF
+12V
E597
FB
200
0.01uF

EXTERNAL FLOPPY

FLOPPY POWER


VCC
4-PIN SIL
+12V
C591
0.01uF
C592
0.01uF
CN12

Note: Some drives are +5 only...


VCC
U7
POWER
22
1
U8
POWER
C7
0.22uF
C8
0.22uF
U26
C26
0.047uF
U29
C29
0.047uF
+12V
D575
1N4001
-12V
1N4001
D576
C28A
0.047uF
U28
C28B
0.047uF

DECOUPLING

A1200 Rev 2 PCB

Rev.1.38 (06.09.2012)

THE REST OF THE FLOPPY STUFF

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DESIGN BY:	DATE
G. Robbins	03/13/92
DRAW: GRR	03/13/92
LAST: BAF	01/11/93
CHKD:	
APPR:	

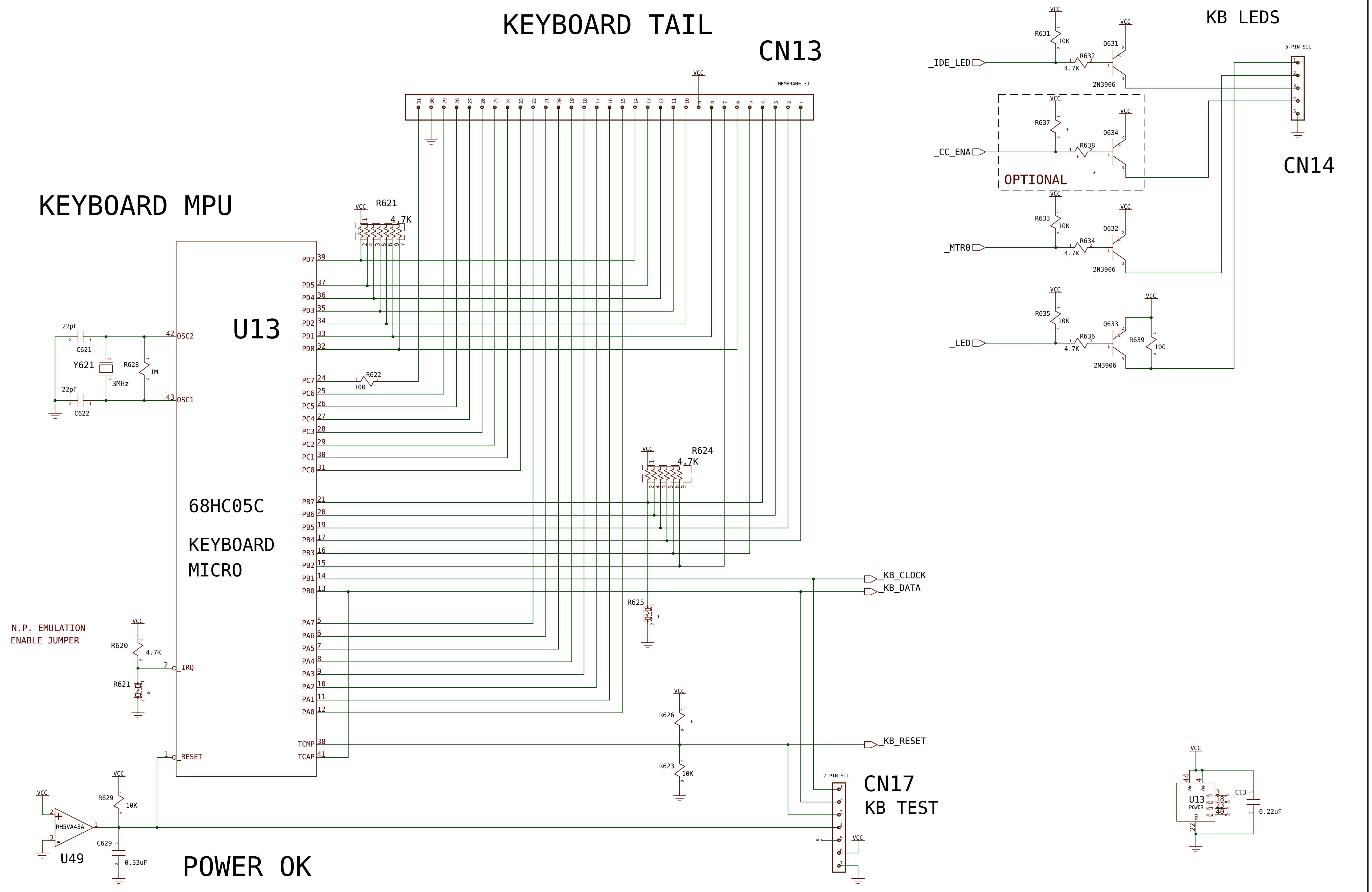
USED ON	NEXT ASSY
C/A1200	365132

Commodore

Schematic A1200 R2
C/A1200 Main Board
"Channel Z"

SIZE C
365133
REV A
SCALE
SHEET 8 OF 13

PATH: /project/a300/channel_z.rev2 sheet8


KEYBOARD TAIL
CN13
MEMBRANE-31
VCC
KEYBOARD MPU
U13
68HC05C
KEYBOARD
MICRO
OSC2 42
OSC1 43
PD7 39
PD5 37
PD4 36
PD3 35
PD2 34
PD1 33
PD0 32
PC7 24
PC6 25
PC5 26
PC4 27
PC3 28
PC2 29
PC1 30
PC0 31
PB7 21
PB6 20
PB5 19
PB4 17
PB3 16
PB2 15
PB1 14
PB0 13
PA7 5
PA6 6
PA5 7
PA4 8
PA3 9
PA2 10
PA1 11
PA0 12
_IRQ 2
_RESET 1
TCMP 38
TCAP 41
R621
4.7K
R622
100
R624
4.7K
R625
22pF
C621
22pF
C622
Y621
3MHz
R628
1M
N.P. EMULATION
ENABLE JUMPER
R620
4.7K
R621
_KB_CLOCK
_KB_DATA
_KB_RESET
R626
R623
10K
7-PIN SIL
CN17
KB TEST
RH5VA43A
U49
R629
10K
C629
0.33uF
POWER OK
KB LEDS
_IDE_LED
R631
10K
R632
4.7K
Q631
2N3906
_CC_ENA
R637
R638
Q634
OPTIONAL
_MTR0
R633
10K
R634
4.7K
Q632
2N3906
_LED
R635
10K
R636
4.7K
Q633
2N3906
R639
100
5-PIN SIL
CN14
U13
POWER
Vdd
Vpp
Vss
NC1
NC2
NC3
NC4
NC
C13
0.22uF
44
4
3
18
23
40
22

THE NEW HOME OF THE KEYBOARD VIRUS

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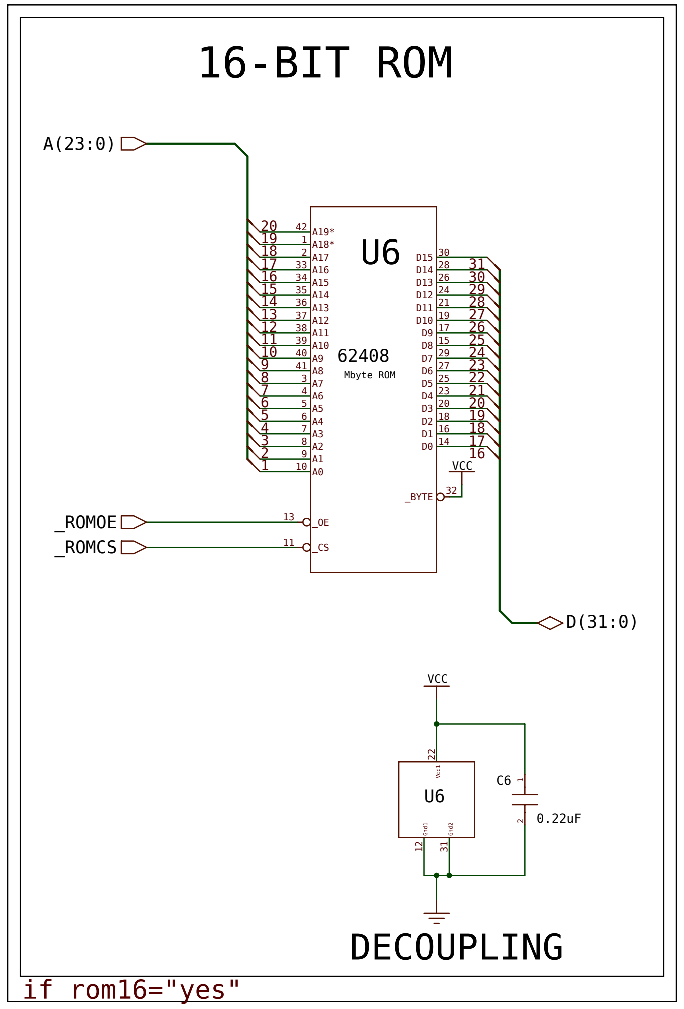
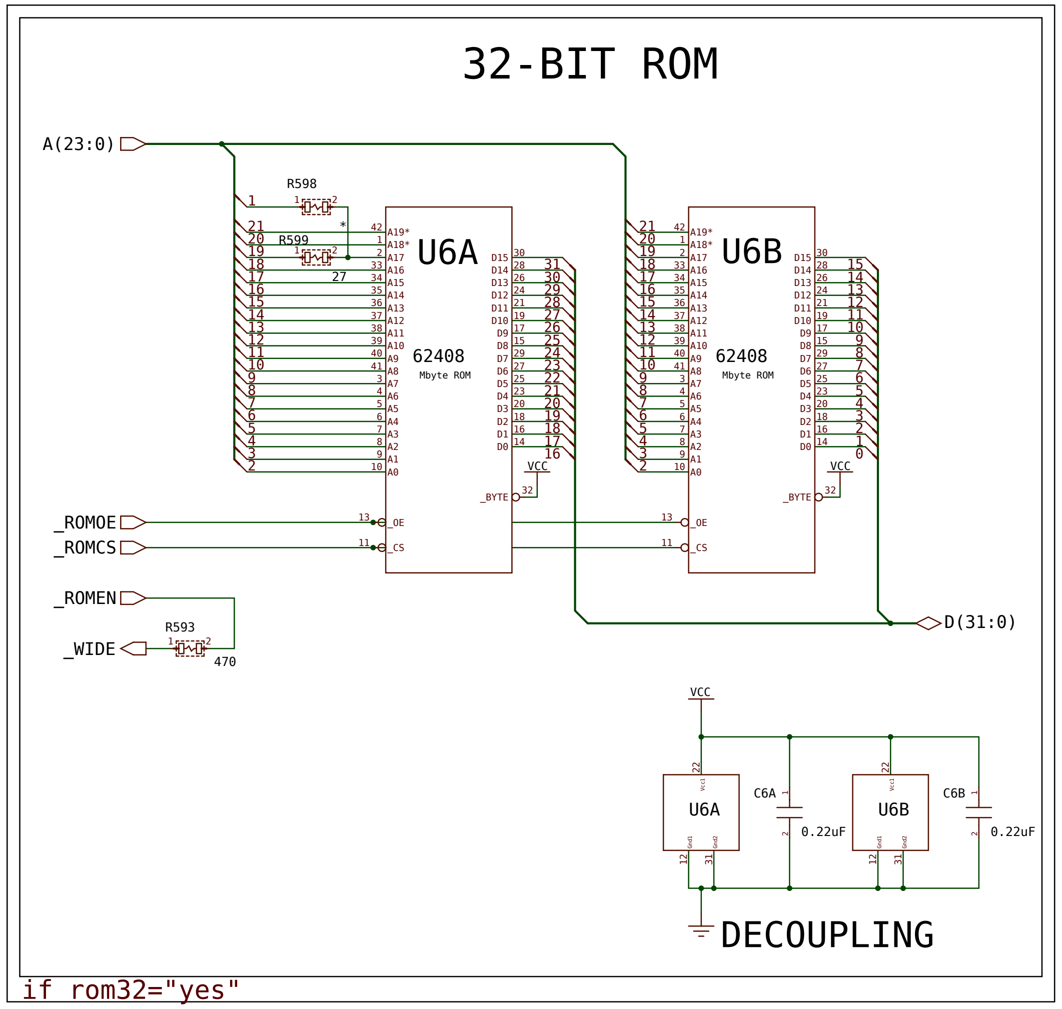
DESIGN BY: G. Robbins	DATE 03/13/92	Commodore
DRAW: GRR	03/13/92	Schematic A1200 R2 C/A1200 Main Board "Channel Z"
LAST: BAF	01/11/93	
CHKD:		
APPR:		
USED ON C/A1200	NEXT ASSY 365132	SIZE C 365133 REV A
		SCALE SHEET 9 OF 13

PATH: /project/a300/channel_z.rev2 sheet9

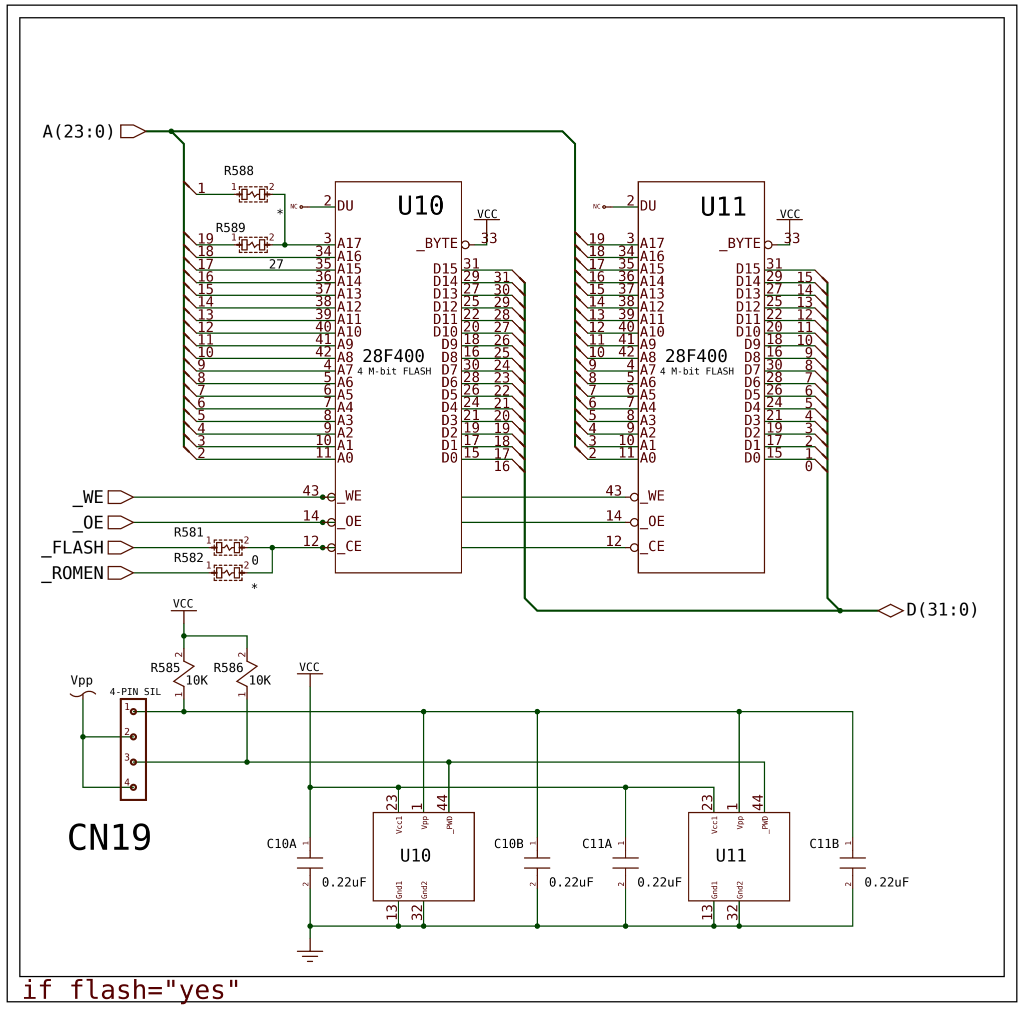
A1200 Rev 2 PCB

Rev.1.38 (06.09.2012)

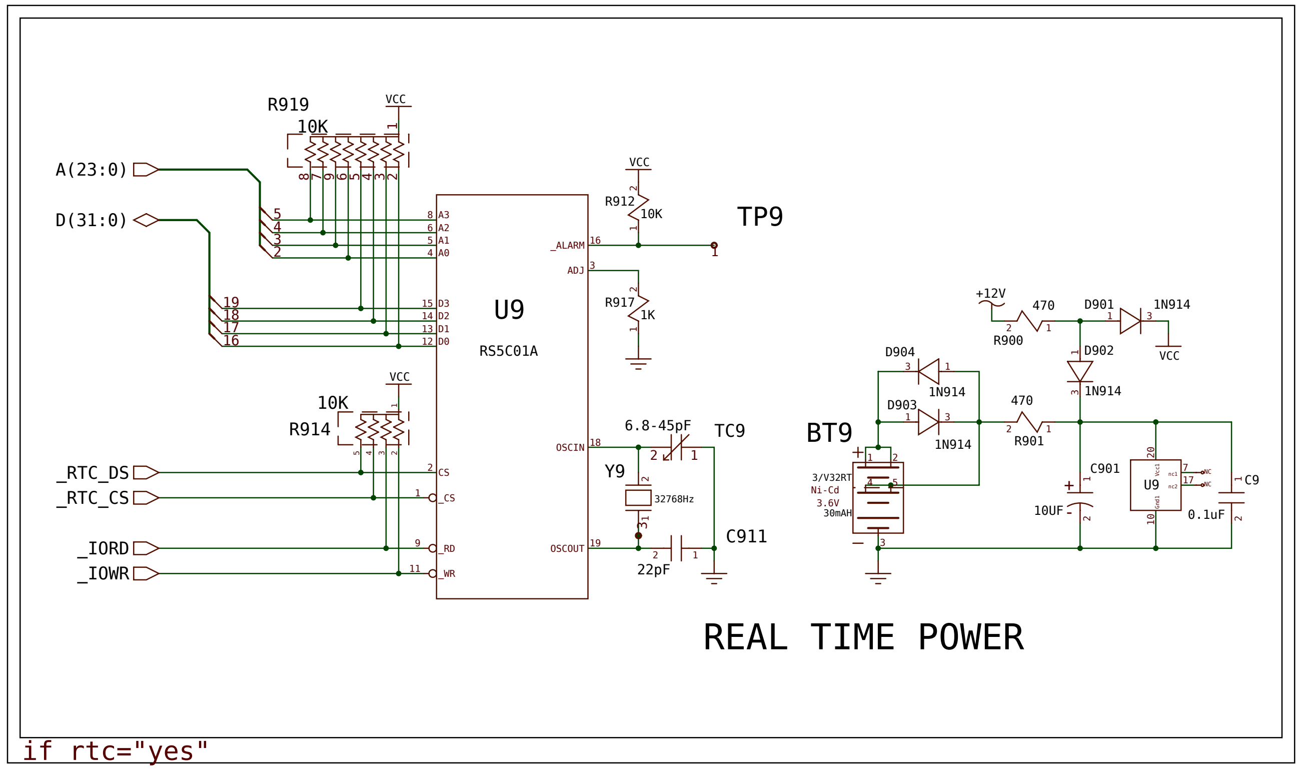

16-BIT ROM
A(23:0)
U6
62408
Mbyte ROM
_ROMOE
_ROMCS
D(31:0)
_BYTE
VCC
U6
C6
0.22uF
DECOUPLING
if rom16="yes"


32-BIT ROM
A(23:0)
R598
R599
27
U6A
62408
Mbyte ROM
U6B
62408
Mbyte ROM
_ROMOE
_ROMCS
_ROMEN
_WIDE
R593
470
D(31:0)
VCC
U6A
U6B
C6A
C6B
0.22uF
0.22uF
DECOUPLING
if rom32="yes"

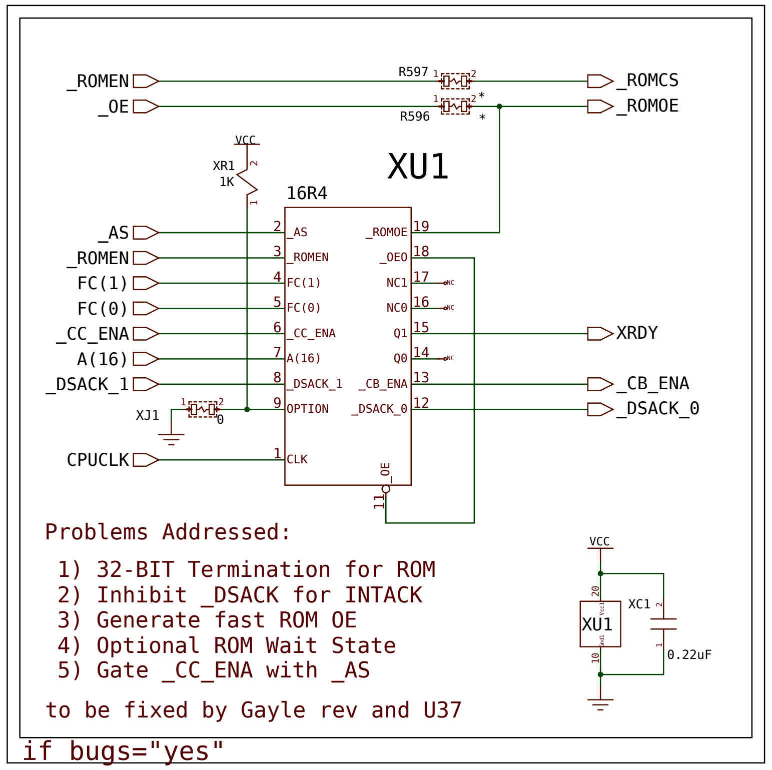
16 AND 32-BIT SOCKETS MAY OVERLAP!


A(23:0)
R588
R589
27
U10
28F400
4 M-bit FLASH
U11
28F400
4 M-bit FLASH
_BYTE
VCC
33
_WE
_OE
_FLASH
_ROMEN
R581
R582
0
D(31:0)
VCC
R585
10K
R586
10K
Vpp
4-PIN SIL
CN19
C10A
C10B
C11A
C11B
0.22uF
0.22uF
0.22uF
0.22uF
U10
U11
if flash="yes"

OPTIONAL FLASH MEMORY


R919
10K
VCC
A(23:0)
D(31:0)
U9
RS5C01A
_ALARM
ADJ
R912
10K
TP9
R917
1K
10K
R914
_RTC_DS
_RTC_CS
_IORD
_IOWR
OSCIN
OSCOUT
6.8-45pF
TC9
Y9
32768Hz
22pF
C911
BT9
3/V32RT
Ni-Cd
3.6V
30mAH
+12V
470
R900
D901
1N914
D904
1N914
D903
1N914
D902
1N914
470
R901
VCC
C901
10UF
U9
0.1uF
C9
REAL TIME POWER
if rtc="yes"

OPTIONAL REAL-TIME CLOCK/CALENDAR

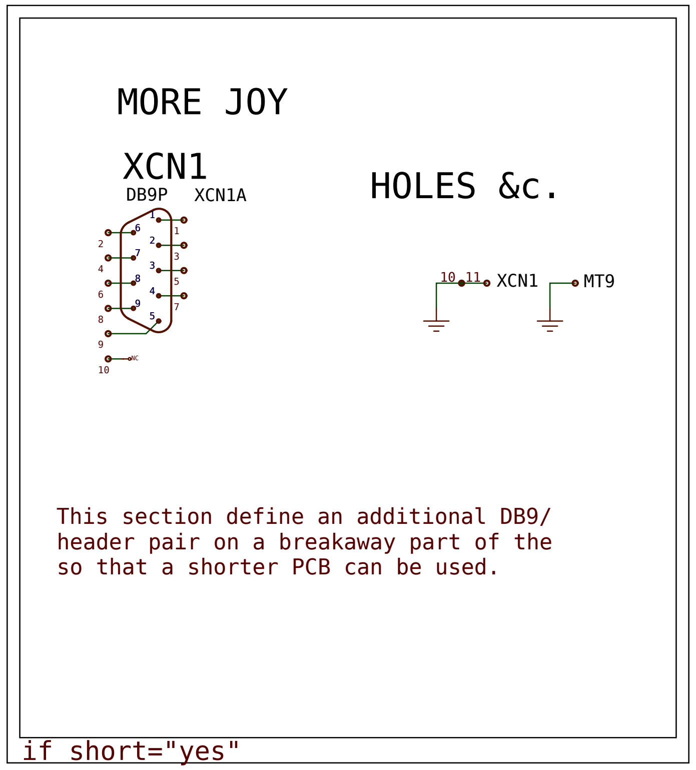

_ROMEN
_OE
R597
R596
_ROMCS
_ROMOE
VCC
XR1
1K
16R4
XU1
_AS
_ROMEN
FC(1)
FC(0)
_CC_ENA
A(16)
_DSACK_1
XJ1
CPUCLK
OPTION
CLK
_ROMOE
_OEO
NC1
NC0
Q1
Q0
_CB_ENA
_DSACK_0
XRDY
_CB_ENA
_DSACK_0
VCC
XU1
XC1
0.22uF
if bugs="yes"

Problems Addressed:

1) 32-BIT Termination for ROM
2) Inhibit _DSACK for INTACK
3) Generate fast ROM OE
4) Optional ROM Wait State
5) Gate _CC_ENA with _AS

to be fixed by Gayle rev and U37

BUGGERY


MORE JOY
XCN1
DB9P
XCN1A
HOLES &c.
XCN1
MT9
if short="yes"

This section define an additional DB9/ header pair on a breakaway part of the so that a shorter PCB can be used.

SHORT PCB TRIX

A1200 Rev 2 PCB

ROM - PLAIN AND FANCY - DODADS TOO!

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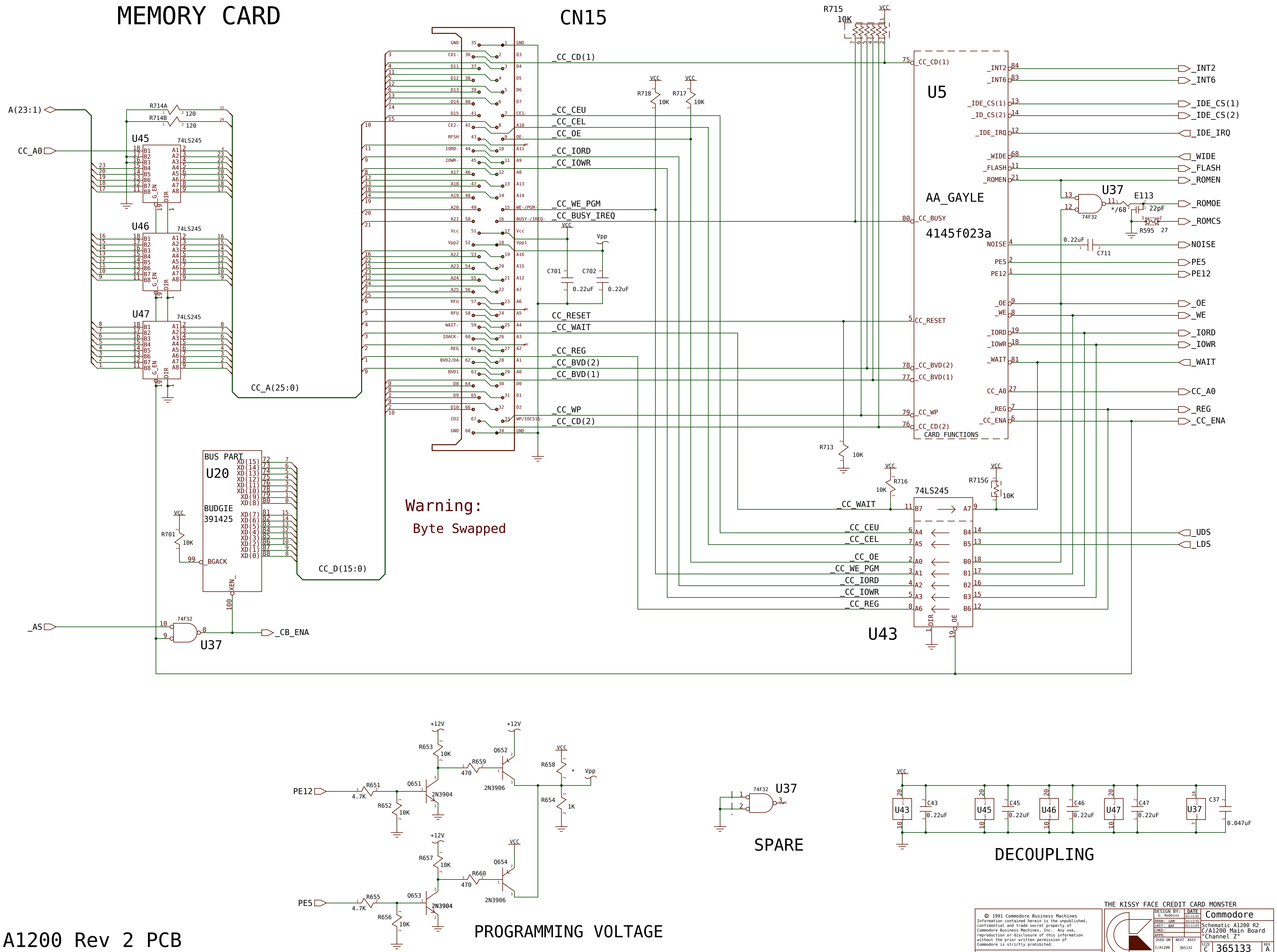
DESIGN BY: G. Robbins	DATE 03/13/92
DRAW: GRR	03/13/92
LAST: BAF	2/23/93
CHKD:	
APPR:	

USED ON C/A1200
NEXT ASSY 365132

Commodore
Schematic A1200 R2
C/A1200 Main Board
"Channel Z"
SIZE C
365133
REV A
SCALE
SHEET 10 OF 13
PATH: /project/a300/channel_z.rev2 sheet10

MEMORY CARD


CN15
U45
U46
U47
74LS245
R714A 120
R714B 120
A(23:1)
CC_A0
CC_A(25:0)
CC_D(15:0)
GND
CD1-
CE2-
RFSH
IORD-
IOWR-
Vcc
Vpp2
Vpp1
RFU
WAIT-
IOACK-
REG
BVD2/DA
BVD1
CD2
CE1-
OE-
WE-/PGM-
BUSY-/IREQ-
WP/IOCS16-
_CC_CD(1)
_CC_CEU
_CC_CEL
_CC_OE
_CC_IORD
_CC_IOWR
_CC_WE_PGM
_CC_BUSY_IREQ
CC_RESET
_CC_WAIT
_CC_REG
_CC_BVD(2)
_CC_BVD(1)
_CC_WP
_CC_CD(2)
C701
C702
0.22uF
Vpp
VCC
R718 10K
R717 10K
R715 10K
R713 10K
R716 10K
R715G 10K
U5
AA_GAYLE
4145f023a
CARD FUNCTIONS
_INT2
_INT6
_IDE_CS(1)
_IDE_CS(2)
_IDE_IRQ
_WIDE
_FLASH
_ROMEN
_ROMOE
_ROMCS
NOISE
PE5
PE12
_OE
_WE
_IORD
_IOWR
_WAIT
CC_A0
_REG
_CC_ENA
U37
74F32
E113
22pF
R595 27
*/68
C711
U43
74LS245
_UDS
_LDS
DIR
OE
U20
BUS PART
BUDGIE
391425
XD(15)
XD(0)
_BGACK
XEN_
R701 10K
_AS
_CB_ENA
Warning:
Byte Swapped
+12V
R653 10K
R659 470
Q651 2N3904
Q652 2N3906
R651 4.7K
R652 10K
R658
R654 1K
R657 10K
R660 470
Q653 2N3904
Q654 2N3906
R655 4.7K
R656 10K
SPARE
C43
C45
C46
C47
C37
0.047uF
DECOUPLING
PROGRAMMING VOLTAGE

A1200 Rev 2 PCB

THE KISSY FACE CREDIT CARD MONSTER

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DESIGN BY:	DATE
G. Robbins	03/13/92
DRAW: GRR	03/13/92
LAST: BAF	01/11/93
CHKD:	
APPR:	

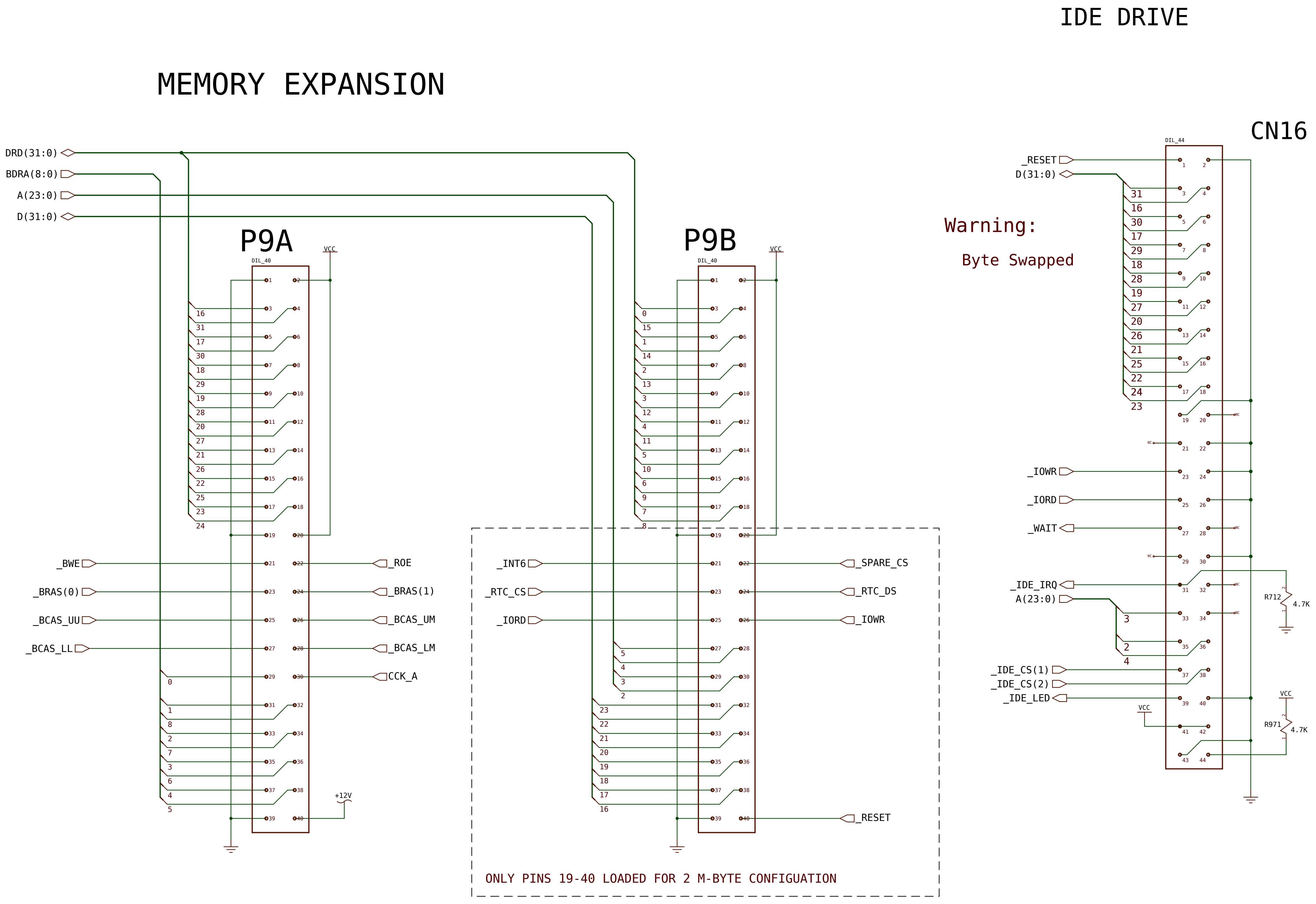
USED ON	NEXT ASSY
C/A1200	365132

Commodore

Schematic A1200 R2
C/A1200 Main Board
"Channel Z"

SIZE C
365133
REV A
SCALE
SHEET 11 OF 13

PATH: /project/a300/channel_z.rev2 sheet11


IDE DRIVE
MEMORY EXPANSION
CN16
DIL_44
_RESET
D(31:0)
31 16 30 17 29 18 28 19 27 20 26 21 25 22 24 23
Warning:
Byte Swapped
_IOWR
_IORD
_WAIT
_IDE_IRQ
A(23:0)
3 2 4
_IDE_CS(1)
_IDE_CS(2)
_IDE_LED
VCC
R712
4.7K
R971
4.7K
DRD(31:0)
BDRA(8:0)
A(23:0)
D(31:0)
P9A
DIL_40
VCC
16 31 17 30 18 29 19 28 20 27 21 26 22 25 23 24
_BWE
_BRAS(0)
_BCAS_UU
_BCAS_LL
_ROE
_BRAS(1)
_BCAS_UM
_BCAS_LM
CCK_A
0 1 8 2 7 3 6 4 5
+12V
P9B
DIL_40
VCC
0 15 1 14 2 13 3 12 4 11 5 10 6 9 7 8
_INT6
_RTC_CS
_IORD
_SPARE_CS
_RTC_DS
_IOWR
5 4 3 2
23 22 21 20 19 18 17 16
_RESET
ONLY PINS 19-40 LOADED FOR 2 M-BYTE CONFIGUATION

A1200 Rev 2 PCB

Rev.1.38 (06.09.2012)

MEMORY EXPANSION AND THE IDE DRIVE

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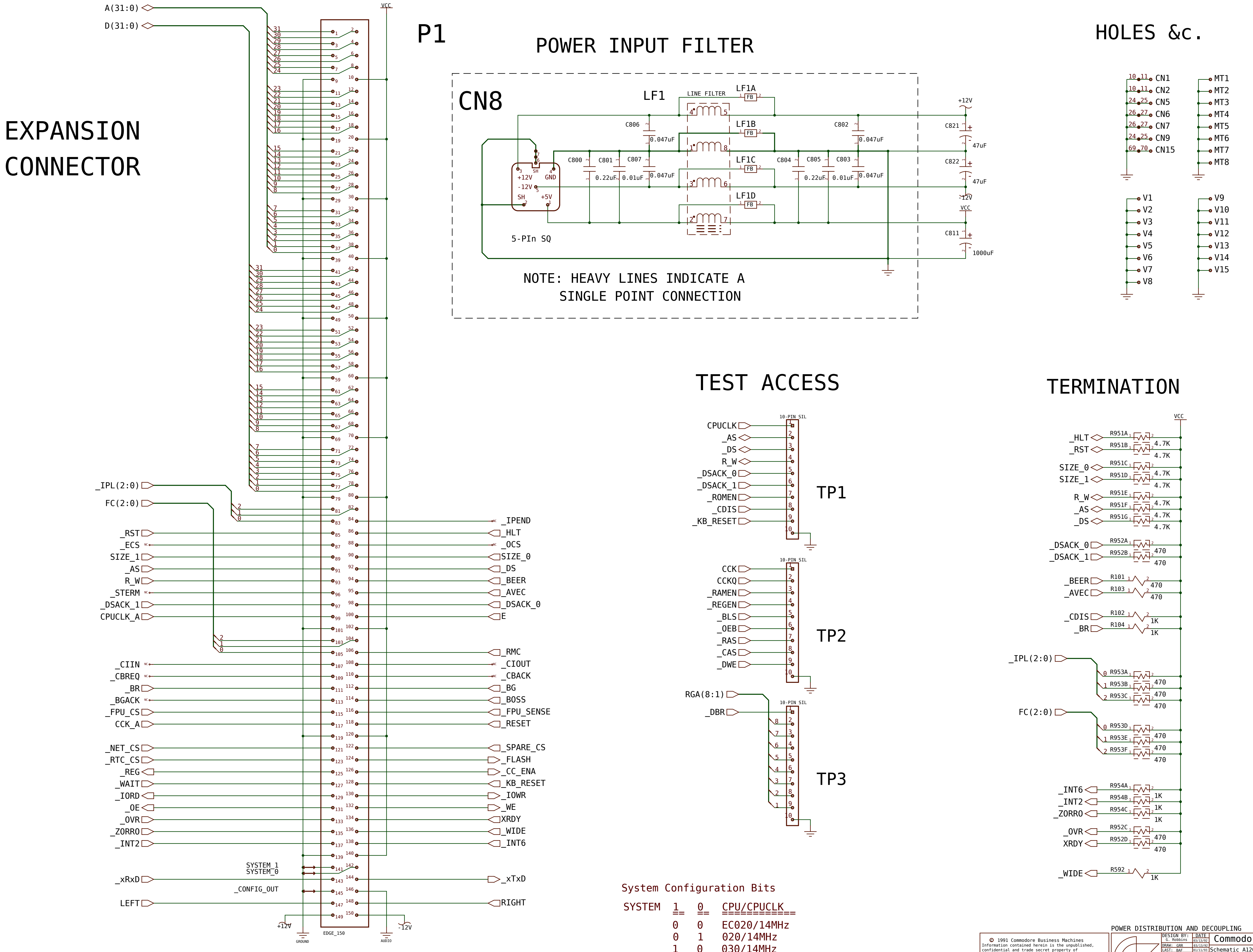
DESIGN BY: G. Robbins	DATE 03/13/92	Commodore
DRAW: GRR	03/13/92	Schematic A1200 R2 C/A1200 Main Board "Channel Z"
LAST: BAF	01/11/93	
CHKD:		
APPR:		
USED ON C/A1200	NEXT ASSY 365132	SIZE C 365133 REV A
		SCALE SHEET 12 OF 13

PATH: /project/a300/channel_z.rev2 sheet12


EXPANSION CONNECTOR
P1
A(31:0)
D(31:0)
VCC
_IPL(2:0)
FC(2:0)
_RST
_ECS
SIZE_1
_AS
R_W
_STERM
_DSACK_1
CPUCLK_A
_CIIN
_CBREQ
_BR
_BGACK
_FPU_CS
CCK_A
_NET_CS
_RTC_CS
_REG
_WAIT
_IORD
_OE
_OVR
_ZORRO
_INT2
_xRxD
LEFT
_IPEND
_HLT
_OCS
SIZE_0
_DS
_BEER
_AVEC
_DSACK_0
E
_RMC
_CIOUT
_CBACK
_BG
_BOSS
_FPU_SENSE
_RESET
_SPARE_CS
_FLASH
_CC_ENA
_KB_RESET
_IOWR
_WE
XRDY
_WIDE
_INT6
_xTxD
RIGHT
SYSTEM_1
SYSTEM_0
_CONFIG_OUT
+12V
-12V
GROUND
EDGE_150
AUDIO
POWER INPUT FILTER
CN8
LF1
LINE FILTER
LF1A
LF1B
LF1C
LF1D
FB
C806
0.047uF
C800
C801
C807
0.22uF
0.01uF
0.047uF
C802
0.047uF
C804
C805
C803
0.22uF
0.01uF
0.047uF
+12V
C821
47uF
C822
47uF
-12V
VCC
C811
1000uF
SH
+12V
GND
-12V
SH
+5V
5-PIn SQ
NOTE: HEAVY LINES INDICATE A SINGLE POINT CONNECTION
HOLES &c.
CN1
CN2
CN5
CN6
CN7
CN9
CN15
MT1
MT2
MT3
MT4
MT5
MT6
MT7
MT8
V1
V2
V3
V4
V5
V6
V7
V8
V9
V10
V11
V12
V13
V14
V15
TEST ACCESS
10-PIN SIL
CPUCLK
_AS
_DS
R_W
_DSACK_0
_DSACK_1
_ROMEN
_CDIS
_KB_RESET
TP1
10-PIN SIL
CCK
CCKQ
_RAMEN
_REGEN
_BLS
_OEB
_RAS
_CAS
_DWE
TP2
RGA(8:1)
_DBR
10-PIN SIL
TP3
TERMINATION
VCC
_HLT
_RST
SIZE_0
SIZE_1
R_W
_AS
_DS
R951A
R951B
R951C
R951D
R951E
R951F
R951G
4.7K
_DSACK_0
_DSACK_1
R952A
R952B
470
_BEER
_AVEC
R101
R103
470
_CDIS
_BR
R102
R104
1K
_IPL(2:0)
R953A
R953B
R953C
470
FC(2:0)
R953D
R953E
R953F
470
_INT6
_INT2
_ZORRO
R954A
R954B
R954C
1K
_OVR
XRDY
R952C
R952D
470
_WIDE
R592
1K

System Configuration Bits

SYSTEM	1	0	CPU/CPUCLK
	0	0	EC020/14MHz
	0	1	020/14MHz
	1	0	030/14MHz
	1	1	030/>14MHz

A1200 Rev 2 PCB

Rev.1.38 (06.09.2012)

POWER DISTRIBUTION AND DECOUPLING

C.A.D. Generated
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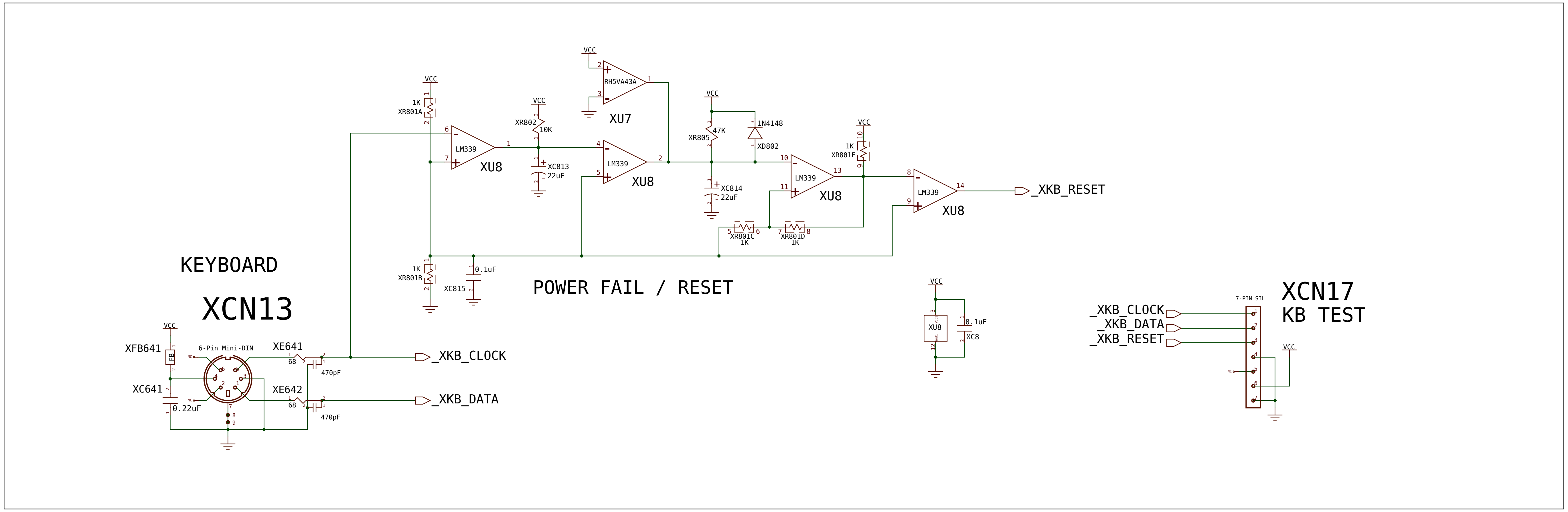
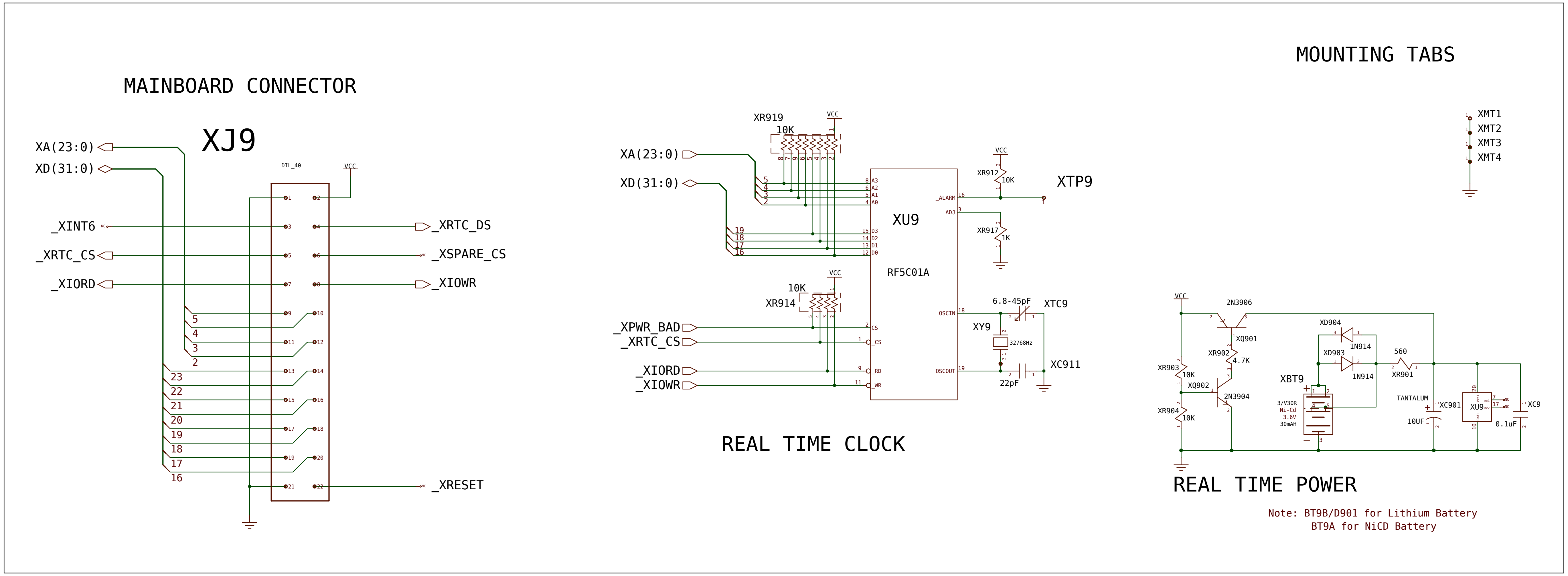
DESIGN BY: G. Robbins	DATE 03/13/92
DRAW: GRR	03/13/92
LAST: BAF	01/11/93
CHKD:	
APPR:	
USED ON C/A1200	NEXT ASSY 365132

Commodore
Schematic A1200 R2
C/A1200 Main Board
"Channel Z"
SIZE C
365133
REV A
SCALE
SHEET 13 OF 13
PATH: /project/a300/channel_z.rev2 sheet13


KEYBOARD
XCN13
VCC
XFB641
FB
XC641
0.22uF
6-Pin Mini-DIN
XE641
68
470pF
XE642
68
470pF
_XKB_CLOCK
_XKB_DATA
POWER FAIL / RESET
VCC
1K
XR801A
LM339
XU8
XR802
10K
XC813
22uF
RH5VA43A
XU7
LM339
XU8
XR805
47K
1N4148
XD802
XC814
22uF
LM339
XU8
1K
XR801E
LM339
XU8
_XKB_RESET
XR801C
1K
XR801D
1K
1K
XR801B
0.1uF
XC815
XU8
0.1uF
XC8
_XKB_CLOCK
_XKB_DATA
_XKB_RESET
7-PIN SIL
XCN17
KB TEST
NC

IF KBTEST="YES"


MAINBOARD CONNECTOR
XJ9
XA(23:0)
XD(31:0)
DIL_40
VCC
_XINT6
_XRTC_CS
_XIORD
_XRTC_DS
_XSPARE_CS
_XIOWR
5
4
3
2
23
22
21
20
19
18
17
16
_XRESET
XR919
10K
VCC
XA(23:0)
XD(31:0)
5
4
3
2
19
18
17
16
A3
A2
A1
A0
D3
D2
D1
D0
XU9
RF5C01A
_ALARM
ADJ
OSCIN
OSCOUT
CS
_CS
RD
WR
10K
XR914
_XPWR_BAD
_XRTC_CS
_XIORD
_XIOWR
VCC
XR912
10K
XTP9
XR917
1K
6.8-45pF
XTC9
XY9
32768Hz
22pF
XC911
REAL TIME CLOCK
MOUNTING TABS
XMT1
XMT2
XMT3
XMT4
VCC
2N3906
XQ901
XR902
4.7K
XR903
10K
XQ902
2N3904
XR904
10K
XD904
1N914
XD903
1N914
560
XR901
XBT9
3/V30R
Ni-Cd
3.6V
30mAH
TANTALUM
XC901
10UF
XU9
XC9
0.1uF
NC
REAL TIME POWER
Note: BT9B/D901 for Lithium Battery
BT9A for NiCD Battery

IF EXTRTC="YES"

BREAKAWAY PCB RTC OPTION

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DESIGN BY:	DATE
G. Robbins	03/13/92
DRAW: GRR	03/13/92
LAST: GRR	06/29/92
CHKD:	
APPR:	

USED ON	NEXT ASSY
C/A1200	364718

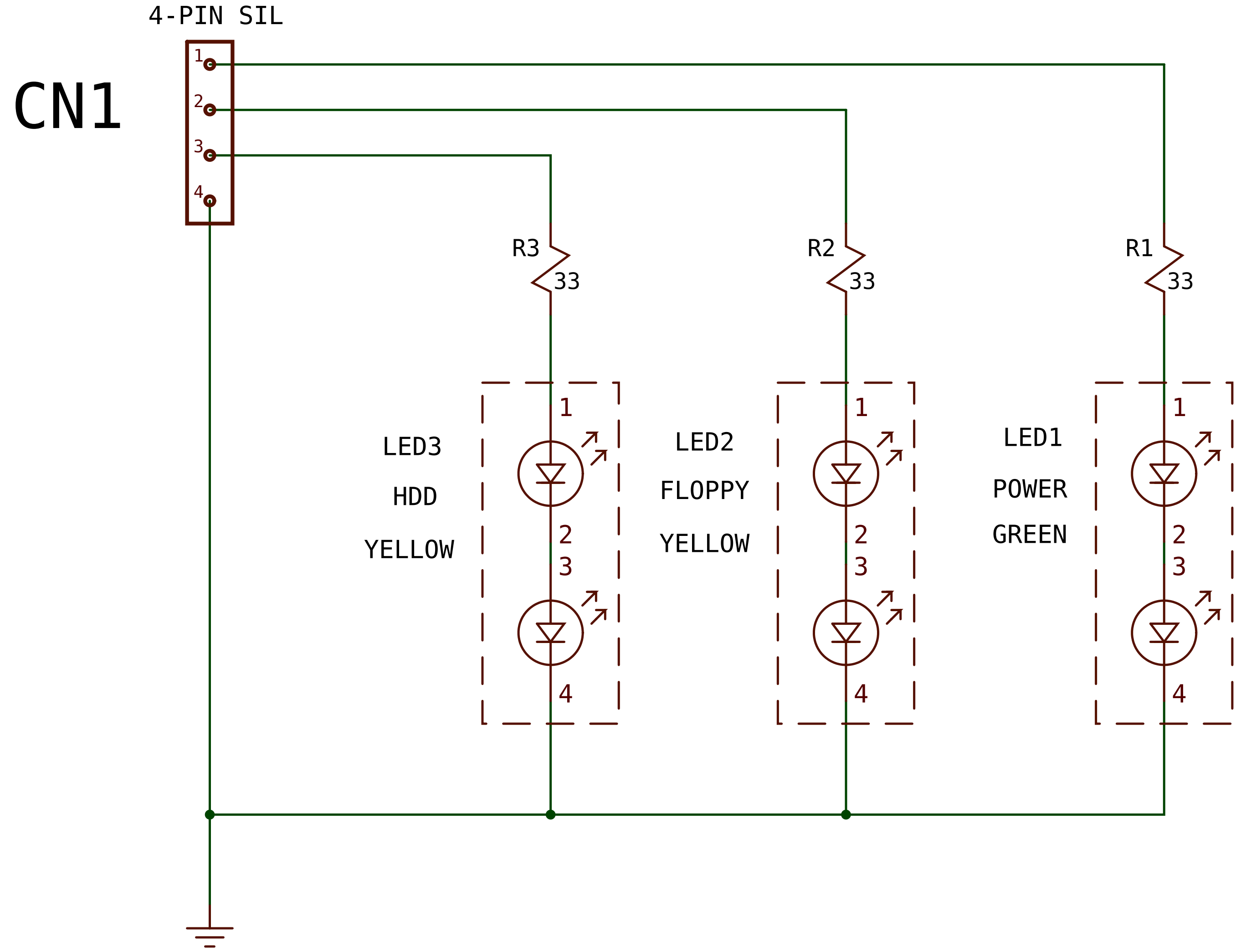
Commodore

Schematic A1200 R2
C/A1200 Main Board
"Channel Z"

SIZE C 364717 REV 2
SCALE SHEET 14 OF 13
PATH: /project/a300/channel_z.rev2 sheet13

A1200 Rev 2 PCB

REVISIONS				
REV	DESCRIPTION	DATE	APRVL	MANAGER
1	ADVANCE ENGINEERING RELEASE			


4-PIN SIL
CN1
1
2
3
4
R3
33
R2
33
R1
33
LED3
HDD
YELLOW
LED2
FLOPPY
YELLOW
LED1
POWER
GREEN
1
2
3
4
1
2
3
4
1
2
3
4

SHINE ON, SHINE ON

C.A.D. Generated
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DESIGN BY: B. FENIMORE | DATE 7/21/92
DRAW: BAF | 7/21/92
LAST: BAF | 7/21/92
CHKD:
APPR:
USED ON A1200
NEXT ASSY 364963

Commodore
SCHEMATIC
A1200 LED ASSY

SIZE A
364966
REV 1
SCALE
SHEET 1 OF 1
PATH: /user/fenimore/AA600/led_assy sheet1

A1200 LED PCB ASSEMBLY REV1

Rev.1.38 (06.09.2012)