# Lecture11: CVD and dielectric thin films

- Contents:
  - Introduction
  - CVD process sequence
  - CVD reactors
  - Basic parameters
  - CVD kinetics
  - Application of CVD dielectric films
  - Film properties
  - Dielectric CVD processes

*Reference Book: "Introduction to semiconductor manufacturing technology", by Xian, Hong, SPIE, 2nd edition, 2012*

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# Thin film

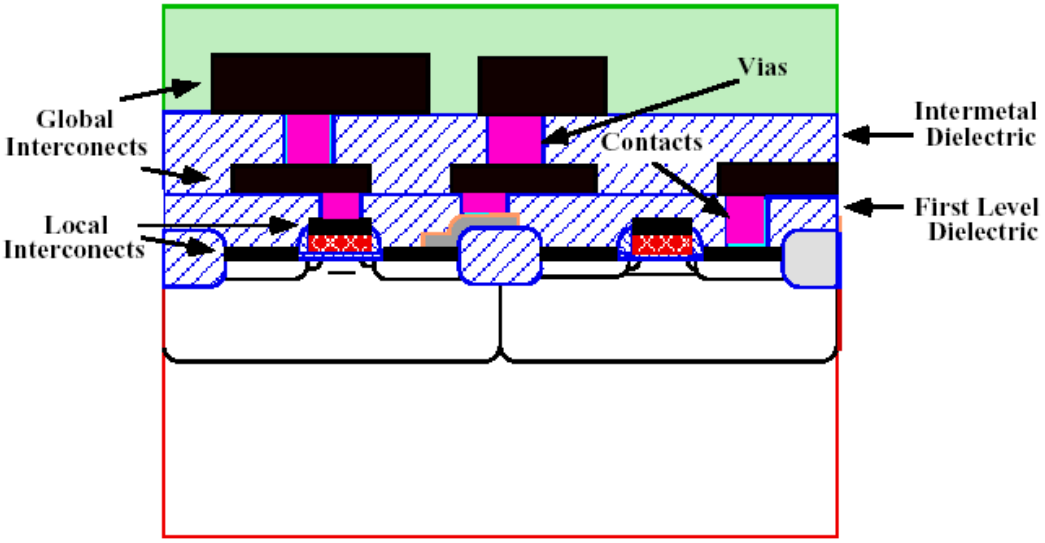
Thin film: thickness typically <1000nm.

Special properties of thin films: different from bulk materials, it may be –

- Not fully dense
- Under stress
- Different defect structures from bulk
- Quasi - two dimensional (very thin films)
- Strongly influenced by surface and interface effects

Typical steps in making thin films:

1. Emission of particles from source (heat, high voltage . . .)
2. Transport of particles to substrate
3. Condensation of particles on substrate




Lithography, thin film deposition and its etching are the three most important processes for micro-nano fabrication.

# Thin film deposition methods

Two main deposition methods are used today:

Chemical Vapor Deposition (CVD)

Reactant gases introduced in the chamber, chemical reactions occur on wafer surface leading to the deposition of a solid film.

E.g. APCVD, LPCVD, PECVD, most commonly used for dielectrics and Si.

Physical Vapor Deposition (PVD) (no chemical reaction involved)

Vapors of constituent materials created inside the chamber, and condensation occurs on wafer surface leading to the deposition of a solid film.

E.g. evaporation, sputter deposition, most commonly used for metals.

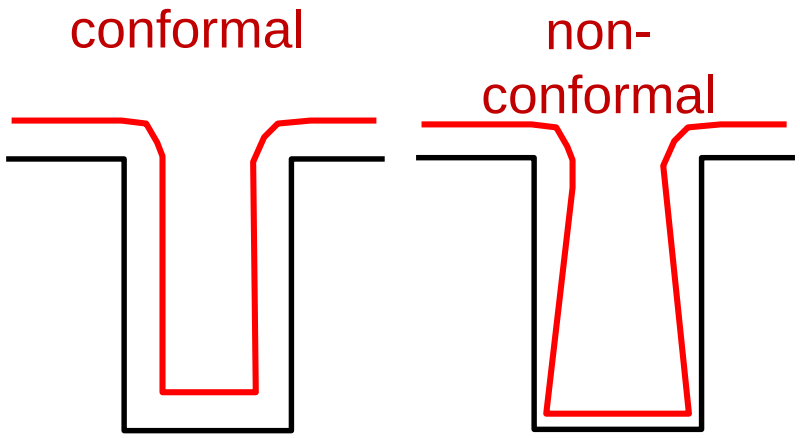
Other methods that are increasingly gaining importance in ULSI fabrication:

1. Coating with a liquid that becomes solid upon heating, e.g. spin-on-glass used for planarization.
2. Electro-deposition: coating from a solution that contains ions of the species to be coated. E.g. Cu electroplating for global interconnects.
3. Thermal oxidation.

# General characteristics of thin film deposition

- Deposition rate
- Film uniformity:
  - Across wafer uniformity.
  - Run-to-run uniformity.
- Materials that can be deposited: metal, dielectric, polymer.
- Quality of film:
  - Physical and chemical properties
  - Electrical property, breakdown voltage
  - Mechanical properties, stress and adhesion to substrate
  - Optical properties, transparency, refractive index
  - Composition, stoichiometry
  - Film density, defect (pinhole…) density
  - Texture, grain size, boundary property, and orientation
  - Impurity level, doping
- Deposition directionality:
  - Directional - good for lift-off, trench filling
  - Non-directional - good for step coverage
- Cost of ownership and operation.

# Step coverage




Poor (non-conformal) step coverage is good for liftoff.
Conformal film is good for electrical connection…

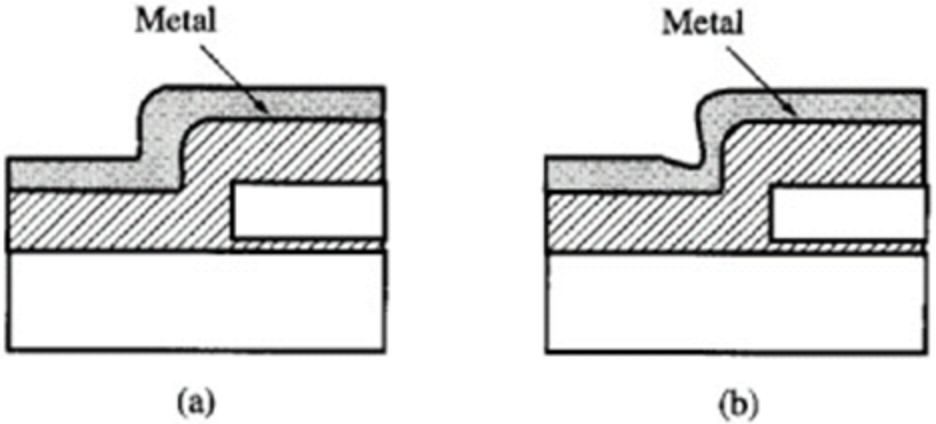
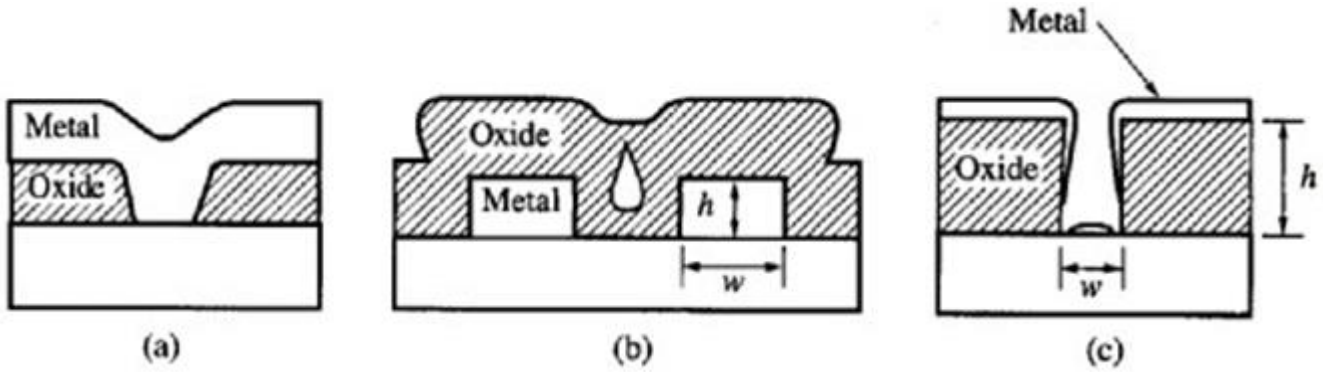


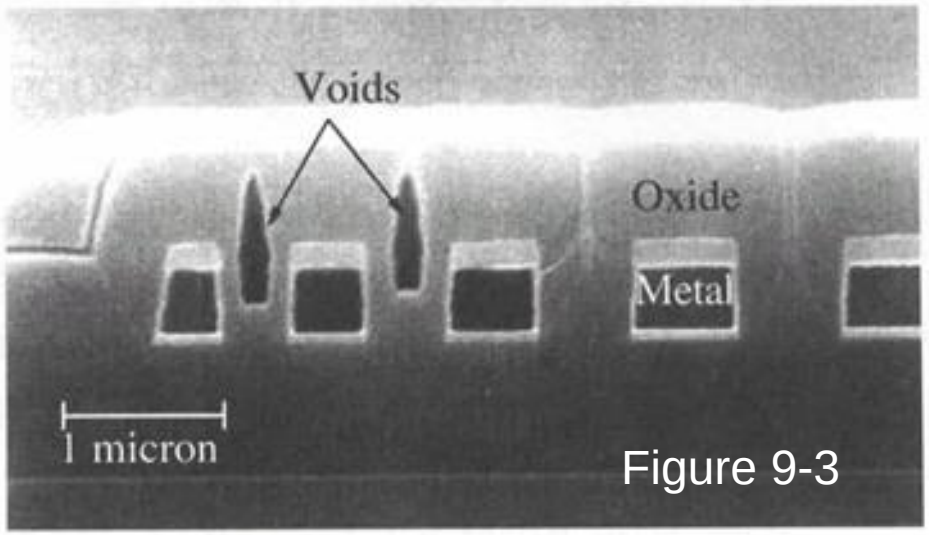

Figure: Step coverage of metal over non-planar topography.
(a) Conformal step coverage, with constant thickness on horizontal and vertical surfaces.
(b) Poor step coverage, here thinner for vertical surfaces.

# Thin film filling of holes/trenches




Aspect ratio (AR):
AR = feature height/width AR = h/w

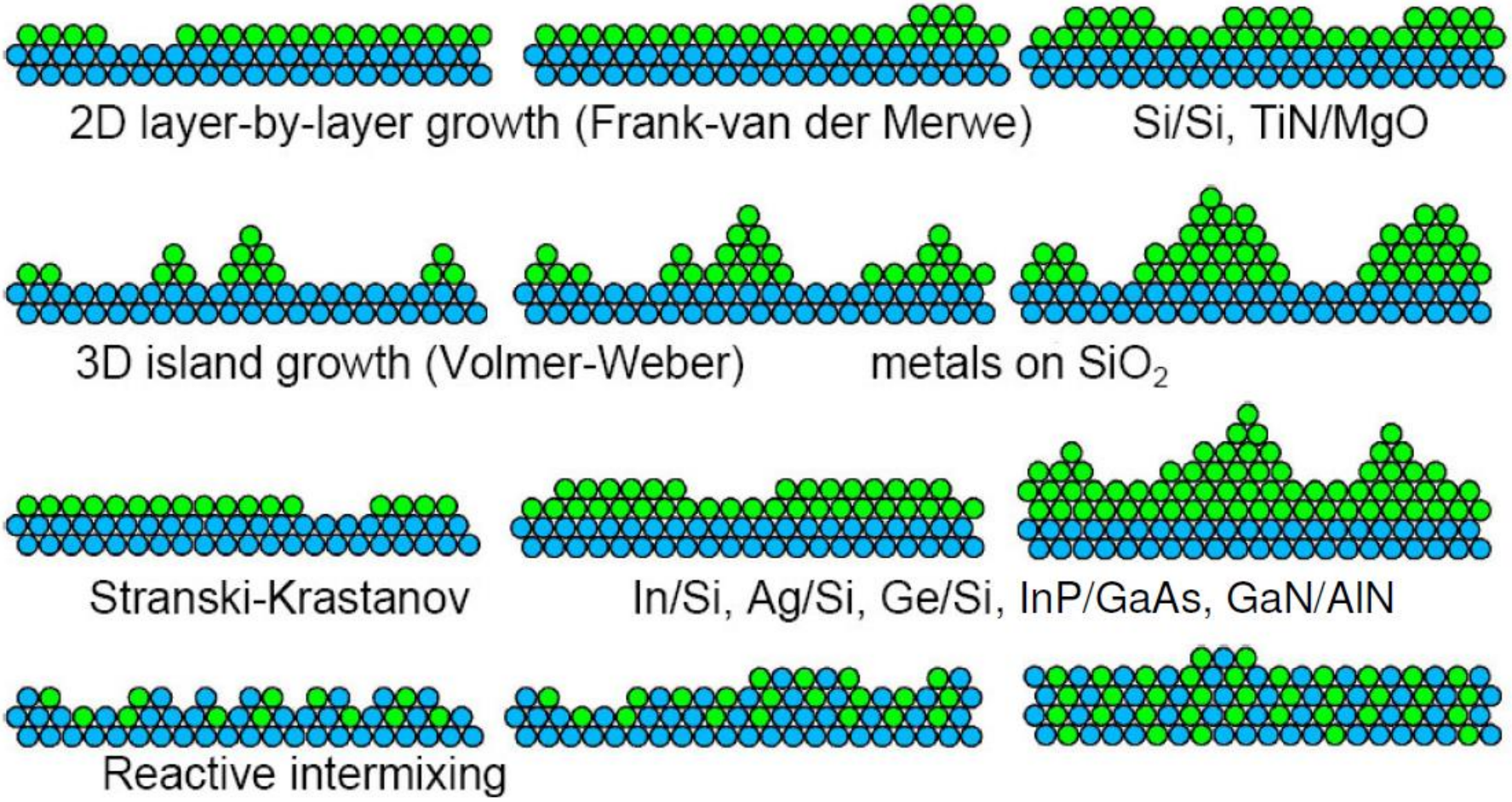
Figure: Thin film filling issues.
(a) Good metal filling of a via or contact in a dielectric layer.
(b) Silicon dioxide filling of the space between metal lines, with poor filling leading to void formation.
(c) Poor filling of the bottom of a via hole with a barrier or contact metal.




Voids in a chemical vapor deposition (CVD) oxide layer for narrow spaces between metal lines.
More difficult to fill without void for higher aspect ratio.

# Four equilibrium growth/deposition modes

Epitaxy = crystal structure of film fits with the one of the substrate



# Four growth modes

- Layer by layer growth (Frank - van der Merwe): film atoms more strongly bound to substrate than to each other and/or fast diffusion
- Island growth (Volmer - Weber): film atoms more strongly bound to each other than to substrate and/or slow diffusion.
- Mixed growth (Stranski - Krastanov): initially layer by layer then forms three dimensional islands.

Thin film types based on crystallinity:

- Epitaxial (single-crystalline, formed layer-by-layer, lattice match to substrate): no grain boundaries, requires high temperatures and slow growth rate. High quality thin films such as III-V semiconductor films (e.g. GaAs) and complex oxides.
- Polycrystalline (island  or mixed growth): lots of grain boundaries, e.g. most elemental metals grown near room temperatures.
- Amorphous (island or mixed growth): no-crystalline structures (yet with some short range atomic ordering), no crystalline defects, e.g. common insulators such as amorphous $SiO_2$.

# Equilibrium growth modes

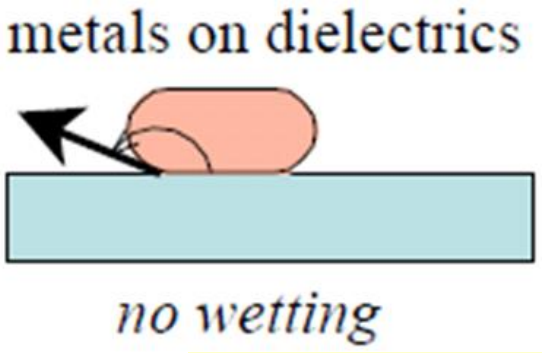
**GROWTH MODE AFFECTED BY**

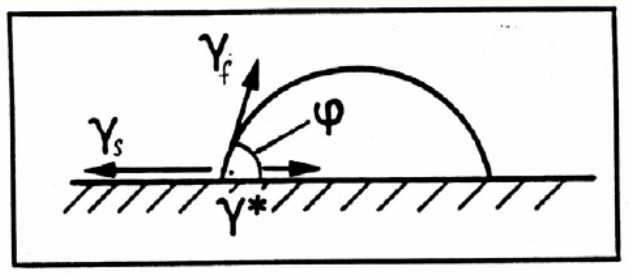
* **LATTICE MISMATCH** (important only for epitaxy)

* **SUPERSATURATION** $\Delta\mu = k_B T_s \ln\zeta$

$\zeta = p/p_e$ **determines change of Gibbs Free Energy from gas to solid**

* **SURFACE, INTERFACE FREE ENERGY** (wetting properties)



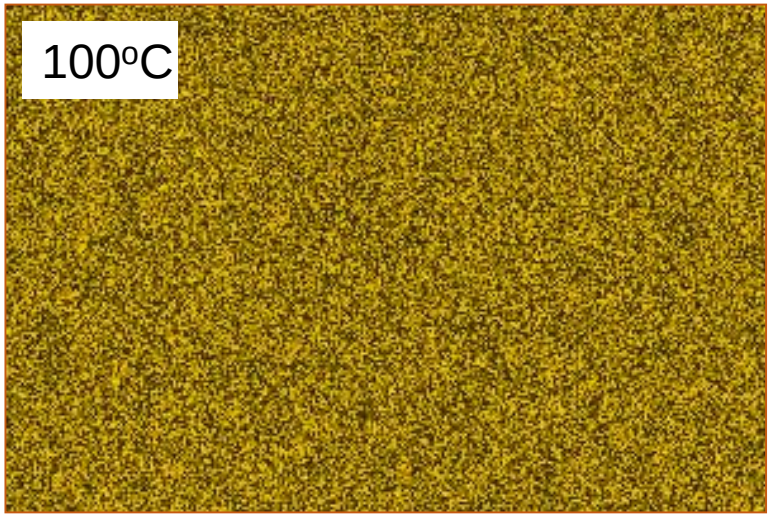

$\varphi = 0 \quad \gamma_S > \gamma_F + \gamma^* - \beta\Delta\mu$ **LAYER GROWTH**

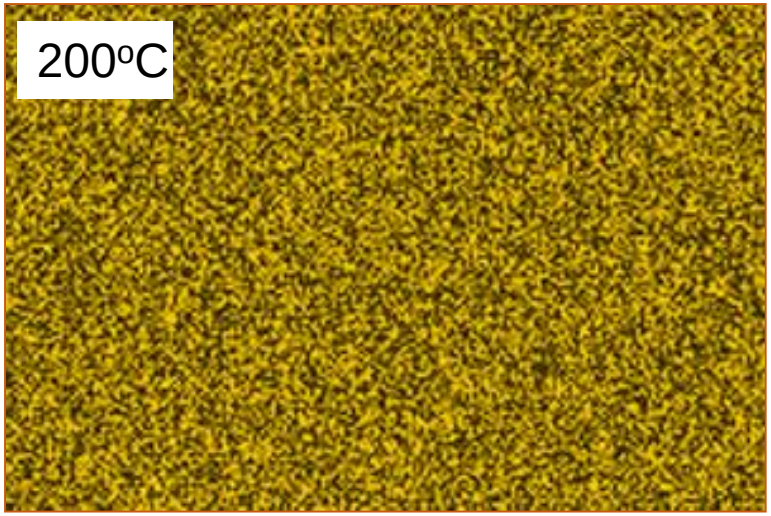
$\varphi > 0 \quad \gamma_S < \gamma_F + \gamma^* - \nu\Delta\mu$ **ISLAND GROWTH**

- Noble metals don't bond ("wet") to $Si/SiO_2$ substrate, so tend to have island growth.
- Ag always form island (not continuous film); Au is better than Ag.
- Adhesion layer Ti or Cr can reduce island formation, but for Ag, surface is still very rough.
- Here, higher adhesion is because Ti or Cr bond chemically to O in $SiO_2$.

# Effect of substrate temperature on the lateral grain size

100 Å thick Au films deposited at 100, 200, and 300°C by vacuum evaporation

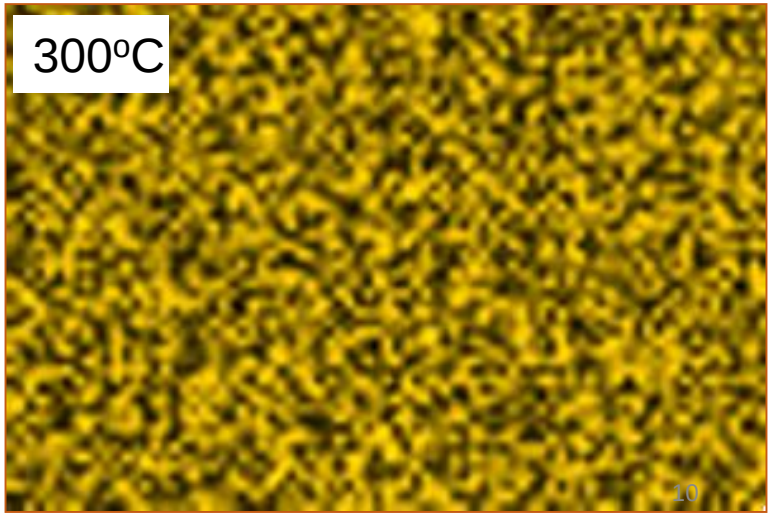



The small islands start coalescing with each other in an attempt to reduce the surface area.

This tendency to form bigger islands is termed agglomeration and is enhanced by increasing the surface mobility of the adsorbed species, such as by increasing the substrate temperature.

Except under special conditions, the crystallographic orientation and the topographical details of different islands are randomly distributed.



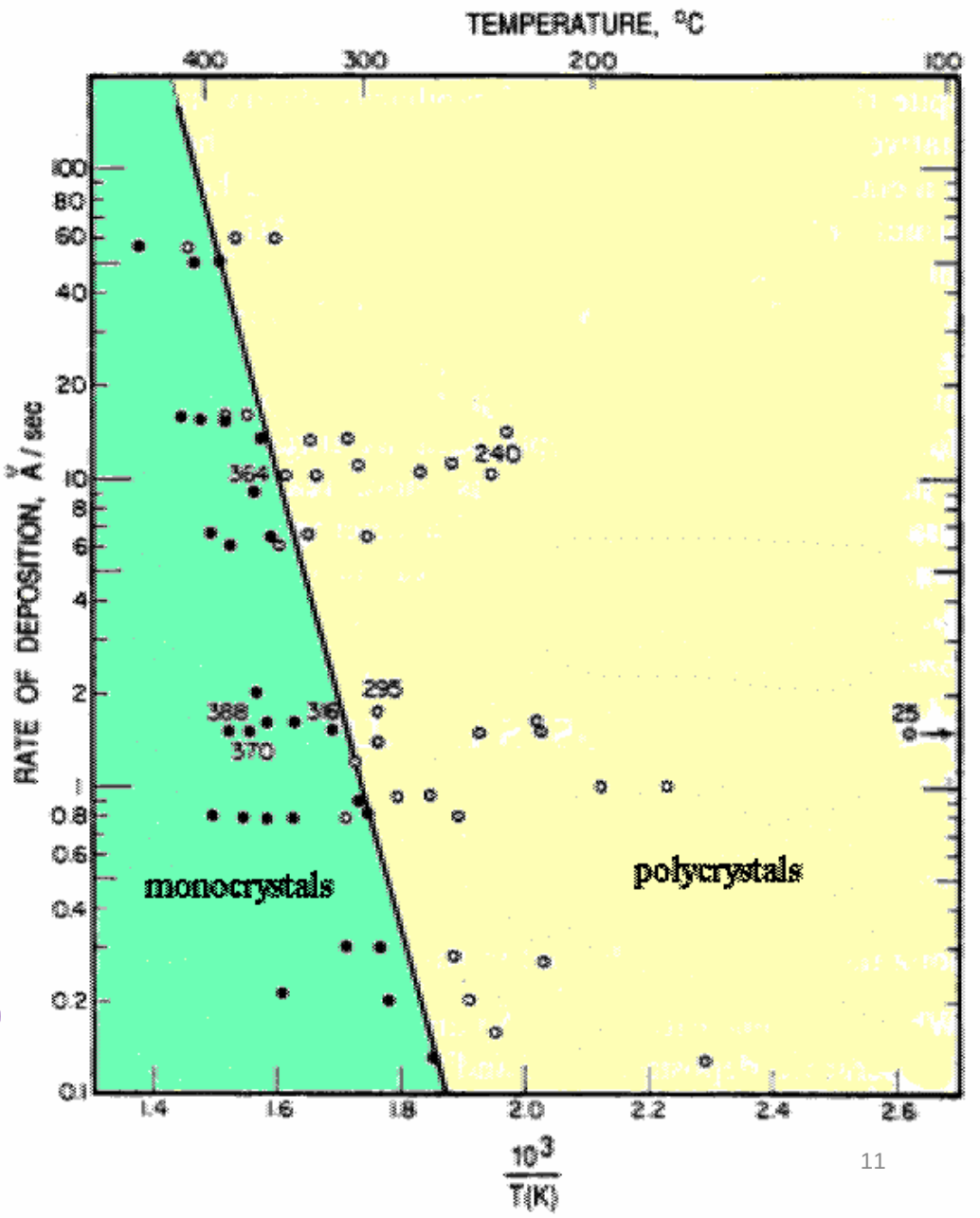
# Dependence on substrate temperature and deposition rate

In this case, if equilibrium is achieved for all ad-atoms, film will be mono-crystal (epitaxy).

Higher temperature increases ad-atom's surface mobility. It will stop once it finds the lowest energy position nearby.

But too fast deposition stops the movement (before the ad-atom finds the lowest energy position nearby) when that ad-atom is covered by a later arrival ad-atom.

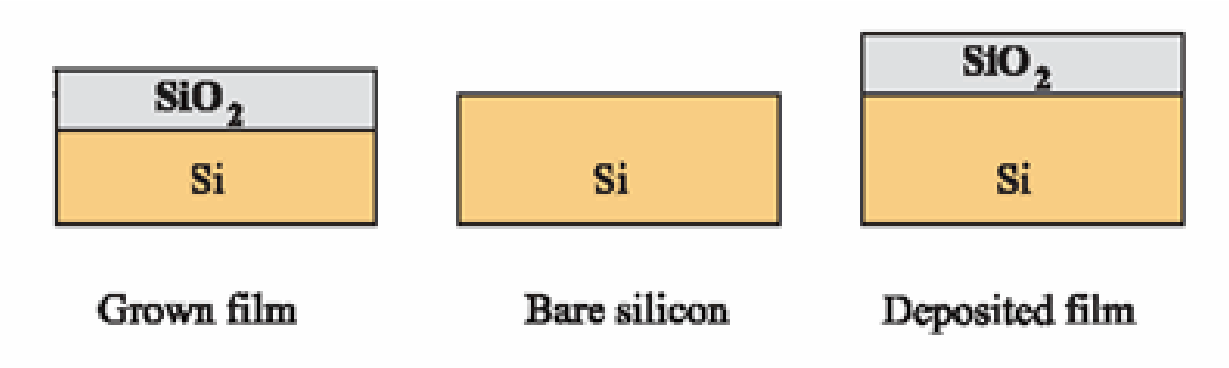
Cu films deposited on (111) NaCl substrate.



# Dielectric thin films in IC chip

# Thermal grown vs. deposited dielectric films

- Two types of dielectric thin films: thermal grown and deposited thin films.
- Thermal grown oxide consumes silicon from the substrate, while deposited film does not.
- Deposited oxide, both silicon and oxygen come from the gas phase.
- Thermal grown films were discussed in thermal processes.
- This lecture covers deposited dielectric films using CVD.




Thermal grown and deposited thin films

# 2 types of common oxides

**Undoped Silicate Glass – USG**

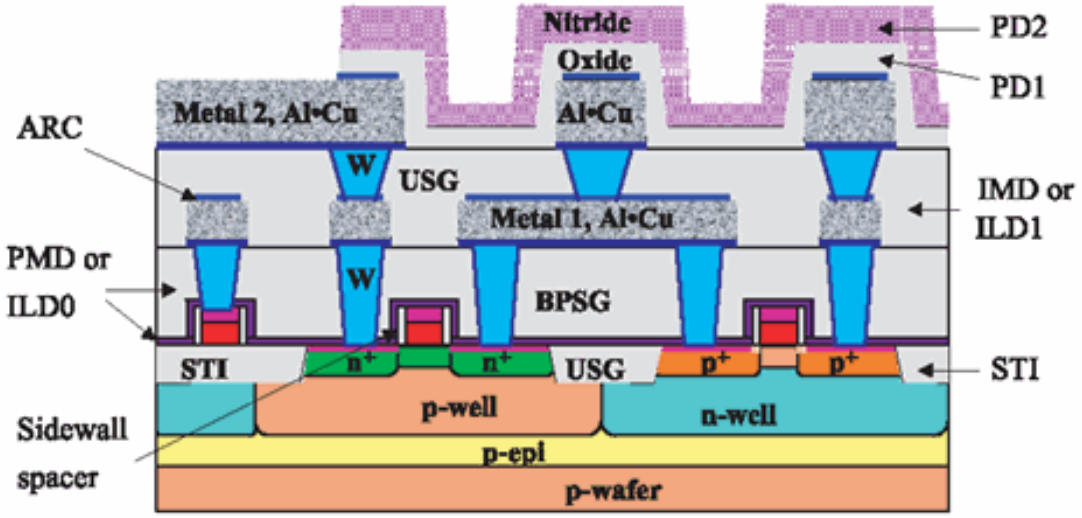
Undoped silicate glass has a high deposition rate at low temperatures, and has similar properties to silicon dioxide. This means it is easy to deposit via plasma enhanced CVD (PECVD), HDP-CVD or SACVD. It's most common as an insulator and passivation layer in multilevel IMD applications.

**Borophosphosilicate Glass – BPSG**

Borophosphosilicate glass (BPSG) is a coating made from a mixture of oxygen and hydrides of silicon (silane – $SiH_4$), boron (diborane – $B_2H_6$), and phosphorus (phosphine – $PH_3$). It is also called a doped oxide film because it is similar to silicon dioxide with the addition boron and phosphorus, which change its thermal properties. The addition of hydrides drastically lowers the melting point of glass, which make this process very useful when a wafer has limited thermal capabilities.

# Applications of deposited dielectric thin films in CMOS circuit

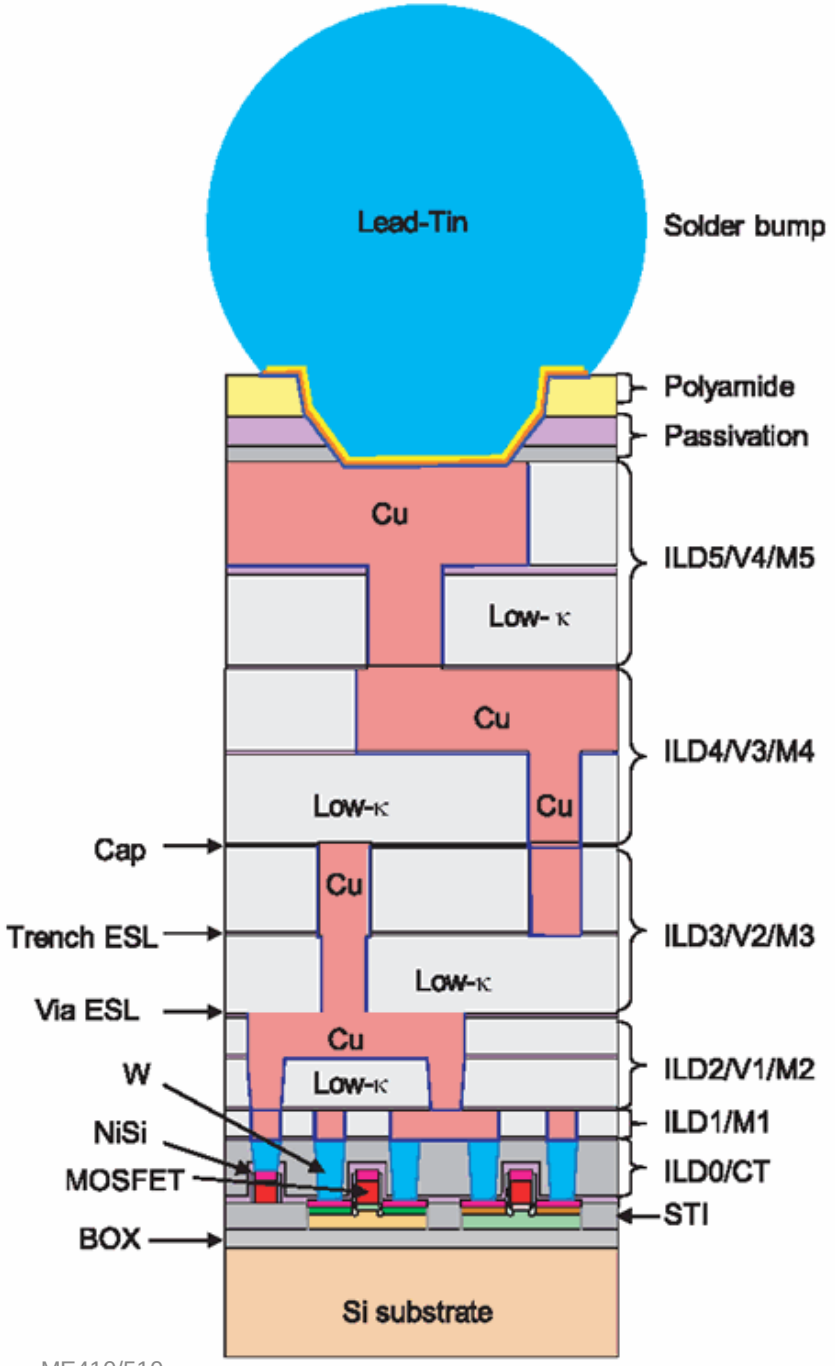
- Main role: as a dielectric layer for electrical insulation in multilevel metal interconnections.
- Also used in STI as electrical insulation between neighboring transistors.
- It's also used as a passivation dielectric seals the IC chip to protect the circuits from environment.




Application of dielectric films in a CMOS circuit with Al-Cu interconnection

Dielectric thin films in a CMOS circuit with Cu/low k ILD with 5 layers of ILD.

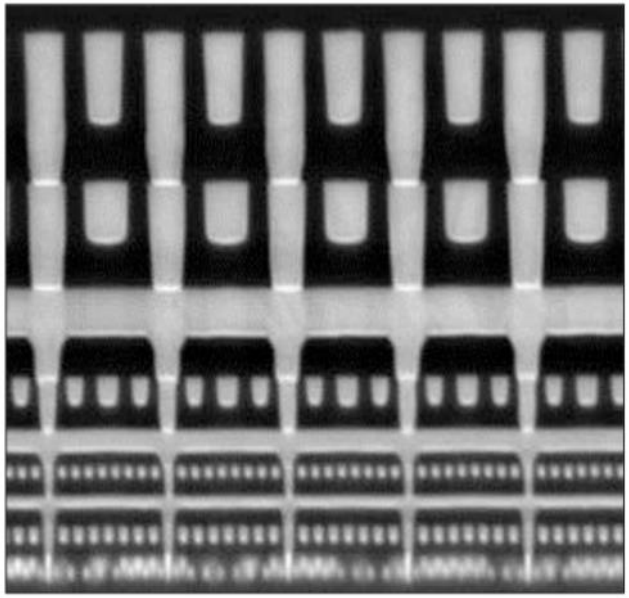
Modern chip has more than 10 ILD layers. ➔ needs many deposited dielectric layers.



# Intel's interconnect XTEM

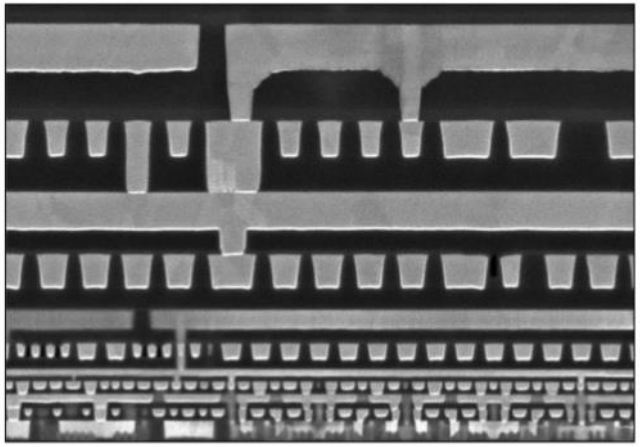
## Interconnects

22 nm Process



80 nm minimum pitch

14 nm Process



52 nm (0.65x) minimum pitch

*52 nm Interconnect Pitch Provides Better-than-normal Interconnect Scaling*

# Chemical vapor deposition (CVD)

# Chemical vapor deposition (CVD)

- CVD is a process in which a gaseous chemical precursor (or precursors) has a chemical reaction on the wafer surface and deposits a solid byproduct as a layer of thin film. Other byproducts are gases and leave the surface.

CVD films in IC industry

| | FILMS | PRECURSORS |
|---|---|---|
| **Semiconductor** | Si (poly) | $SiH_4$ (silane) |
| | Si (epi) | $SiCl_2H_2$ (DCS)<br>$SiCl_3H$ (TCS)<br>$SiCl_4$ (Siltet) |
| **Dielectrics** | Oxide | $SiH_4$, $O_2$<br>$SiH_4$, $N_2O$<br>$Si(OC_2H_5)_4$ (TEOS), $O_2$<br>TEOS<br>TEOS, $O_3$ (ozone) |
| | Oxynitride | $SiH_4$, $N_2O$, $N_2$, $NH_3$ |
| | $Si_3N_4$ | $SiH_4$, $N_2$, $NH_3$<br>$SiH_4$, $N_2$, $NH_3$<br>$C_8H_{22}N_2Si$ (BTBAS) |
| | Low-κ | 3MS (trimethylsilane),<br>4MS (tetramethylsilane), etc., and $O_2$ |
| | ULK | DEMS (diethoxymethylsilane) and $C_6H_{10}O$ (cyclohexene oxide) |
| | W (Tungsten) | $WF_6$ (tungsten hexafluoride), $SiH_4$, $H_2$ |
| **Conductors** | $WSi_2$ | $WF_6$ (tungsten hexafluoride), $SiH_4$, $H_2$ |
| | TiN | $Ti[N(CH_3)_2]_4$ (TDMAT) |
| | Ti | $TiCl_4$ |
| | Cu | Cu (hfac) (vtms) |

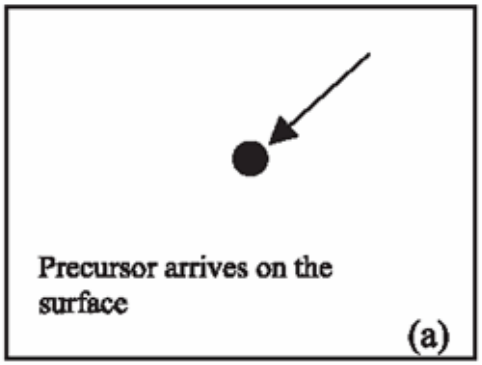
Our focus today
On dielectric films

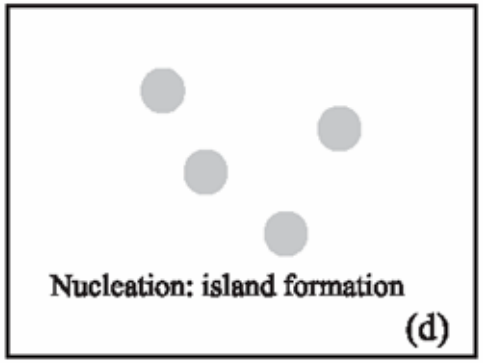
# CVD process sequence

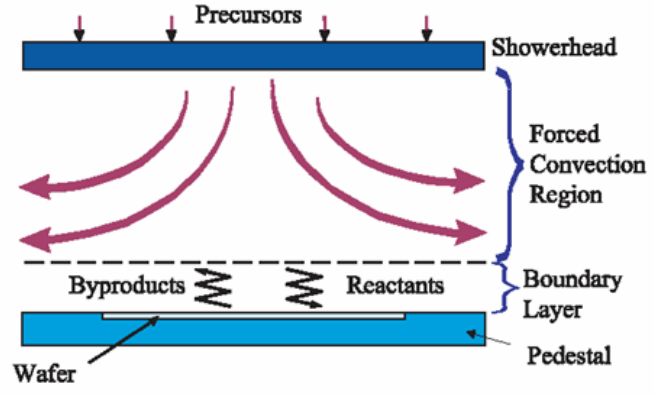
# CVD process sequence

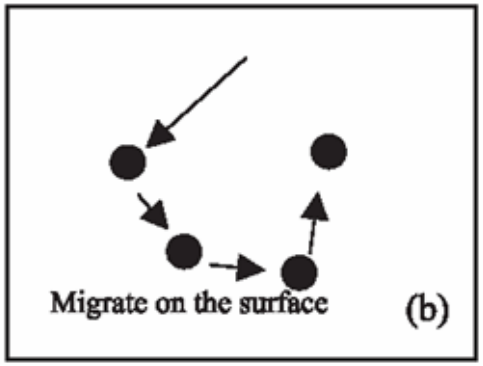
1. Gas or vapor phase precursors are introduced into the reactor
2. Precursors diffuse across the boundary layer and reach the substrate surface
3. Precursors adsorb on the substrate surface
4. Adsorbed precursors migrate on the substrate surface
5. Chemical reaction occurs on the substrate surface
6. Solid byproducts form nuclei on the substrate surface
7. Nuclei grow into islands
8. Islands merge into the continuous thin film
9. Other gaseous byproducts desorb from the substrate surface
10. Gaseous byproducts diffuse across the boundary layer
11. Gaseous byproducts flow out of the reactor

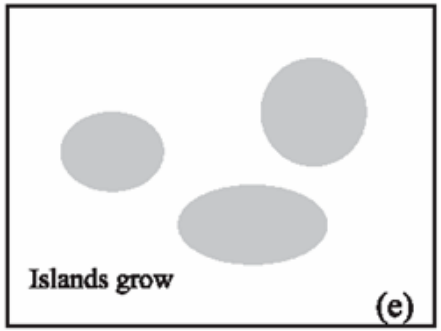
# CVD process sequence (con'd)

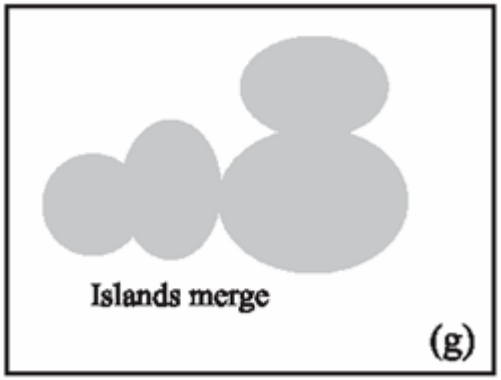


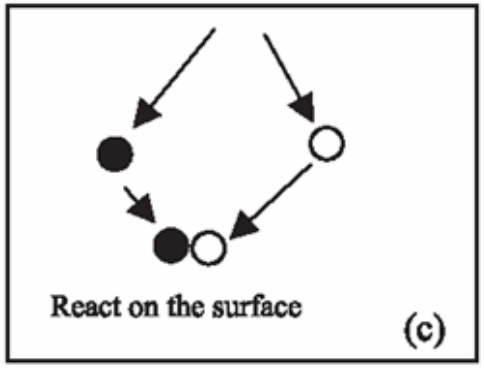



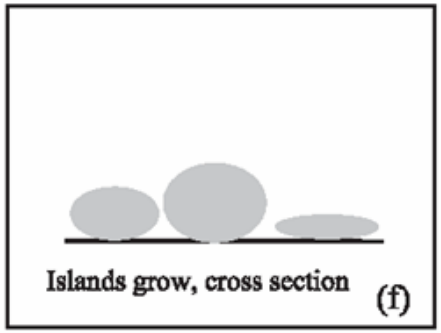



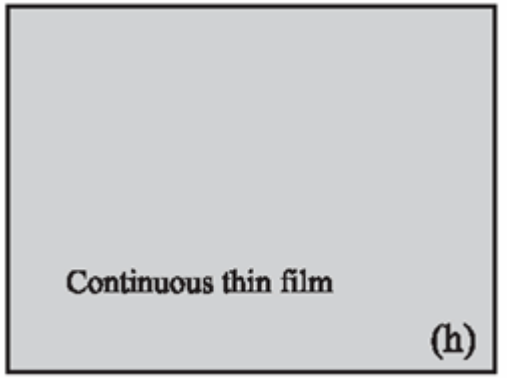



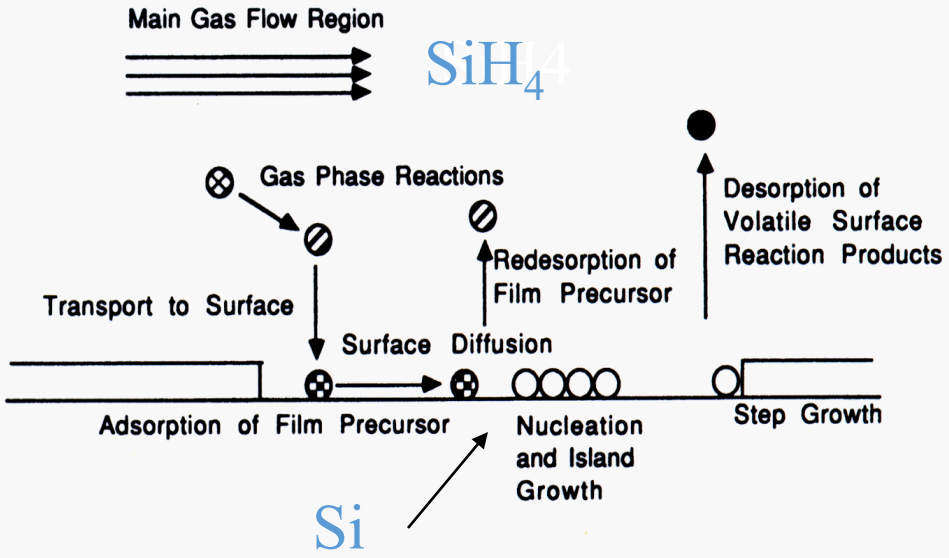



# Chemical vapor deposition (CVD): reaction mechanisms

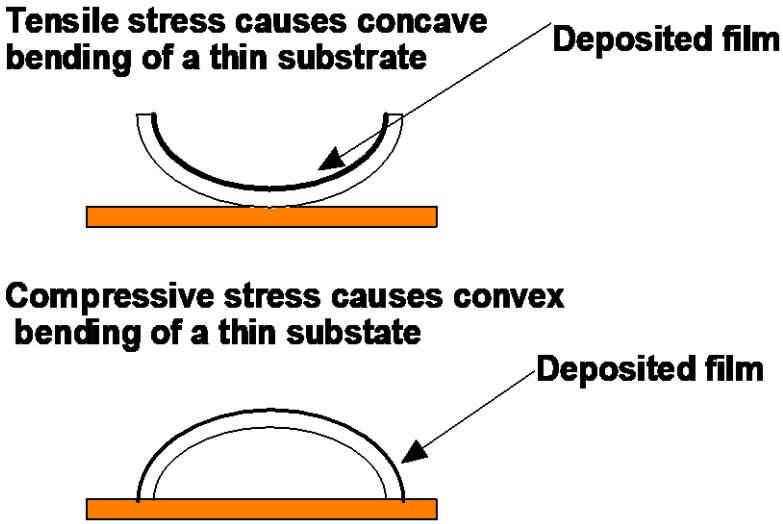
- Mass transport of the reactant in the bulk
- Gas-phase reactions (homogeneous)
- Mass transport to the surface
- Adsorption on the surface
- Surface reactions (heterogeneous)
- Surface migration
- Incorporation of film constituents, island formation
- Desorption of by-products
- Mass transport of by-produccts in bulk

CVD: Diffusive-convective transport of depositing species to a substrate with many intermolecular collisions-driven by a concentration gradient



# Chemical vapor deposition (CVD) : overview

- CVD (thermal)
  - APCVD (atmospheric)
  - LPCVD (<10 Pa)
  - VLPCVD (<1.3 Pa)
- PE CVD (plasma enhanced)
- Photon-assisted CVD
- Laser-assisted CVD
- MOCVD



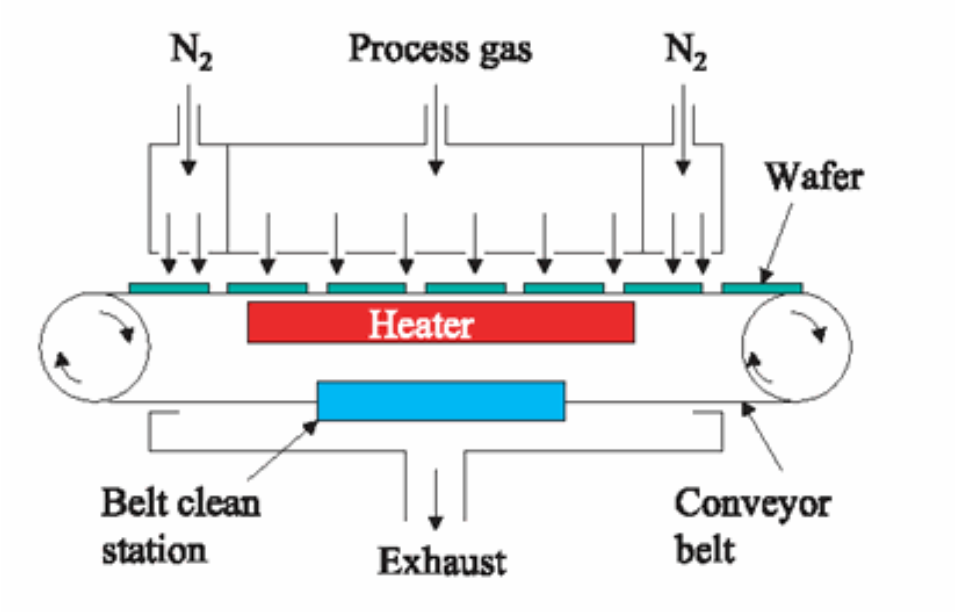
# CVD reactors

# CVD reactor types

- Three types of CVD reactors are commonly used in IC fabs:
  - Atmospheric pressure CVD (APCVD)
  - Low pressure CVD (LPCVD)
  - Plasma-enhanced CVD (PECVD)

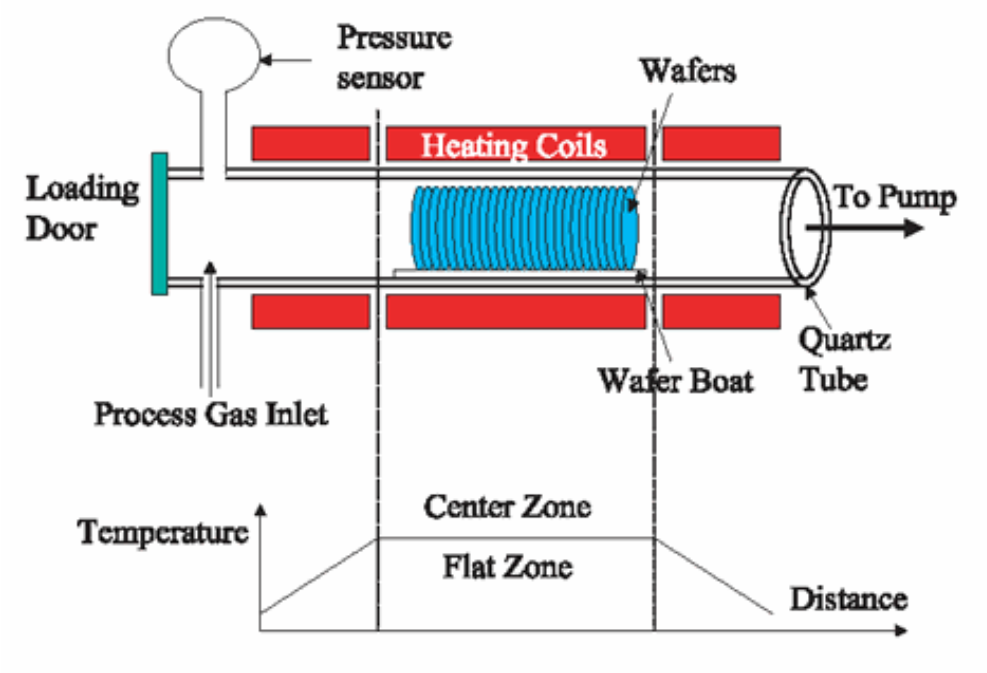
# 1. Atmospheric pressure CVD reactor

- APCVD operates at atmospheric pressure (760 torr).
- The two nitrogen buffer zones prevent the process gases from leaking into the atmosphere.
- The conveyor belt transports wafers into the process zone.
- Wafers are heated.
- The process is controlled by the temperature, gas flow rate and belt speed.



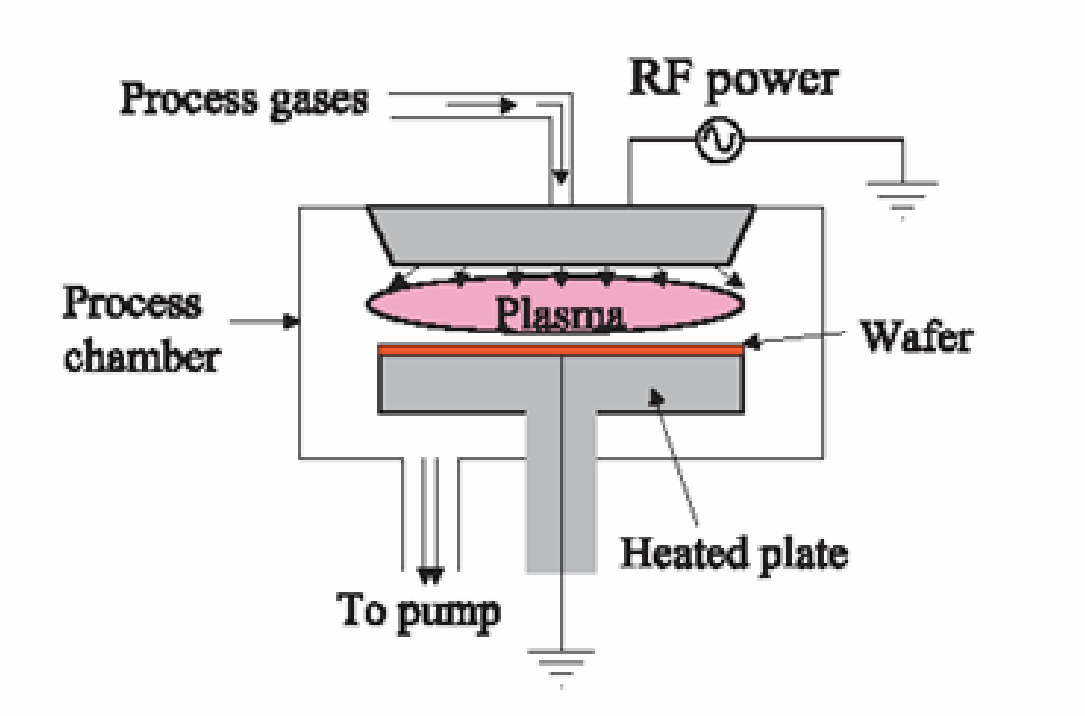
# 2. Low pressure CVD reactor

- LPCVD operates at low pressure ( 0.1 to 1 torr).
- Wafers are processed at the flat heating zone.
- It operates at high temperature ( ~ > 650 °C).
- The process is mainly controlled by the wafer temperature.



# 3. Plasma-enhanced CVD reactor

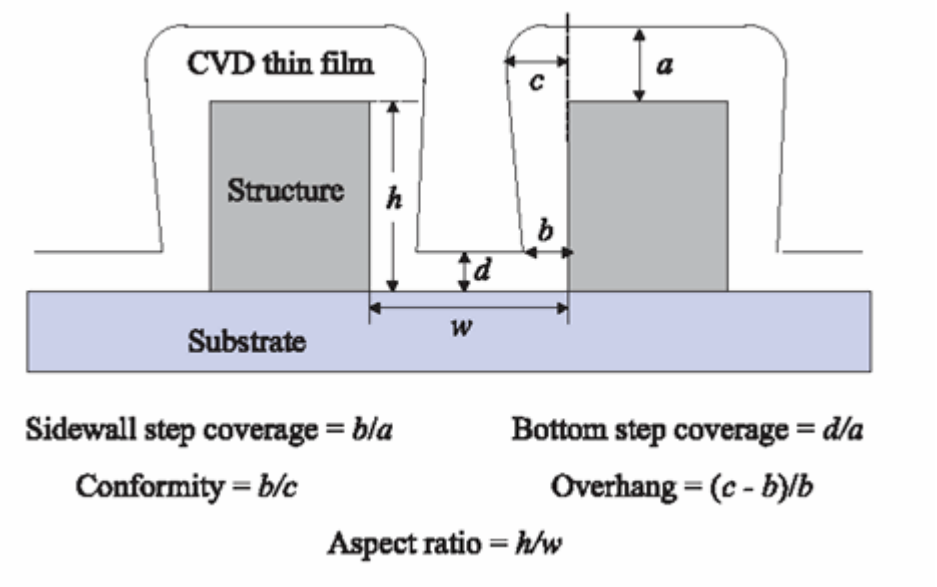
- PECVD operates at a pressure of 1 to 10 torr.
- The free radicals generated by plasma dramatically increase the chemical reaction rate.
- PECVD can achieve high deposition rate at relatively low temperature ➔ ideal for depositing ILD layers.

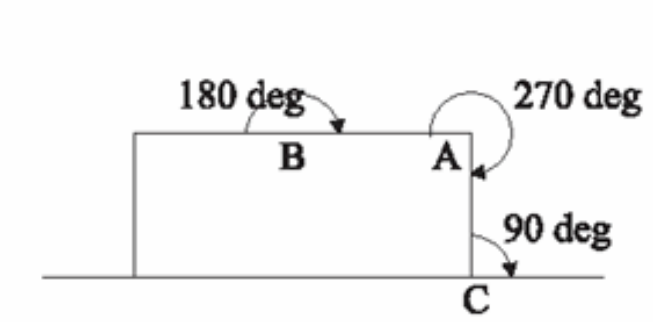


# CVD basics
# Recipe parameters

# Step coverage, conformity, overhang and arriving angle

- Definition of step coverage, conformity, overhang and precursor arriving angle

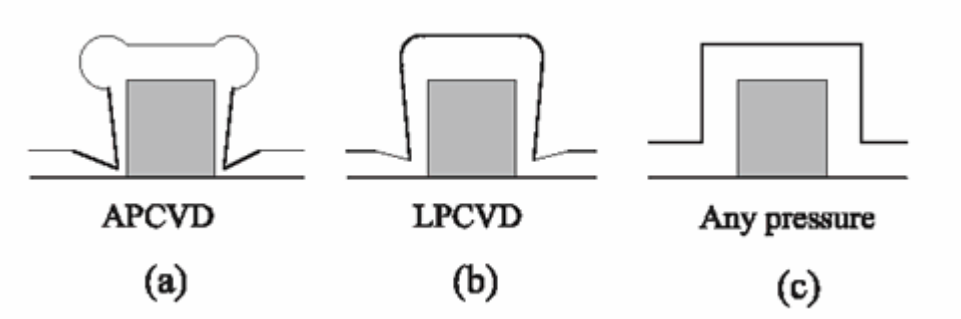



Arriving angle

# Step coverage

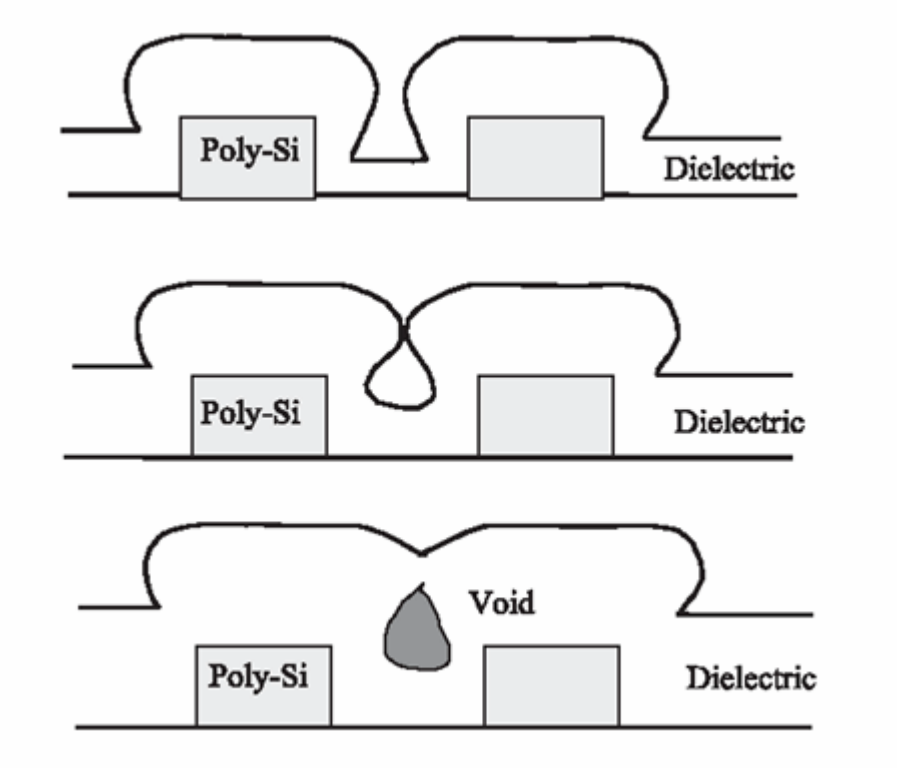
- Step coverage is a measurement of the deposited film reproducing the slope of a step on a substrate surface.
- Step coverage is determined by both the arriving angle and precursor mobility.
- At locations with large arriving angle, more precursor atoms/molecules will be adsorbed and will have more deposition.
- Step coverage related to pressure and mobility.




a. High pressure, low mobility; b. low pressure, low mobility; c. high mobility

# Void formation

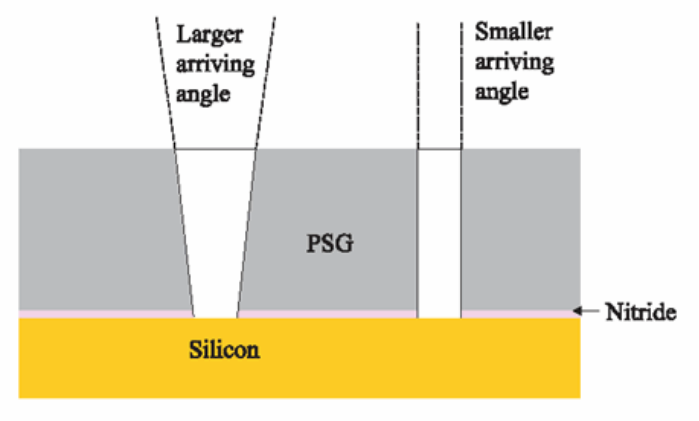
- Overhangs are not desirable.
- Overhangs may form voids in the dielectric film, causing device failures.



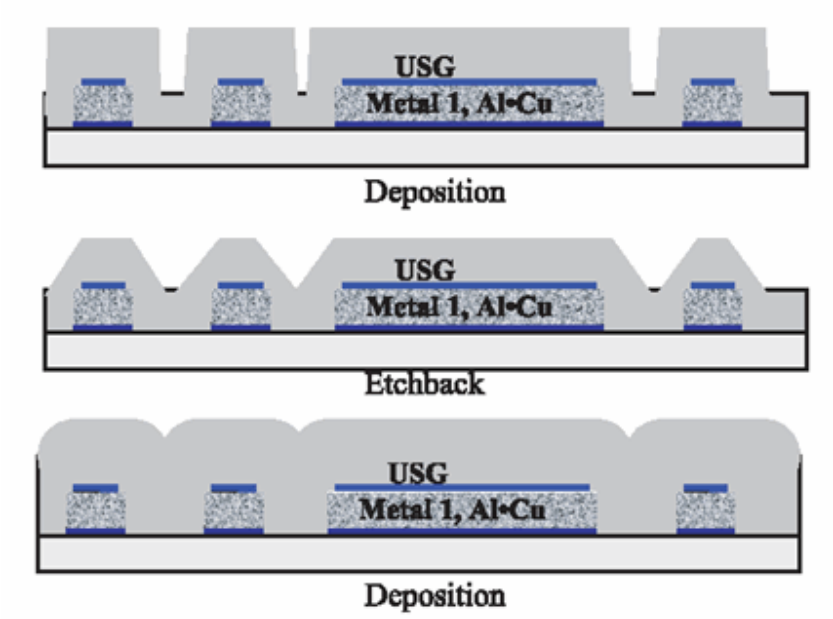

Void formation process

# Gap fill

- It's very important for CVD processes to fill gaps without voids.
- Due to arriving angle issue, high aspect ratio holes are hard to fill without voids.
- Methods developed:
  - Tapered hole
  - Deposition/etchback/deposition




Tapered hole for gap fill




Dep/etch/dep gap fill method

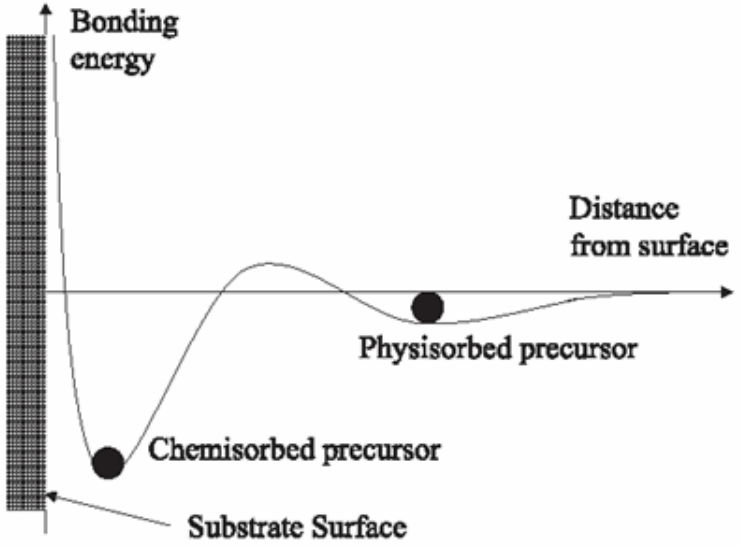
# CVD kinetics

# Surface adsorptions

- Two types of precursor adsorptions at the substrate surface:
  - Chemisorption
  - Physisorption

- Chemisorption – chemical adsorption where actual chemical bond is formed between an atom on the surface and an stom in the adsorbed precursor molecule.
  - Bond energy ~ 2 eV, very slow mobility

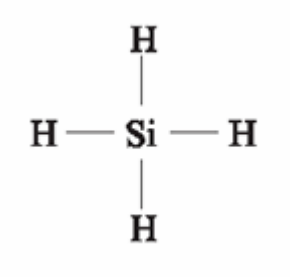
- Physisorption – physical adsorption where no chemical bond is formed.
  - Weak adsorption energy (< 0.5 eV); high mobility.



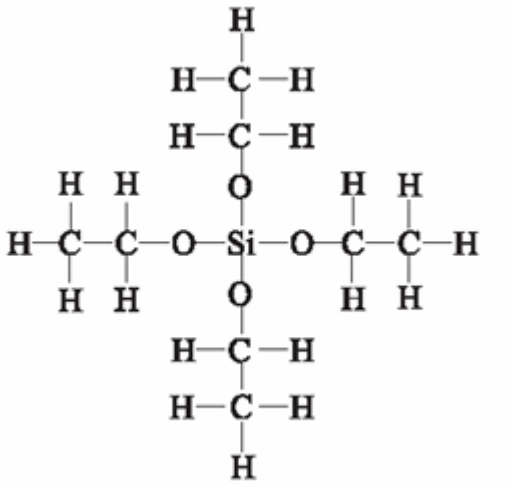

Relationship of bonding energy to chemisorption and physisorption

# CVD precursors and their adsorption

- Silane ($SiH_4$) – most commonly used silicon source for CVD
  - Very reactive, explosive and toxic
  - Silane free radicals are very reactive, and can readily chemisorb on substrate surface.  Mainly chemisorption.
  - Silane based precursors have very slow surface mobility
- TEOS [$Si(OC_2H_5)_4$] – commonly used CVD precursor for oxide deposition. It has a large organic molecule.
  - Mainly physisorption
  - Has high surface mobility
- 3MS (trimethylsilane) – for low-k ILD




Silane molecular structure

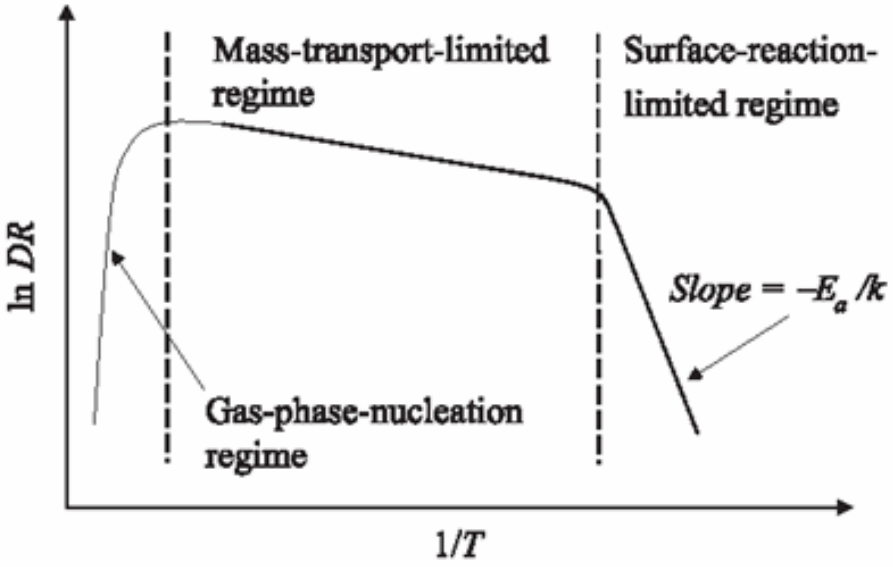


TEOS molecular structure

# CVD kinetics

- Surface-reaction-limited regime
  - Chemical reaction rate is slow, cannot match precursor diffusion and adsorption rates;
  - Precursors pile up on the surface waiting for reaction.
  - Deposition rate very sensitive to temperature.
- Mass-transport-limited regime
  - Chemical reaction rate is high enough that it waits for precursors to diffuse and adsorb on surface.
  - Deposition rate is controlled by the gas flow rate.
- Gas-phase-nucleation regime
  - No good! Needs to be avoided.

CVD deposition rate regimes



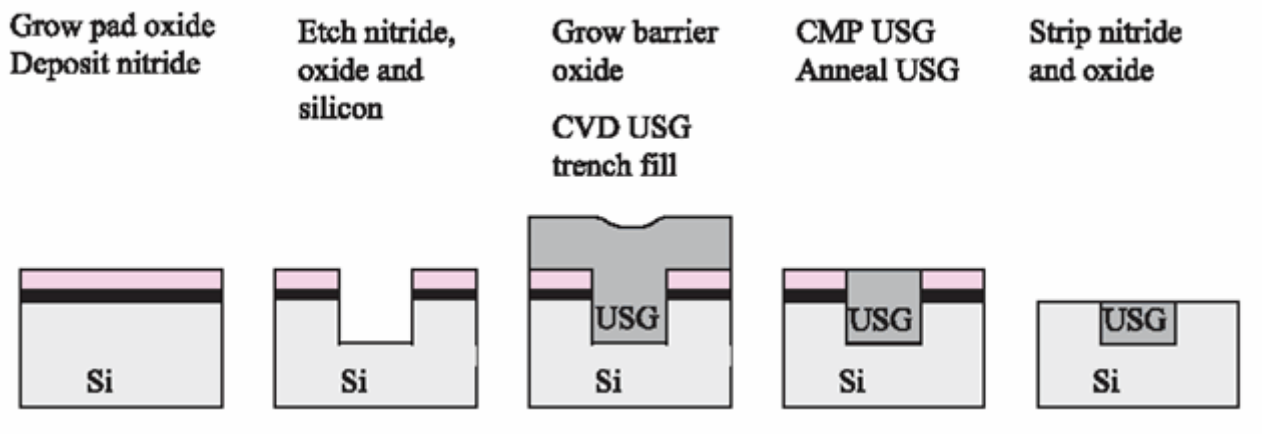
# CVD reactor deposition regime

- In surface-reaction-limited regime, deposition rate is controlled by temperature;
- In mass-transport-limited regime, deposition rate is controlled by precursor gas flow rate;
- Most single wafer CVD reactors are designed to operate in mass-transport-limited regime because it is easier to control gas flow rate than wafer temperature.

# Application of CVD dielectric thin films

# 1. Shallow trench isolation (STI)

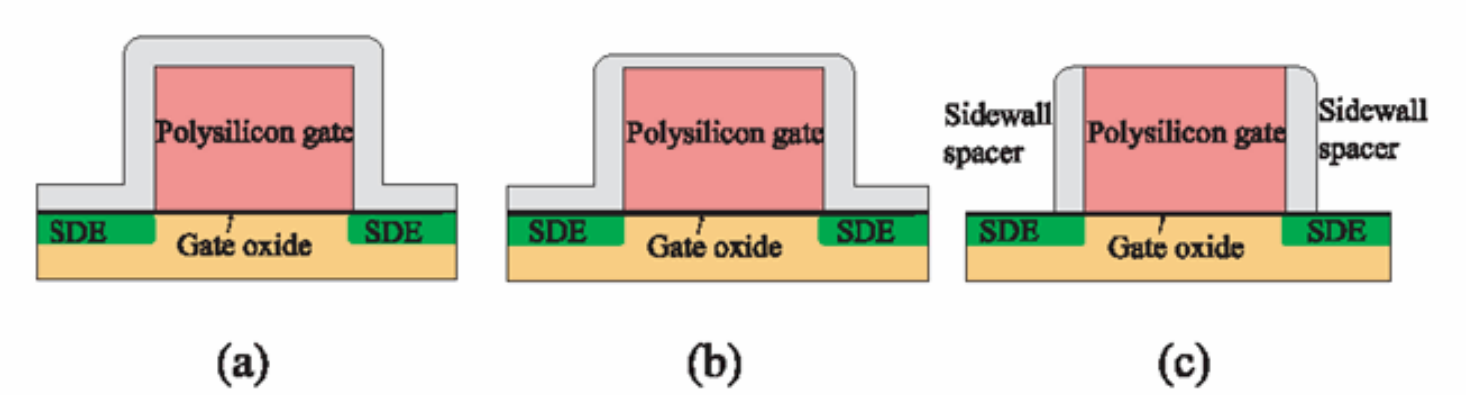
- STI is used for isolation between neighboring transistors.
- Undoped silicate glass (USG) is used for STI fill.
- Requirements for CVD film for STI are void-free gap fill and dense film.
- TEOS is a common precursor for STI CVD




Processing steps for a STI

# 2. Sidewall spacer

- Sidewall spacers are used to suppress the hot carrier effects and to provide a diffusion buffer for dopant atoms in a S/D.
- Can use LPCVD nitride as sidewall spacer.
- Requirement of the dielectric film is high step coverage, not too high temperature (limited by thermal budget).




Sidewall spacer formation: a). Dielectric film deposition; b). Etch back; c). Spacer formation

# 3. Interlayer dielectric-0

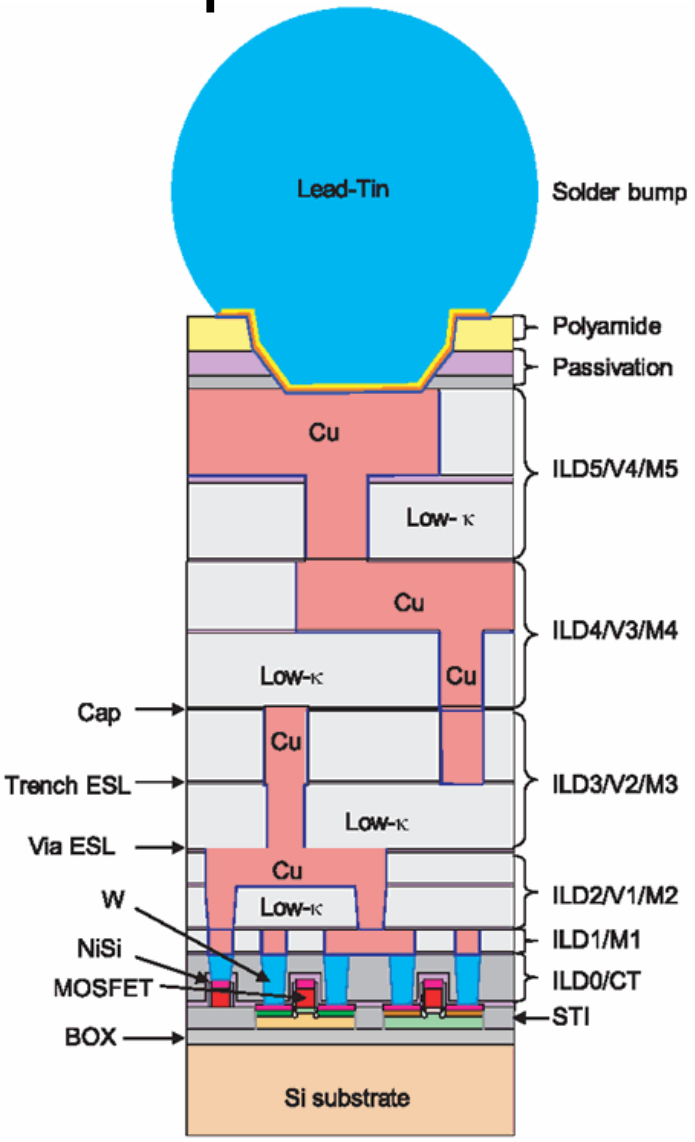
- ILD0 is the first dielectric layer deposited on a wafer surface after transistors have been created.

- ILD0 requirements: low dielectric constant, void-free gap fill, good planarization.  Depositing temperature within thermal budget.

- Common ILD0 material: phosphorus-doped silicate glass (PSG) or phosphorus- and boron-doped silicate glass (BPSG).

# 4. Interlayer dielectric-1 and up

- Up to 10 ILD dielectric layers in a modern IC chip.
- Requirements of ILD are low dielectric constant, void-free gap sill, and planarization of the surface.
- Typical ILD deposition temperature to be ~ 400 °C due to the device thermal budget



# 5. Passivation dielectrics

- PD is to protect the IC chip from moisture and mobile ions in the environment, in addition to mechanical protection.

- PD requirements:
  - High dielectric strength
  - High mechanical strength

- Common PD material
  - PECVD grown silicon nitride

- PD deposition temperature:
  - ~ 400 °C due to metal line limitations.

# CVD film properties

# Film shrinkage

- Thermal cycle – Heating up a wafer and cooling it back to room temperature is called a thermal cycle.

- After a thermal cycle, film thickness usually decreases. The amount of shrinkage indicates the original film quality.

  Shrinkage = (thickness change after thermal cycle)/(original film thickness)

- Shrinkage is one of the major concerns for oxide film for STI application.

# Stress

- Stress in dielectric films are due to material mismatch or difference in coefficients of thermal expansion (CTE).
- Films stress can be compressive or tensile.
- High stress on the dielectric film can cause film cracking, metal line spiking, void formation, or even break wafers.

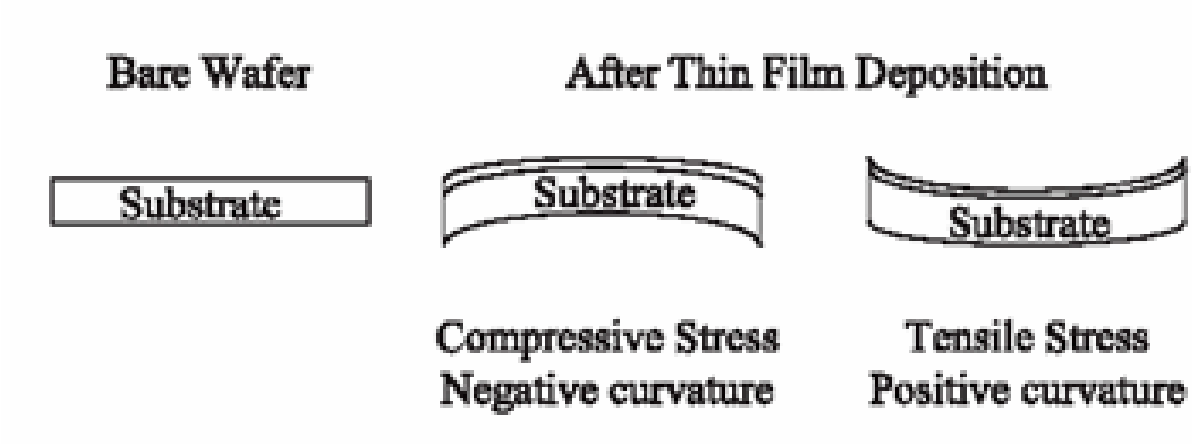



Illustration of the film compressive and tensile stresses

# Stress example

- Thermal expansion of material:

$$\Delta L = \alpha \Delta T L$$

- Si has higher CTE than $SiO_2$
- After cooling back to room temperature, the $SiO_2$ film has a compressive stress.

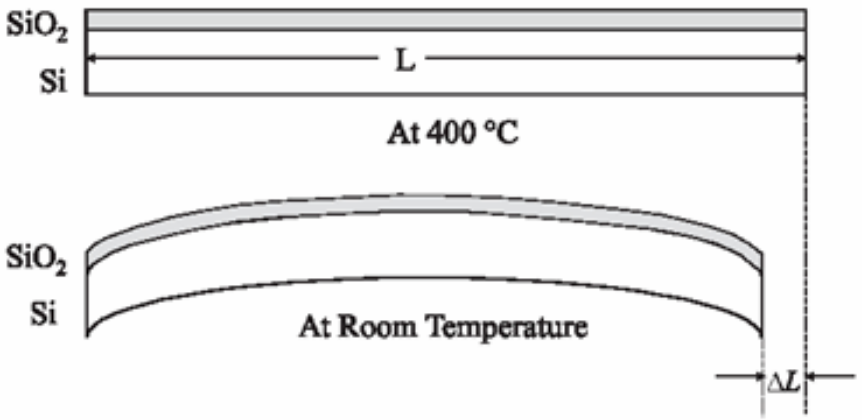



**Table 10.7** Coefficients of thermal expansion (in $10^{-6}$ °$C^{-1}$).

| | |
|---|---|
| $\alpha(SiO_2) = 0.5 \times 10^{-6}$ °$C^{-1}$ | $\alpha(W) = 4.5 \times 10^{-6}$ °$C^{-1}$ |
| $\alpha(Si) = 2.5 \times 10^{-6}$ °$C^{-1}$ | $\alpha(Al) = 23.2 \times 10^{-6}$ °$C^{-1}$ |
| $\alpha(Si_3N_4) = 2.8 \times 10^{-6}$ °$C^{-1}$ | $\alpha(Cu) = 17 \times 10^{-6}$ °$C^{-1}$ |

# Dielectric CVD process Reactions

- Two common processes:
  - Thermal CVD – APCVD, LPCVD
  - PECVD

- Common Precursors:
  - Silane for nitride and oxide
  - TEOS for oxide
  - 3MS for low-k dielectric

# Thermal silane CVD process

- Silane is used as precursor for dielectric silicon dioxide CVD processes, both in APCVD and LPCVD reactors.

$$SiH_4 + 2O_2 \xrightarrow{\text{heat}} SiO_2 + 2H_2O$$

- APCVD uses diluted silane (3% in nitrogen) and LPCVD uses pure silane.

- LPCVD silane oxide has higher throughput and better step coverage.

# Thermal TEOS CVD process

- Tetraethoxysilane (TEOS) oxide film has better step coverage and conformity due to TEOS molecule's high surface mobility.
- At high temperature (~ 700 °C), TEOS will dissociate and form silicon dioxide:

$$Si(OC_2H_5)_4 \rightarrow SiO_2 + \text{volatile organics}$$

- LPCVD reactor operated at ~ 700 °C is use.
- This TEOS CVD process is used to deposit sidewall spacers and for BPSG ILD0 layer.

# Plasma-enhanced CVD silane process

- PECVD reactor is used.
- Two precursor gases: Silane as the Si source, and $N_2O$ as the oxygen source.

$$SiH_4 + N_2O \rightarrow SiO_2 + H_2O + N_2 + NH_3 + \ldots$$

- The PECVD saline oxide process has three main steps:
  - Stabilization (~ 5 sec) – to stabilize the pressure and gas flow rate.
  - Deposition – Not change in pressure and gas flow rate. RF power is on.
  - Chamber pump down – RF power, gas flows all off. Deposition stopped. Prepared for next process.

PECVD saline process example:

| Step 2 | Deposition |
|---|---|
| Pressure (torr) | 3.0 |
| Temperature (°C) | 400 |
| rf (W) | 250 |
| $SiH_4$ flow (sccm) | 120 |
| $N_2O$ flow (sccm) | 2400 |

*(sccm = standard cubic centimeter per minute)*

# PECVD silane process for passivation

- Silicon nitride is a very good barrier layer for moisture and mobile ions and is widely used as the final passive layer.
- PECVD nitride at low temperature (< 450 °C) is used.
- Two precursors: silane as Si source, and ammonia as nitrogen source, and $N_2$ as the carrier gas and the 2$^{nd}$ nitrogen source.

$$SiH_4 + N_2 + NH_3 \rightarrow Si_3N_4 + H_2 + N_2 + NH_3 + \ldots$$

- The passivation nitride requires good step coverage, high deposition rate, good uniformity and good stress control.
- PECVD silane passive dielectric deposition processes have the following steps: stabilization 1; oxide deposition; pumping; stabilization 2; nitride deposition; plasma purging; chamber purging.

# PECVD TEOS processes for ILD layers

- PECVD TEOS processes operated at low temperature (~ 400 °C) are widely used for ILD dielectric layers.
- Chemical reactions:

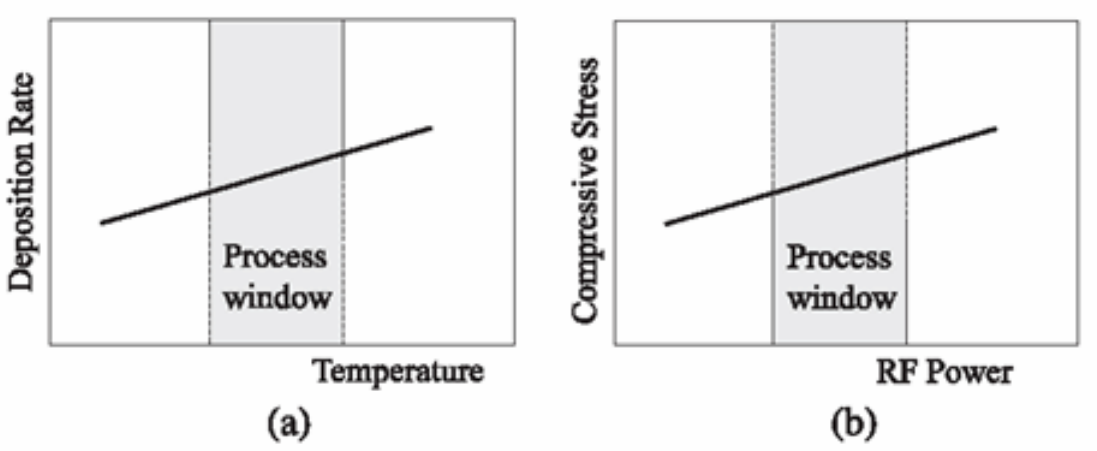
$$Si(OC_2H_5)_4 + O_2 \xrightarrow{\text{heat, plasma}} SiO_2 + \text{other volatiles}$$

- PE-TEOS oxide film has very good step coverage and conformality due to TEOS precursors high mobility (physisorbed).
- PE-TEOS can also be used to deposit PSG and BPSG for ILD0 applications.

# PECVD process trends

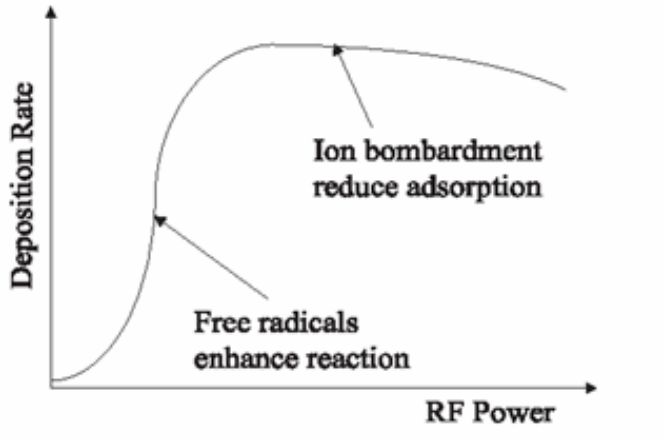
# Silane PECVD process trends

- Increasing the process temperature always increases the deposition rate.
- Increasing temperature also improve film step coverage and quality.
- Increasing RF power will increase compressive stress. (because high RF power increases ion density and energy during bombardment).
- Prefer to operate at high RF power regime (at mass-transport-limited regime); Silane precursor molecule is chemisorption.









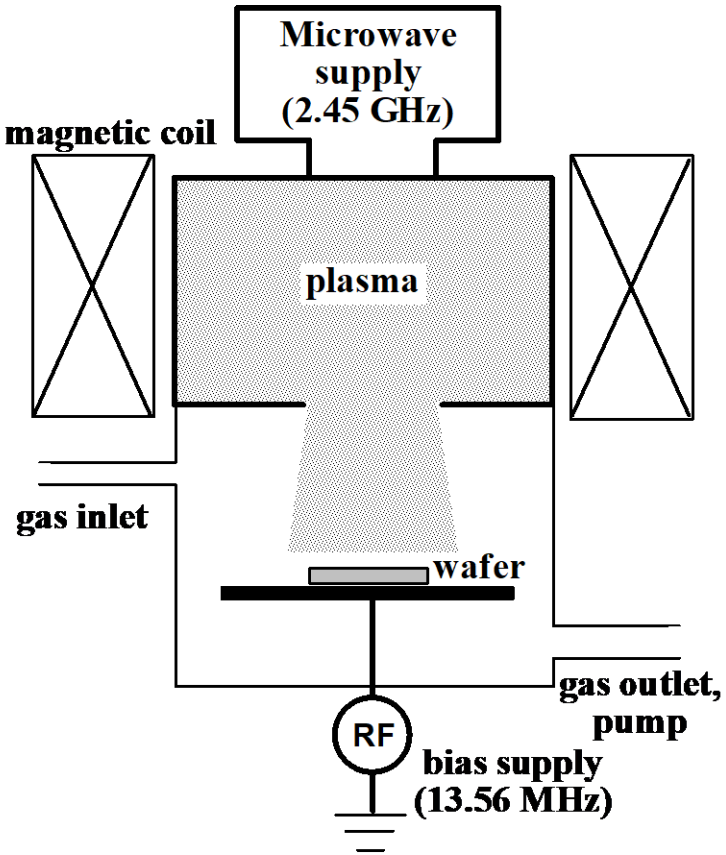
# Examples of PECVD systems and applications

| Material Deposited | Common Precursors | Deposition Temp. °C | Applications | Status |
|---|---|---|---|---|
| a-Si | $SiH_4$-$H_2$ | 250 | semiconductor photovoltaic | production |
| Epitaxial silicon | $SiH_4$ | 750 | semiconductor | R & D |
| $Si_3N_4$ | $SiH_4$-$N_2$-$NH_3$ | 300 | passivation | production |
| $SiO_2$ | $SiH_4$-$N_2O$ | 300 | passivation optical fiber decorative | production |
| Boro-phospho-silicate | $SiH_4$-TEOS-$B_2H_6$-$PH_3$ | 355 | passivation | semi-production |
| W | $WF_6$ | 250–400 | conductor in IC's | R & D |
| $WSi_2$ | $WF_6$-$SiH_4$ | 230 | conductor in IC's | semi-production |
| $TiSi_2$ | $TiCl_4$-$SiH_4$ | 380–450 | conductor in IC's | semi-production |
| TiC | $TiCl_4$-$C2H_2$ | 500 | abrasion cutting tools | R & D |
| TiN | $TiCl_4$-$NH_3$ | 500 | abrasion cutting tools | R & D |
| Diamond-like carbon | $CH_4$-$H_2$ hydrocarbon | 300 | wear, erosion, optical | semi-production |

**PECVD Films, Source Gases, and Deposition Temperatures**

| Film | Source gases | Deposition temperature (°C) |
|---|---|---|
| Elemental | | |
| Al | $AlCl_3$–$H_2$ | 100–250 |
| a-B | $BCl_3$–$H_2$ | 400 |
| a-C | $C_nH_m$–$H_2$/Ar | 25–250 |
| a-Si | $SiH_4$–$H_2$ | 300 |
| c-Si | $SiH_4$–$H_2$ | 400 |
| Oxides | | |
| $Al_2O_3$ | $AlCl_3$–$O_2$ | 100–400 |
| $SiO_2$ | $SiCl_4$–$O_2$ | 100–400 |
| $TiO_2$ | $TiCl_4$–$O_2$ | 100–500 |
| Nitrides | | |
| AlN | $AlCl_3$–$N_2$ | <1000 |
| BN | $B_2H_6$–$NH_3$ | 300–700 |
| | $BCl_3$–$NH_3$/Ar | 300–700 |
| $Si_3N_4$ | $SiH_4$–$NH_3$–$N_2$ | 25–500 |
| TiN | $TiCl_4$–$N_2$–$H_2$ | 100–500 |
| Carbides | | |
| $B_4C$ | $B_2H_6$–$CH_4$ | 400 |
| BCN | $B_2H_6$–$CH_4$–$N_2$ | ~25 |
| | $C_8H_{18}BN$ | 250 |
| SiC | $SiH_4$–$C_nH_m$ | 140–600 |
| TiC | $TiCl_4$–$CH_4$–$H_2$ | 400–900 |
| Borides | | |
| $TiB_2$ | $TiCl_4$–$BCl_3$–$H_2$ | 480–650 |

# High Density Plasma (HDP) CVD




- High density plasma CVD gives dense layers ($SiO_2$) at low T (150 °C) and low P (1- 10 mTorr); T increases to 400°C by bombardment.
- Separate RF (gives substrate biasing for bombardment) from plasma generation (electron cyclotron resonance ECR and inductively coupled plasma ICP).
- Simultaneous deposition and sputtering/ bombardment. Improved planarization and filling due to preferential sputtering of sloped surface. Mostly used for $SiO_2$ deposition in backend processes.

# Miscellaneous: selective deposition and laser CVD

Selective deposition:

- Especially important in microelectronics, surface patterning and 3D-growth.
- Reaction rate of precursor is limited on a non-growth surface. E.g. deposition of Cu from (hfac)Cu($PMe_3$) occur on Cu, Pt… but not on $SiO_2$.
- Growth surface acts as co-reactant, and is selectively consumed. E.g. Si reacts with $WF_6$ or $MoF_6$, while reaction at $SiO_2$ or $Si_3N_4$ is slower.
- A chemical reaction of a gaseous co-reactant occur on the growth surface. E.g. $H_2$ dissociation

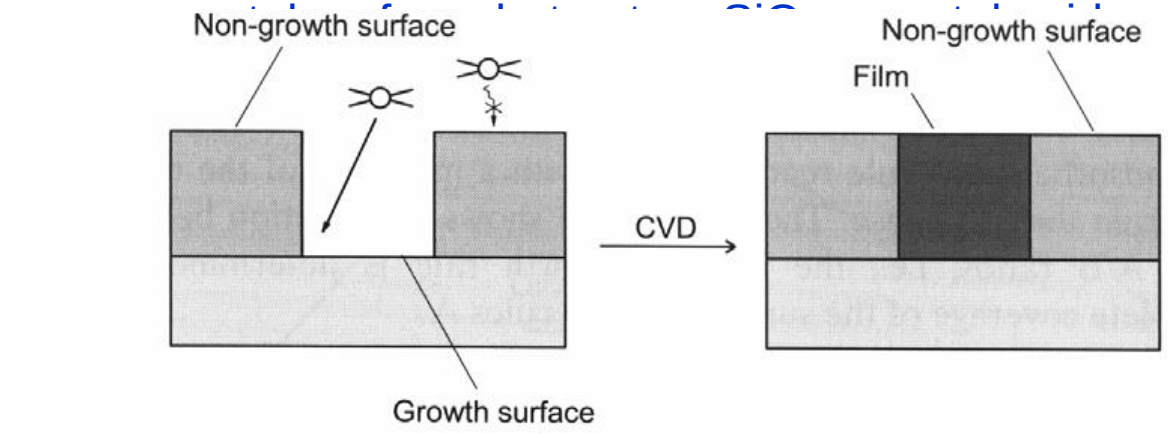
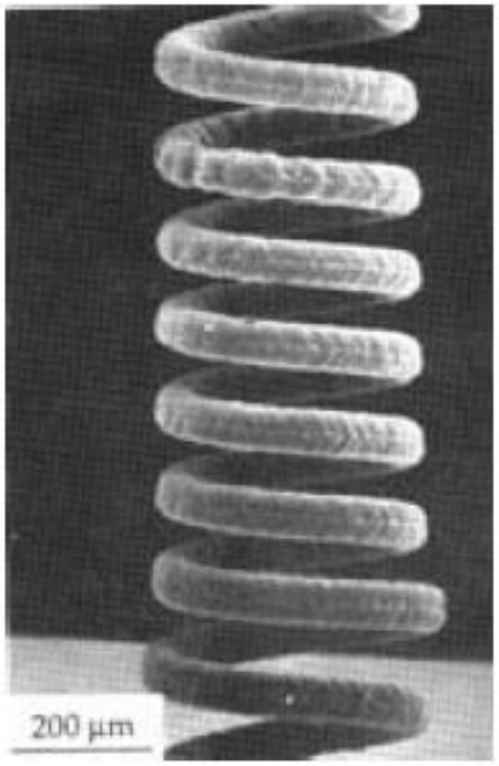



**Figure 3-11.** Selective deposition by CVD.

## Laser CVD

(energy provided by laser)




Tungsten spring grown by laser CVD.

# CVD reactor types: quick summary

- **Chamber pressure:**
  - atmospheric-pressure (APCVD)
  - low-pressure
    - * LPCVD
    - * PECVD
- **Reactor heating:**
  - Hot-wall
  - Cold-wall

**Reaction Mechanism**

- mass transport, when *P* and *T* are high
- surface reaction, when *P* and *T* are low
- possible to switch from one to another by changing *P* or *T*

**APCVD**

± mass-transport limited region
\+ fast deposition
– poor step coverage

**LPCVD**

± surface reaction rate limited
\+ excellent purity, uniformity and step coverage
– low deposition rates
– requires vacuum system

**Cold-wall**

\+ no reaction on the wall
– difficult to control the real T

**Hot-wall**

– particle contamin. (peel off)
– requires periodic cleanup

- In APCVD reactive gas *partial* pressure could be set much higher than that in LPCVD.
- Its pressure could be much lower (by 10×) than 1atm and is still called APCVD.
- Gas transport actually increases with T as $T^{3/2}$ (APCVD is usually done at higher T than LPCVD).
- When putting wafer side-by-side facing the gas, more exposed to gas, thus faster transport.