Lecture 12: Metallization

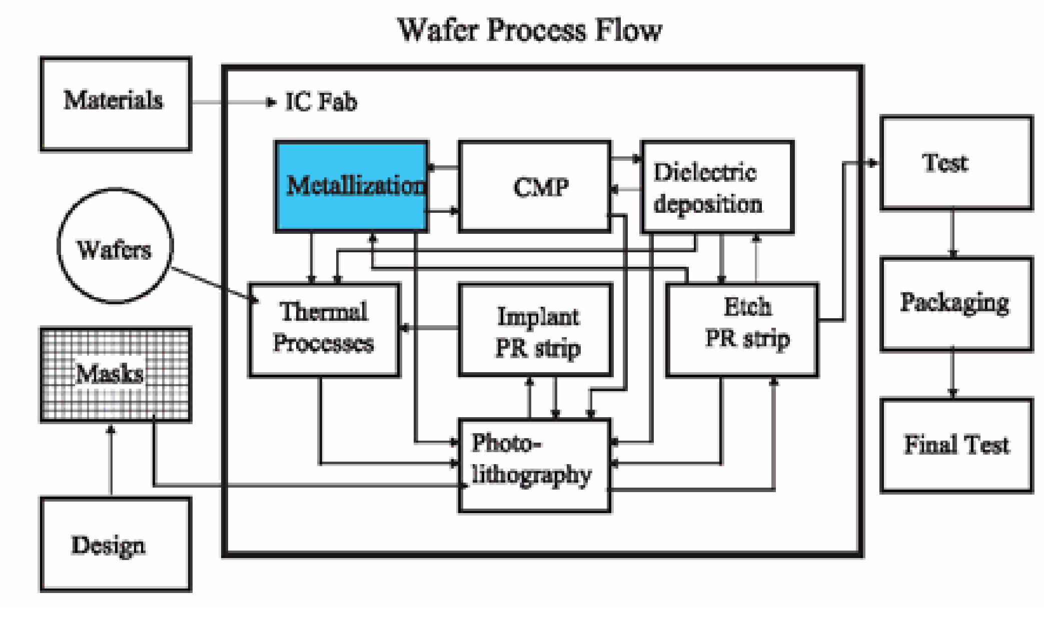
- Contents:
  - Introduction
  - Common conducting films in an IC chip
  - Metal thin-film characteristics
  - Metal CVD
  - Physical vapor deposition (PVD)
  - CMP

Reference Book: "Introduction to semiconductor manufacturing technology", by Xian, Hong, SPIE, 2nd edition, 2012

Introduction

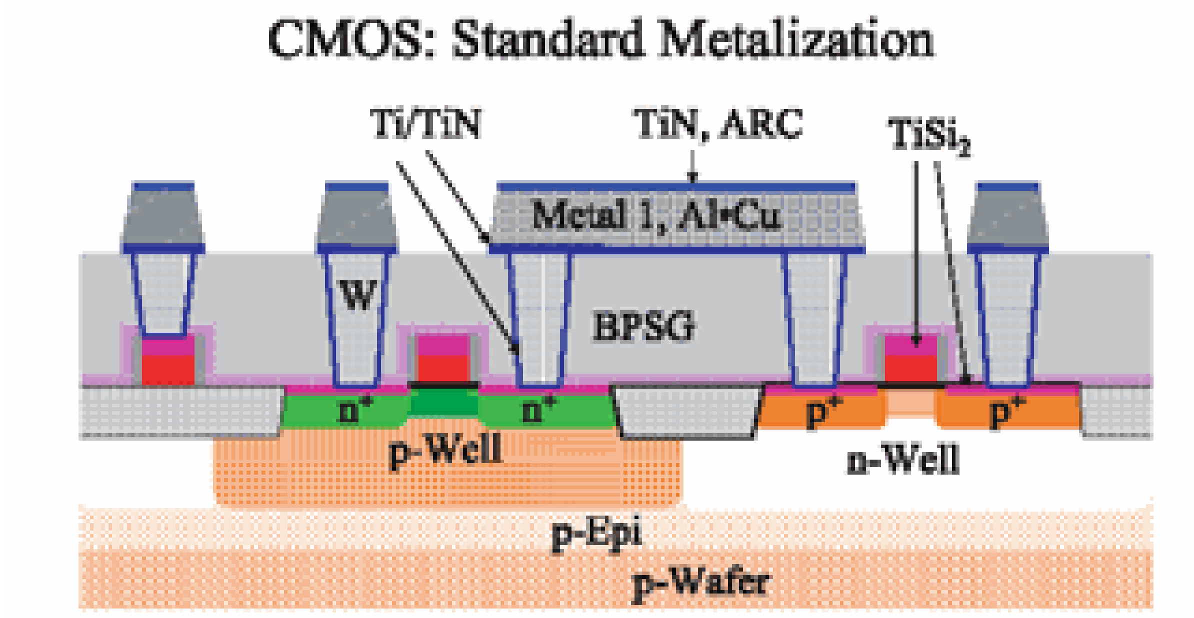
Metallization

- Metallization is an adding process that deposit metal layers on a wafer surface.
- Requirements for metallization are:
  - Low resistivity (less power consumption and less RC delay)
  - Smooth surface (for high resolution patterning)
  - High electro-migration resistance (for chip high reliability)
  - Low film stress (for good adhesion to underline substrates)



Chips with Al-Cu interconnection

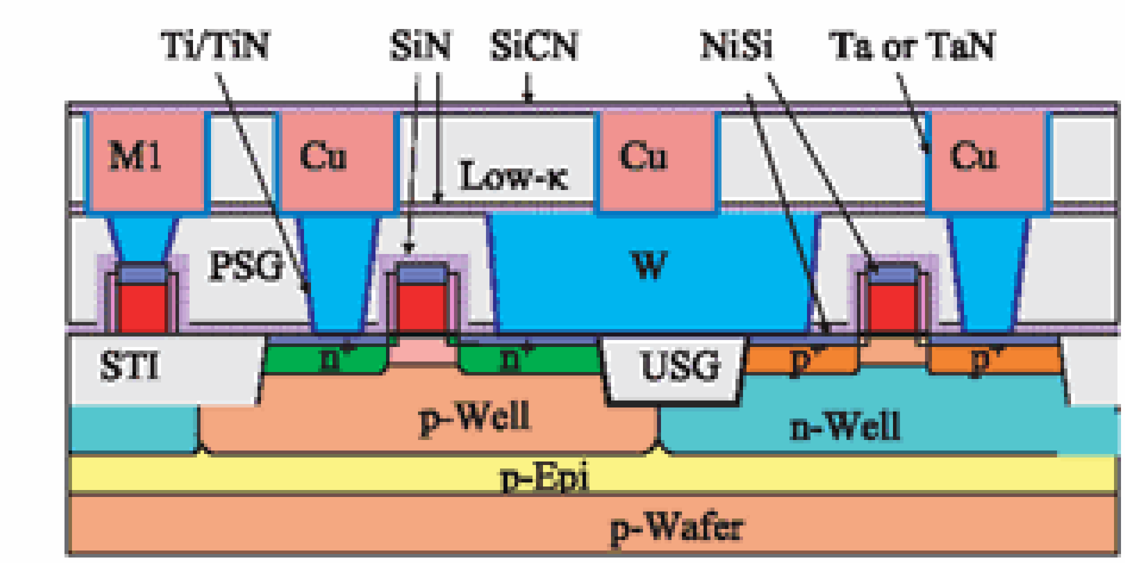
- Al-Cu for interconnection
- Tungsten (W) to fill the via holes
- Titanium (Ti) and titanium nitride (TiN) as barrier/adhesion layer



Cross-section of an IC chip with Al-Cu interconnection

Chips with Cu interconnection

- Copper (Cu) interconnection
- Tantalum (Ta) and tantalum nitride (TaN) as the barrier layer
- Silicon nitride (SiN) or silicon carbon nitride (SiCN) as barrier and cap layers to isolate the Cu layer to prevent it from diffusing into the Si substrate.



Cross-section of an IC chip with Cu interconnection and low-k ILD

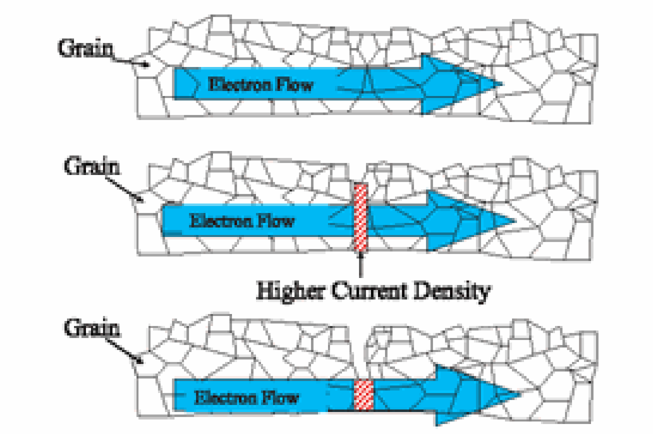
Common conducting thin films in IC chips

Polysilicon and silicides

- Polysilicon as the transistor gate
  - Titanium silicide ($TiSi_2$) and tungsten silicide (WSi_2) to improve gate conductivity.

Aluminum (Al)

- Aluminum (Al) and Al-Cu – once the most commonly used metal in IC chips
  - Good conductivity (after Au, Ag and Cu).
  - Electromigration – Electron bombardments cause some grains to move, resulting in large cracks in the wire with large current density at the remaining connection.
  - Cu is added in Al to avoid electromigration. ➔ Al-Cu

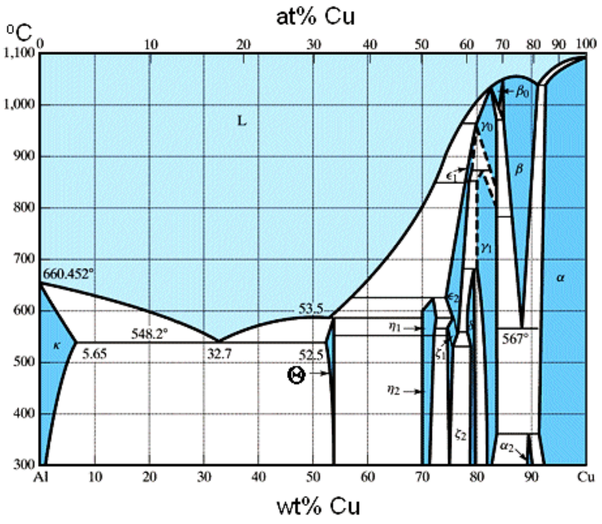


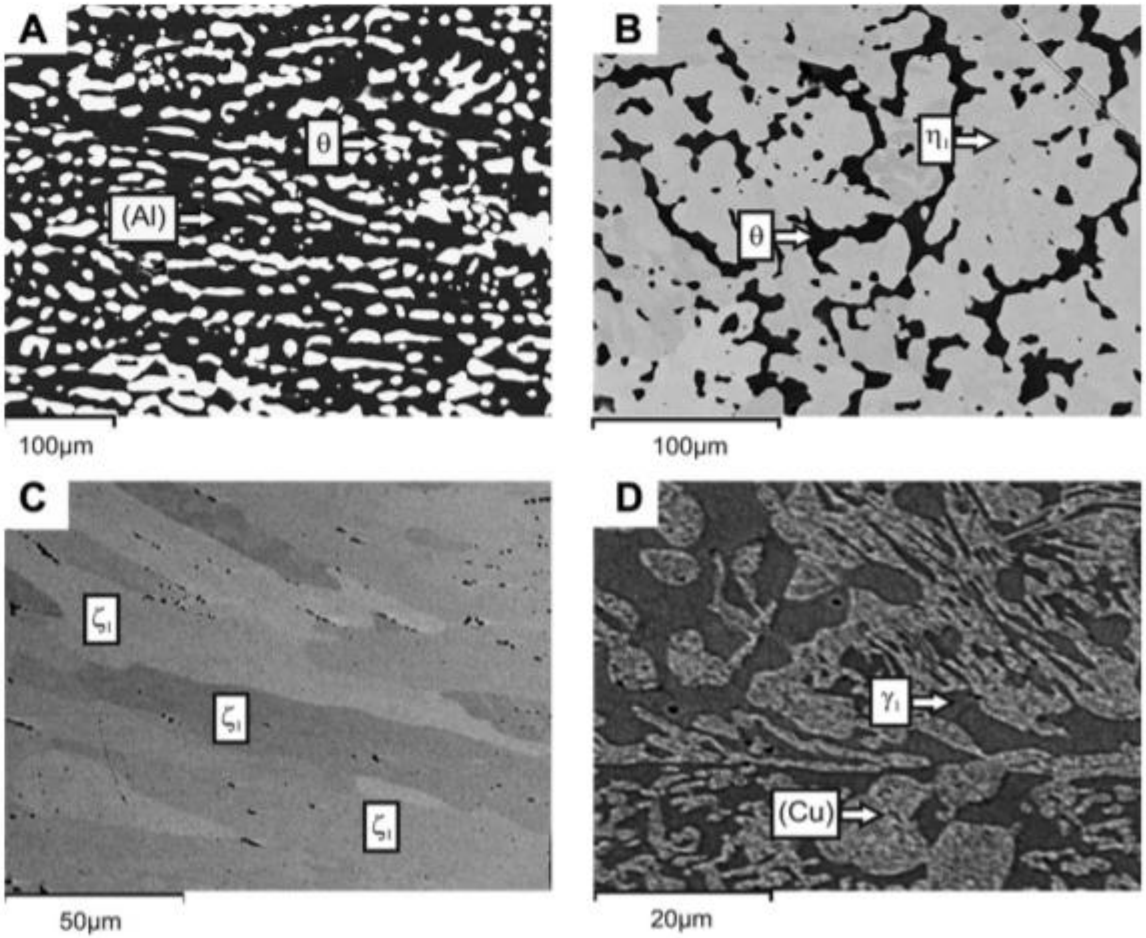
Electromigration in Aluminum

Aluminum basics

Name	Aluminum
Symbol	Al
Atomic number	13
Atomic weight	26.98
Density of solid	2.70 g/cm3
Hardness	2.75
Reflectivity	71%
Resistivity	2.65 $\mu\Omega$.cm
Melting point	660 °C
Boiling point	2519 °C
Thermal conductivity	235 W/mK
Coefficient of thermal expansion	$23.1\text{x}10^{-6}K^{-1}$

Cu-Al alloy





Al stays at the grain boundary to prevent Cu to move, thus helps EM

Titanium and titanium nitride

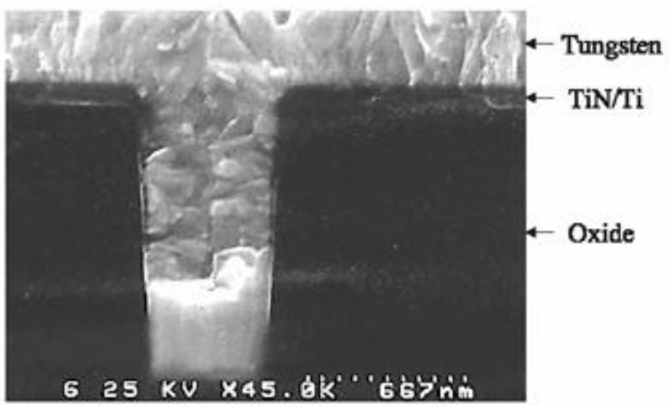
- Titanium and titanium nitride
  - Widely used as a welding layer for tungsten and aluminum to reduce contact resistance
  - TiN as diffusion barrier for W-plugs and for the local interconnections, prevent it from diffusing into oxide and silicon.
  - TiN film is also used as an adhesion layer or an antireflection coating.

Titanium basics

Name	Titanium
Symbol	Ti
Atomic number	22
Atomic weight	47.867
Density of solid	4.507 g/cm3
Hardness	6.0
Resistivity	40 μΩ.cm
Melting point	1668 °C
Boiling point	3287 °C
Thermal conductivity	22 W/mK
Coefficient of thermal expansion	8.6x$10^{-6}K^{-1}$

Tungsten (W)

- Tungsten (W):
  - For filling contact holes and serve as contact vias between metal layers
  - Form plugs that connect the metal layer and the silicon substrates
  - W is deposited during CVD process, with WF_6 as precursor



Tungsten plug and TiN/Ti barrier/adhesion layer

Tungsten basics

Name	Tungsten
Symbol	W
Atomic number	74
Atomic weight	183.84
Density of solid	19.25 g/cm3
Hardness	7.5
Reflectivity	62%
Resistivity	5 $\mu\Omega$.cm
Melting point	3422 °C
Boiling point	5555 °C
Thermal conductivity	170 W/mK
Coefficient of thermal expansion	$4.5\text{x}10^{-6}K^{-1}$

Copper (Cu)

- Cu is used for interconnections.
- Cu has low resistivity and better resistance to electromigration than Aluminum or Al-Cu.
- But Cu has a high diffusion rate in Si and in SiO_2, and Cu diffusion will cause heavy metal contamination that can fail the device.
- Also, it is difficult to dry etch Cu.
- Cu became popular only after the copper chemical mechanical polishing (CMP) technology is developed.

Copper basics

Name	Copper
Symbol	Cu
Atomic number	29
Atomic weight	63.546
Density of solid	8.92 g/cm3
Hardness	3.0
Reflectivity	90%
Resistivity	1.7 $\mu\Omega$.cm
Melting point	1084.77 °C
Boiling point	5555 °C
Thermal conductivity	400 W/mK
Coefficient of thermal expansion	$16.5\text{x}10^{-6}K^{-1}$

Tantalum (Ta)

- Used as a barrier layer for copper to prevent copper from diffusing across SiO_2 into silicon substrate and cause device damage.
- Ta is a better barrier material for copper.
- Ta is deposited with a sputtering process.

Tantalum basics

Name	Tantalum
Symbol	Ta
Atomic number	73
Atomic weight	180.9479
Density of solid	16.654 g/cm3
Hardness	3.0
Reflectivity	90%
Resistivity	12.45 μΩ.cm
Melting point	2996 °C
Boiling point	5425 °C
Thermal conductivity	57.5 W/mK
Coefficient of thermal expansion	$6.3\text{x}10^{-6}K^{-1}$

Cobalt (Co)

- Cobalt is mainly used to form cobalt silicide ($CoSi_2$) for gate and local interconnections.
- Mainly for CMOS logic device with 180- to 90-nm technology nodes.
- Cobalt is deposited with sputtering process.

Cobalt basics

Name	Cobalt
Symbol	Co
Atomic number	27
Atomic weight	180.9479
Density of solid	8.900 g/cm3
Hardness	6.5
Reflectivity	67%
Resistivity	13 $\mu\Omega$.cm
Melting point	1768 °C
Boiling point	3200 °C
Thermal conductivity	100 W/mK
Coefficient of thermal expansion	$13.0\text{x}10^{-6}K^{-1}$

Nickel

- Nickel is used to form nickel silicide (NiSi) for CMOS logic devices.
- To reduce the resistance of S/D contacts and local gate interconnections
- Main application is for 65nm and smaller nodes.
- NiSi formation needs lower temperature than other silicides, suitable for smaller nodes and lower thermal budgets.
- It is deposited using sputtering process.
- Nickel is a magnetic material.

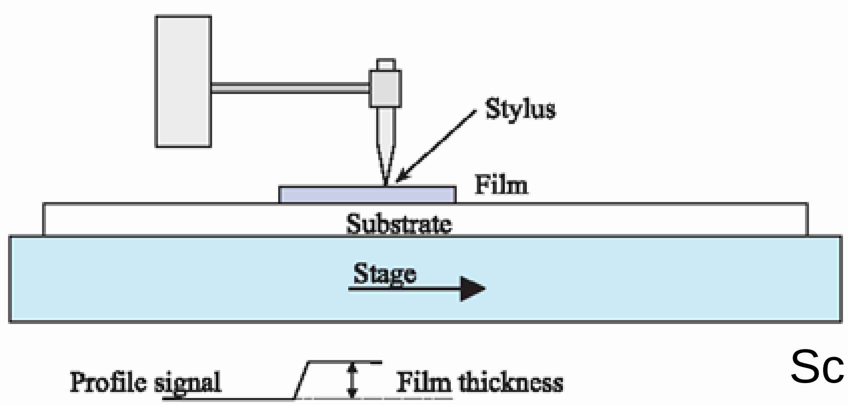
Nickel basics

Name	Nickel
Symbol	Ni
Atomic number	28
Atomic weight	58.693
Density of solid	8.908g/cm3
Hardness	4.0
Reflectivity	72%
Resistivity	7.2 $\mu\Omega$.cm
Melting point	1455 °C
Boiling point	2913 °C
Thermal conductivity	91 W/mK
Coefficient of thermal expansion	13.4x$10^{-6}K^{-1}$

Metal thin-film characteristics

Thickness and deposition rate

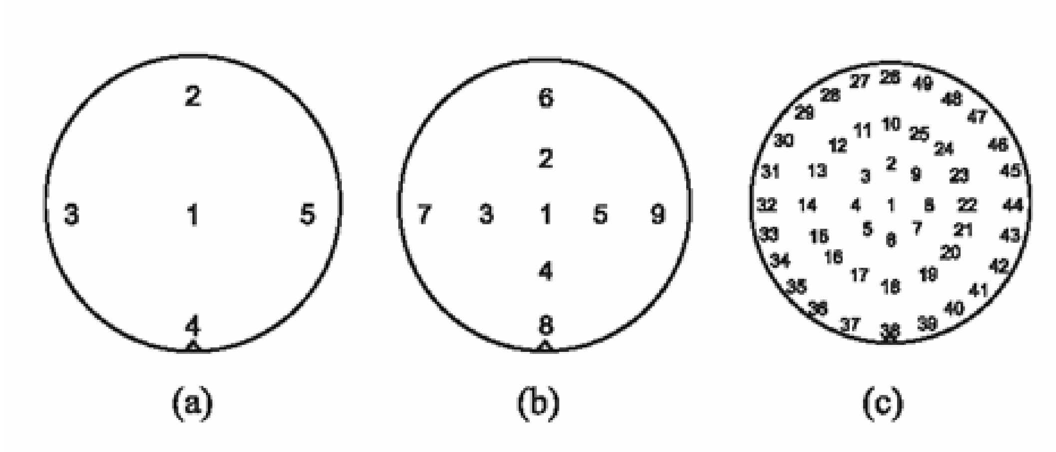
- Metal thin films are opaque.
- Metal thin films have polycrystalline structures.
- Common thickness measurements methods:
  - Cross-section SEM measurements
    - Accurate, destructive, expensive
  - Profilometer measurements
    - Needs test patterns to measure
    - Accuracy is limited
  - A four-point probe method
    - Indirect measurements
    - Assuming the resistivity of the film is constant over the entire wafer surface



Schematic of a profilometer

Uniformity

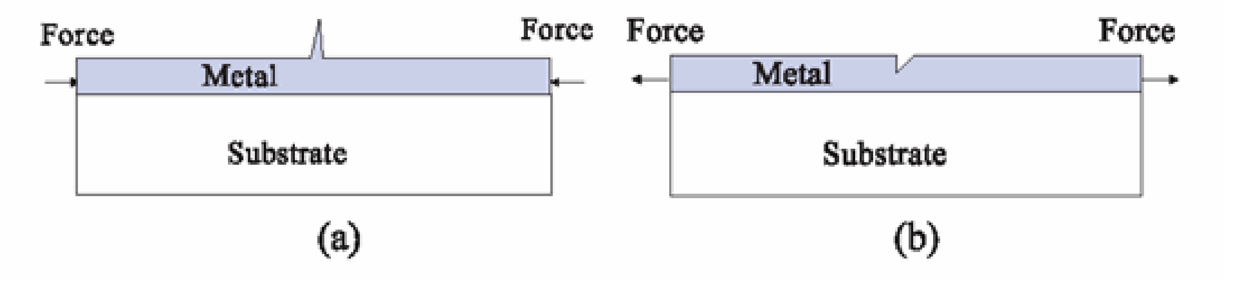
- Uniformity of the thickness, sheet resistance are routinely measured during process development and process monitoring.
- It can typically be calculated from multiple measurements from a wafer – sampling.
- 3σ standard deviation nonuniformity is the most commonly used definition for film nonuniformity.



Sampling pattern for uniformity measurements: a). 5-point; b). 9-point; c). 49-point

Stress

- Stress is due to material mismatch between a film and the substrate.
- Two types of stress: compressive and tensile.
- High compressive stress can cause film to form hillocks that may short metal wires between different layers.
- High tensile stress can cause the film to crack for peel.
- Stress can be measured from the change of wafer curvatures before and after thin-film deposition.



Defects caused by film high stresses: a). Hillock due to compressive stress; b). Crack due to tensile stress.

Reflectivity

- Reflectivity is a function of film grain size and surface smoothness. Small grain size, smooth surface ➔ higher reflectivity.
- For a stable metallization process, reflectivity of the deposited film should be a constant.
- A change in reflectivity indicates a drifting of process condition.
- Reflectivity can be measured by focusing a light beam on a film surface and then measuring the intensity of the reflected beam.
- Film reflectivity results use the value relative to silicon.
- Reflectivity is very important to photolithography resolution because it can cause standing wave effect. ARC (Anti reflective Coating) is required for metal patterning process due to high reflectivity.

Sheet resistance

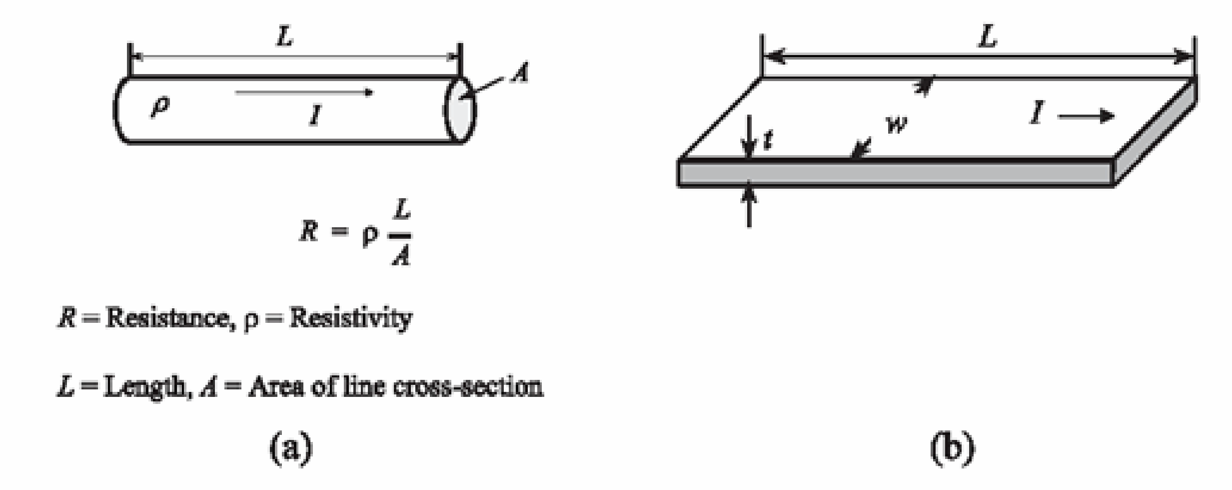
- Sheet resistance is the most important property of a conducting film.
- Sheet resistance definition:

  For a metal line, resistance $R = \rho\ L/A$

  If the cross-section is rectangle, $A = wt$, then $R = \rho\ L/wt$

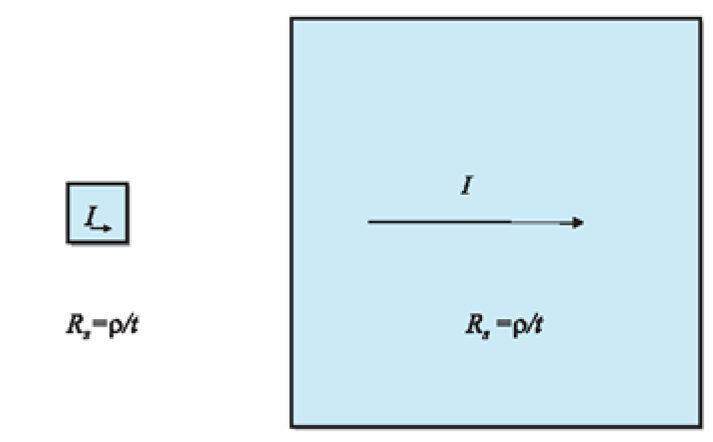
  For a square sheet, $L=w$, then $R = \rho/t$ ➔ define it as R_s
- Sheet resistance is the resistance of a square conducting sheet:

  $R_s = \rho/t$ (unit: ohms per square)



Q&A

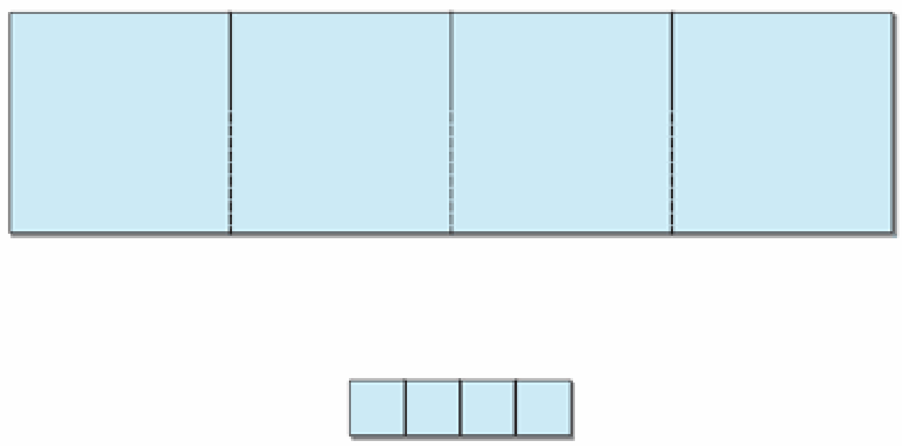
Q: Compare the resistance of the two square with the same uniform thickness: a). 1 um square; b). 1 inch square?



A: The same. For both $R = R_s = \rho/t$

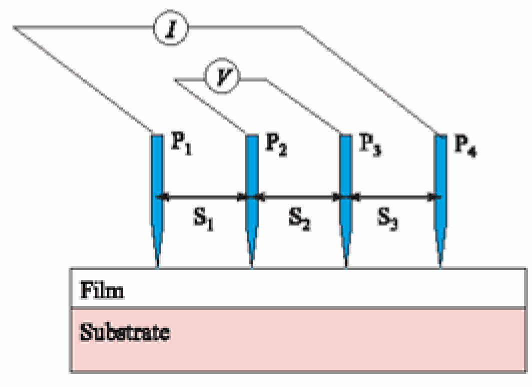
Q&A

- Q: For two conducting lines patterned from the same thin metal film with the same length-to-width ratios, are their line resistances the same?
- A: Yes. Both lines are consistent with the same number of square sheet resistors in serial connection. Each has the same sheet resistance.



Sheet resistance measurement

- Four-point probe method is the most common.
- Four-point probe:
  - Applying current "I" between P1 and P4, measuring voltage "V" from P2 and P3, then **Rs = 4.53 V/I**
  - Applying current "I" between P1 and P3, measuring voltage "V" from P2 and P4, then **Rs = 5.75 V/I**
- Sheet resistance is affected by film thickness, grain size (larger grain size, lower resistivity), impurities, etc.



For a typical four-point probe, $S_1 = S_2 = S_3 = 1$ mm,
If current is applied between P_1 and P_4, $R_s = 4.53\ V/I$
If current is applied between P_1 and P_3, $R_s = 5.75\ V/I$

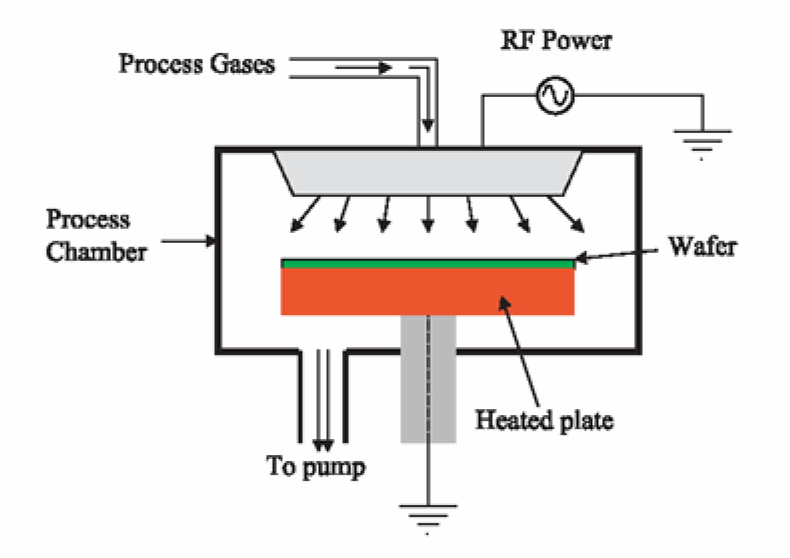
Metal CVD

Metal CVD

- Metal CVD uses gas precursors to form chemical reactions under external heat, resulting in metal film deposition.
- CVD metal films have very good step coverage and gap-fill capability (can fill tiny holes).
- CVD metal films are good for plug and local connections.
- CVD metal films have poorer quality and higher resistance than PVD metal films.
- Popular CVD metals are:
  - tungsten
  - tungsten silicide
  - titanium nitride

Metal CVD systems

- Most metal depositions are thermal processes, although sometime remote plasma sources are also used to generate free radicals.



A metal CVD system. The RF power is used for plasma cleaning the chamber

A typical metal CVD process sequence:

- Wafer slides into the chamber
- Slip valve closes
- Pressure and temperature are set
- All process gases flow in; deposit starts
- Main processing gas is terminated (second processing gas remains on)
- All process gases are terminated
- Chamber is purged with nitrogen
- Slip valve opens, and robot pulls the wafer out
- Chamber is ready for next deposition

Physical vapor deposition (PVD)

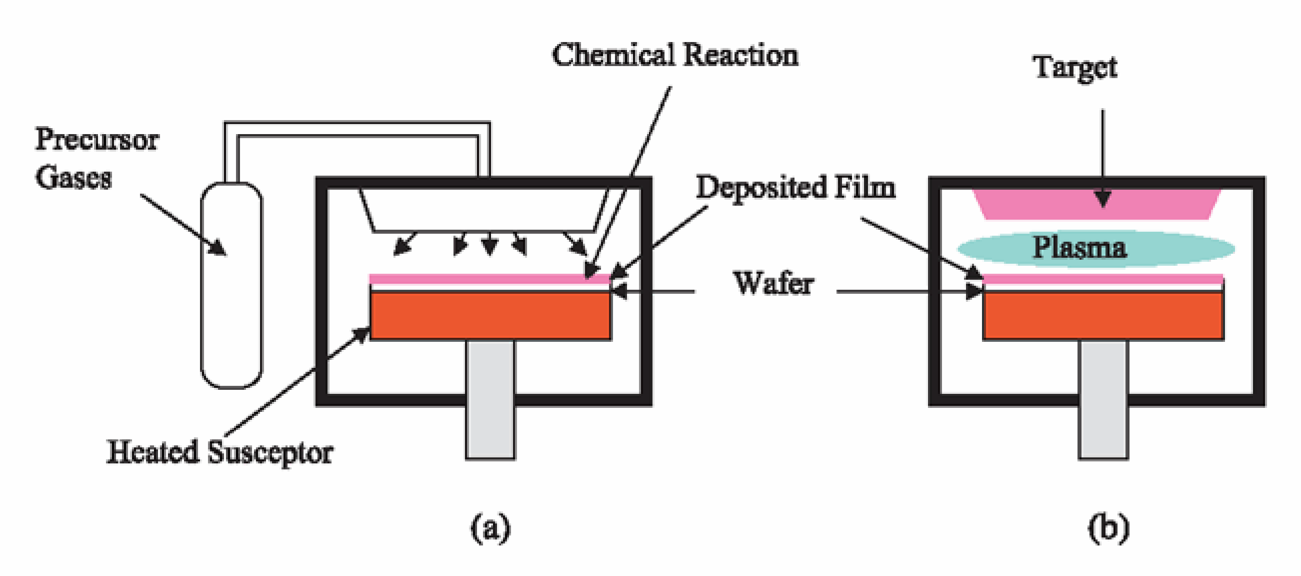
Physical vapor deposition (PVD)

- Physical vapor deposition process:
  - Vaporizing the solid materials by heating or sputtering
  - Re-condensing the vapor on the substrate surface to form solid film.
- PVD processes are used to deposit:
  - Ni layers
  - TiN glue layers; TiN ARC layer;
  - Ta and TaN barrier layers
  - Al-Cu layers
- Two methods are used in metal PVD processes:
  - Evaporation
  - Sputtering

PVD vs. CVD

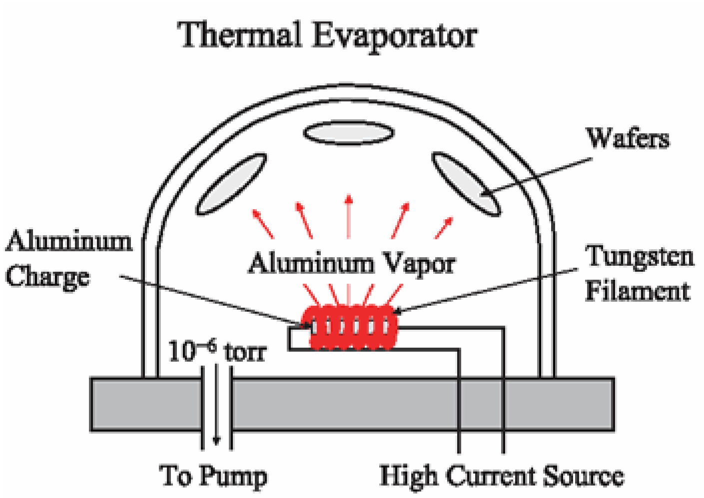
- PVD vs. CVD:
  - CVD – use gaseous precursors; rely on chemical reactions;
  - PVD – use solid sources; not rely on chemical reactions;
- CVD films typically have better step coverage
- PVD films typically have better quality, low resistivity, low impurity

a). CVD
b). PVD

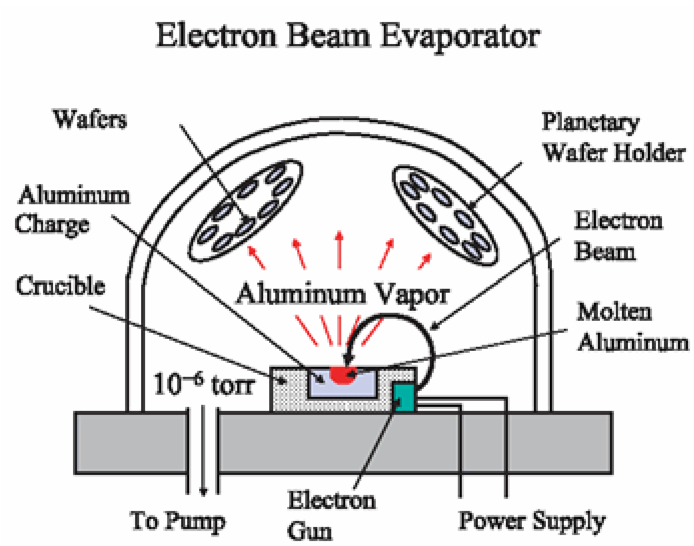


Evaporation processes

- Aluminum (Al) can be deposited using both the thermal evaporator and the electron beam evaporator.
- Al has relatively low melting (660 °C) and boiling points (2519 °C)
- E-beam evaporation has better step coverage and less contamination.



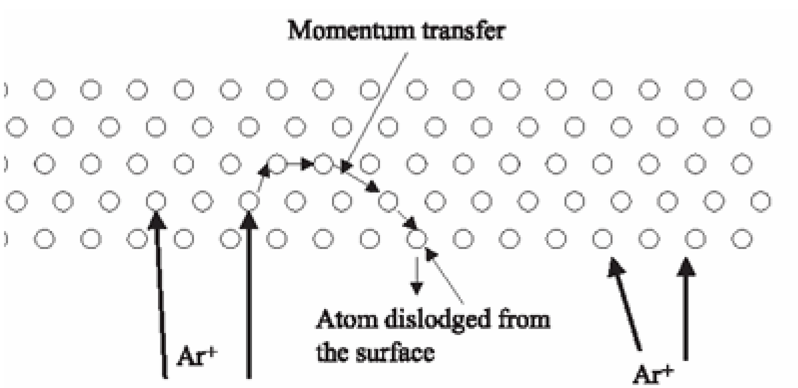
Thermal evaporator



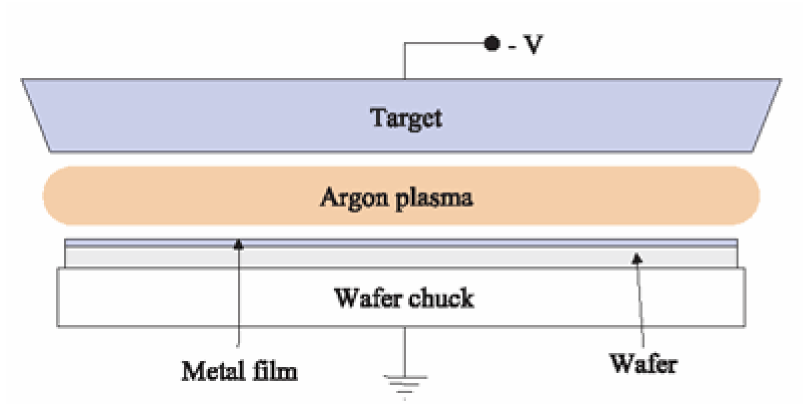
E-beam evaporator

Sputtering process

- Sputtering is the most common PVD process for IC fabrication
- It uses energetic ion bombardment to dislodge atoms or molecules from a solid metal surface and redeposit them on a substrate surface to form a metal thin film.
- Argon is the most commonly used gas for sputtering because it is inert, heavy and low cost.
- Metal solid target has negative bias, accepting Ar+ bombardment.
- Ulta-high vacuum (UHV) is required to minimize contamination.



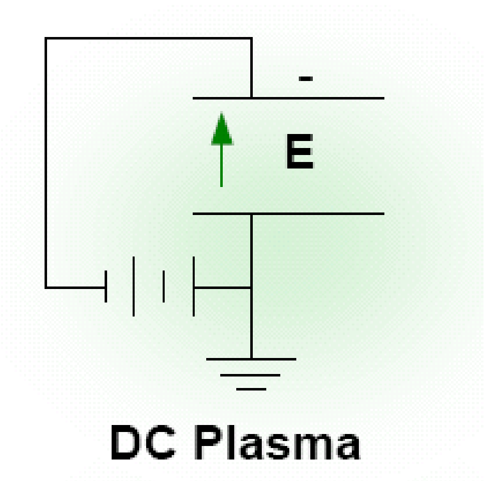
Sputtering process

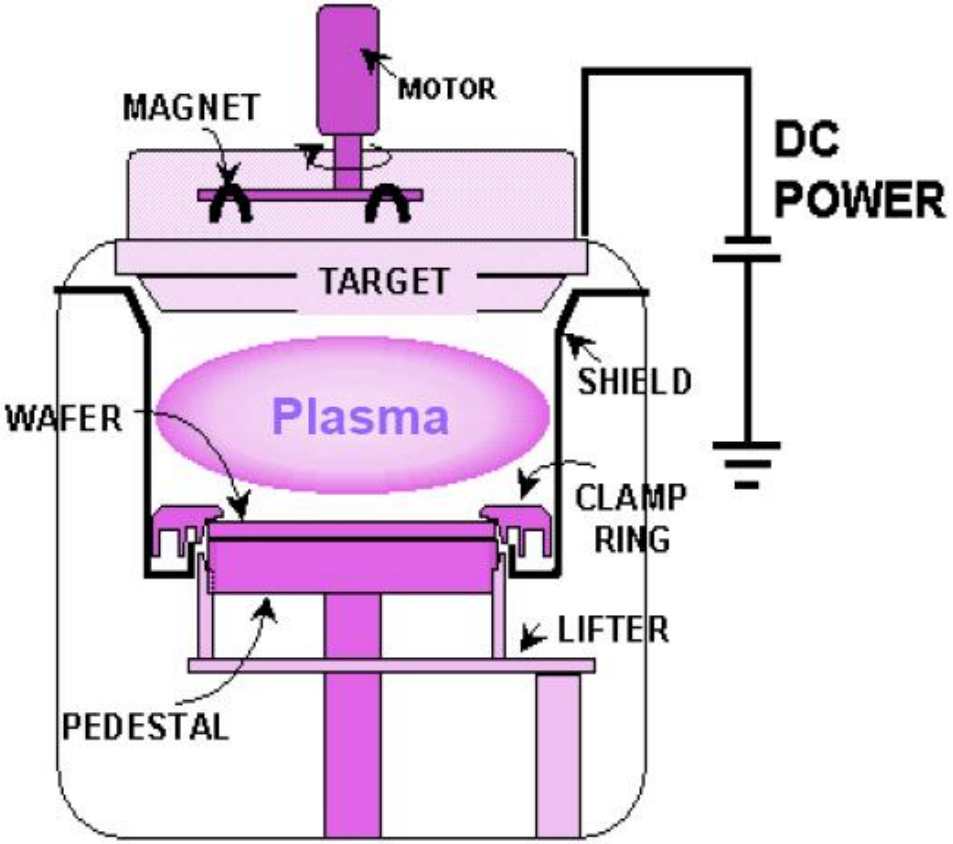


a dc sputtering system

Convention PVD (DC Plasma)

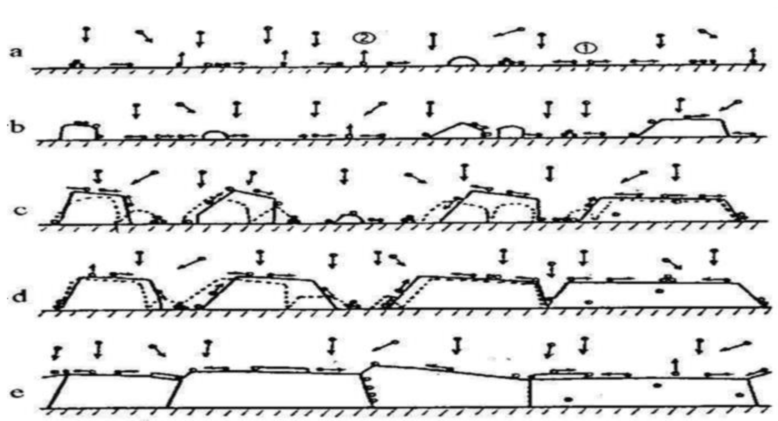
- Target (Metal source)
- Plasma
- Gas
- Pump
- Pedestal

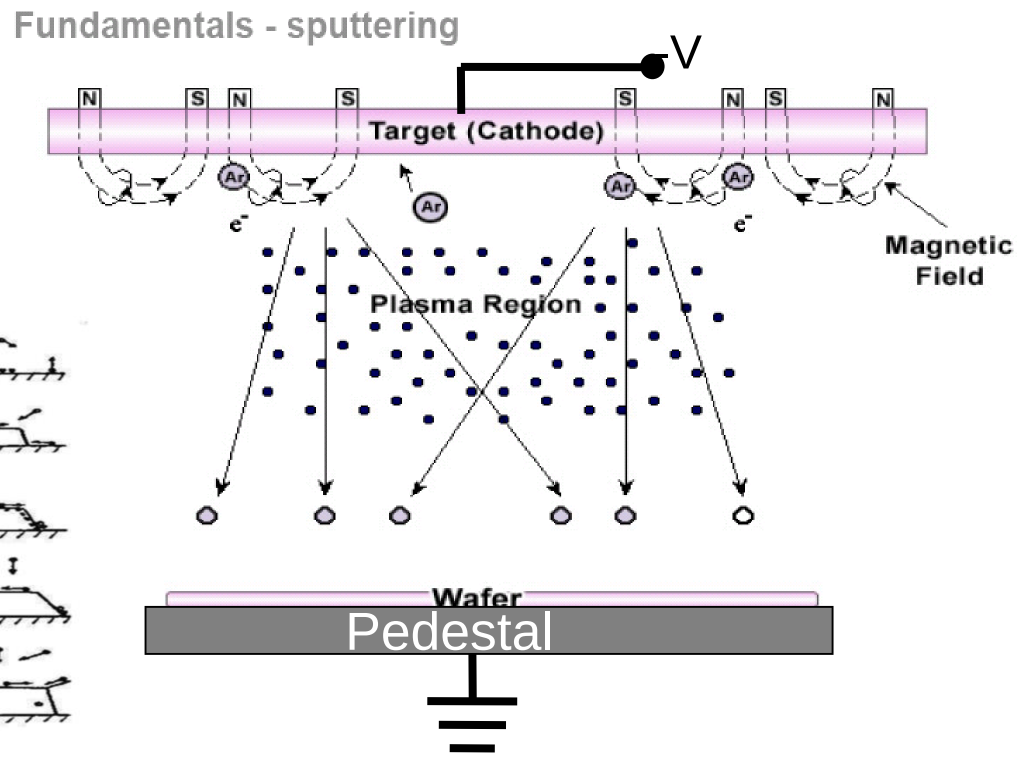




Convention PVD Process

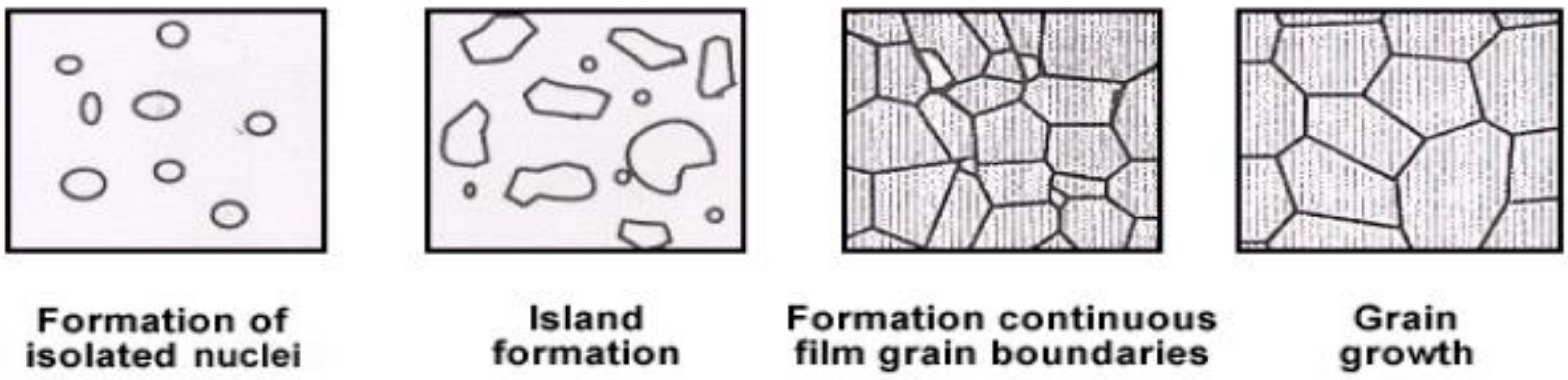
- Ion generated & toward a target
- Atoms sputter from target
- Sputtered atoms traverse to substrate
  - Condense
  - Nucleated
  - Form a film



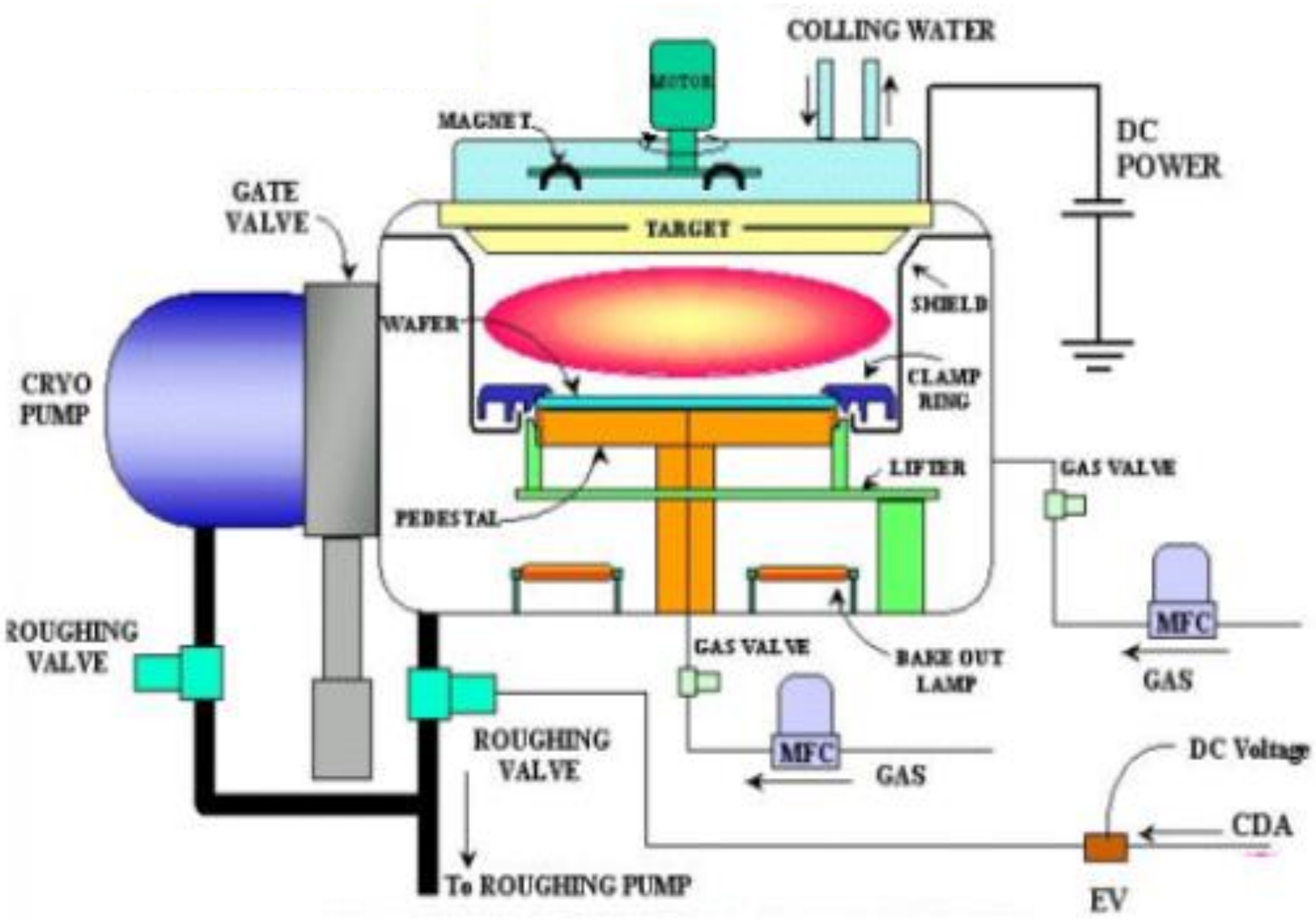


Film Growth Overview

- Formation of isolated nuclei
- Island formation
- Formation continuous film grain boundaries
- Grain growth

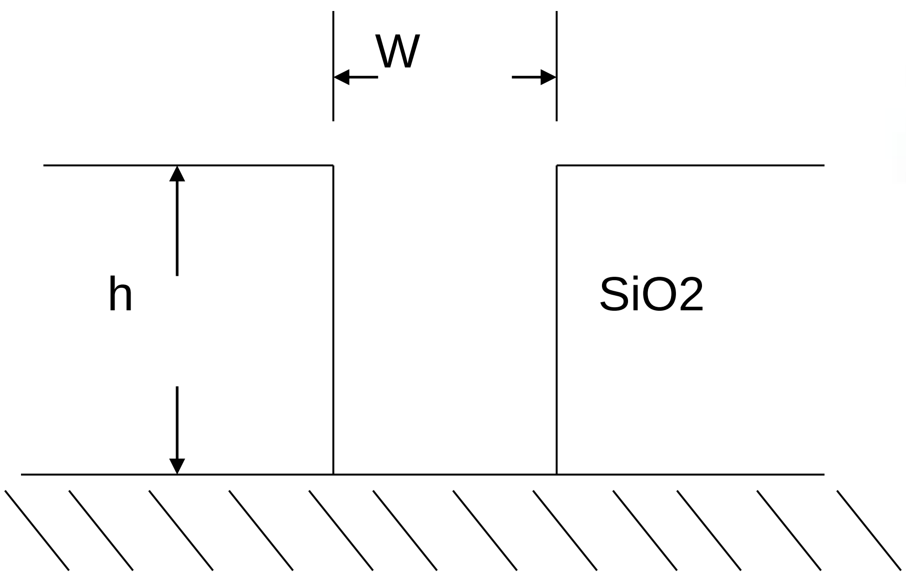


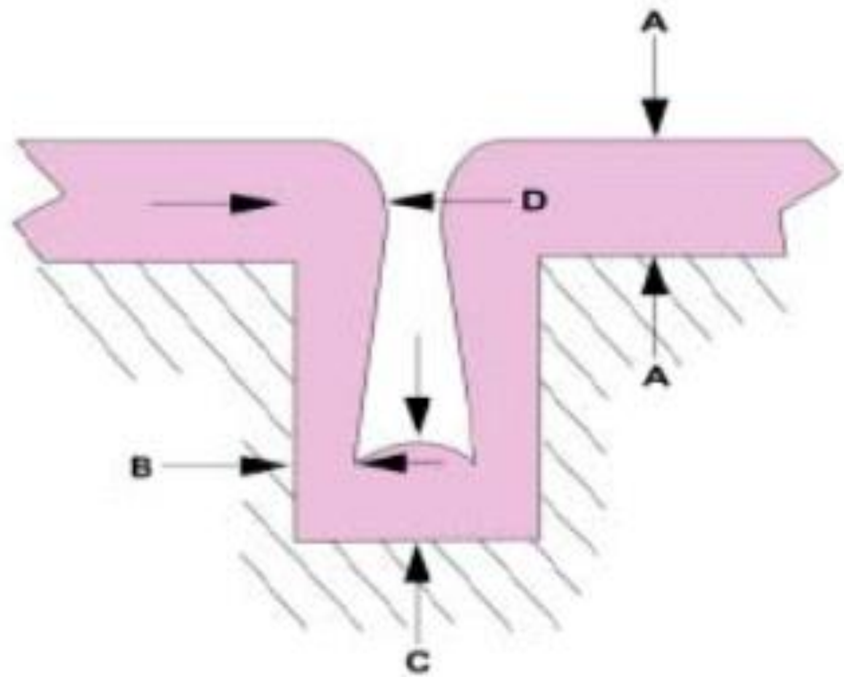
DC Sputtering Deposition Schematic



DC Plasma PVD Bottle Neck

- **Aspect Ratio (h/w)**
- **Step Coverage**





Integrated metallization process

Integrated metallization process

- In a modern wafer fab, the metallization process is normally performed in one integrated process sequence using a cluster tool with multiple chambers.
- For example, the Al-Cu metallization steps are:
  Degas ➔ pre-deposition sputtering cleaning ➔ barrier layer deposition ➔bulk aluminum alloy deposition.

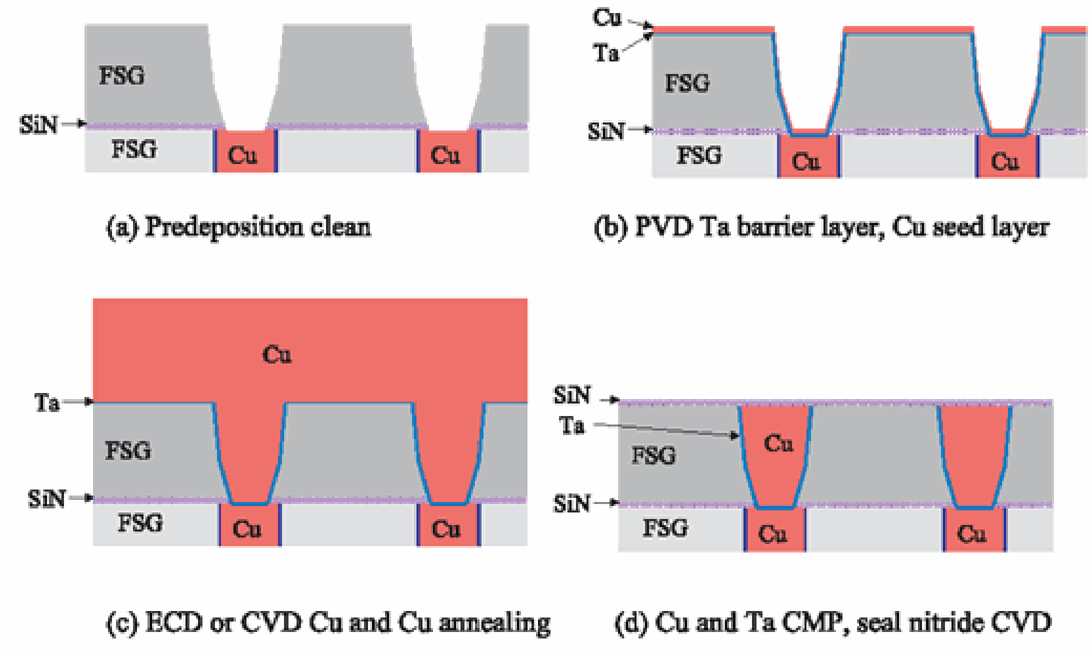
<u>Degas:</u> heat wafer to drive out gases and moistures;

<u>Pre-cleaning:</u> to remove native oxide from metal surface to reduce film resistance.

Cluster tool for integrated metallization process

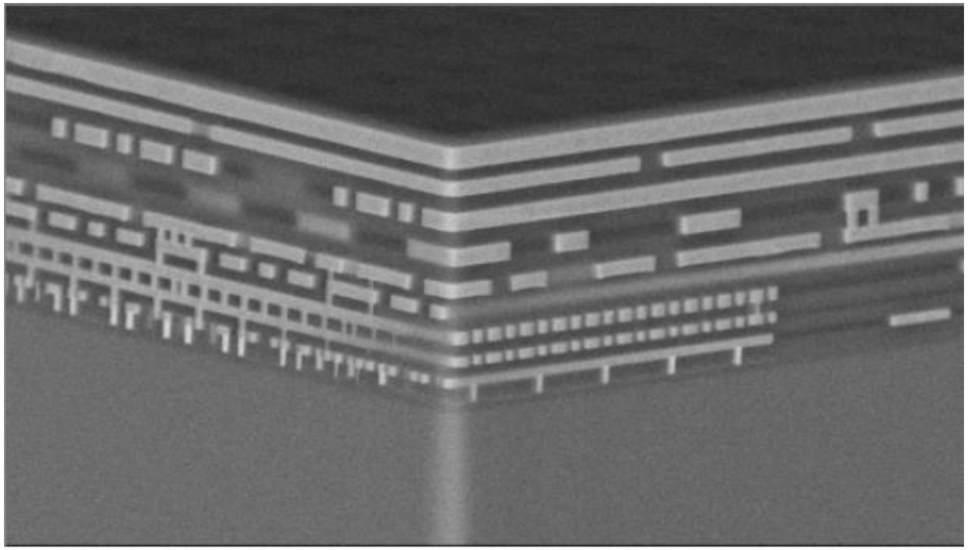
Cu interconnection process

a. Pre-deposition clean to remove native oxide from metal surface;
b. PVD Ta barrier, Cu seed layer deposition
c. CVD Cu and Cu annealing
d. Cu and Ta chemical-mechanical polishing (CMP), seal nitride CVD



Key Factors Affecting Cu Interconnect Performance

1. Gap-Fill
2. CD Uniformity
3. Overburden
4. Anneal

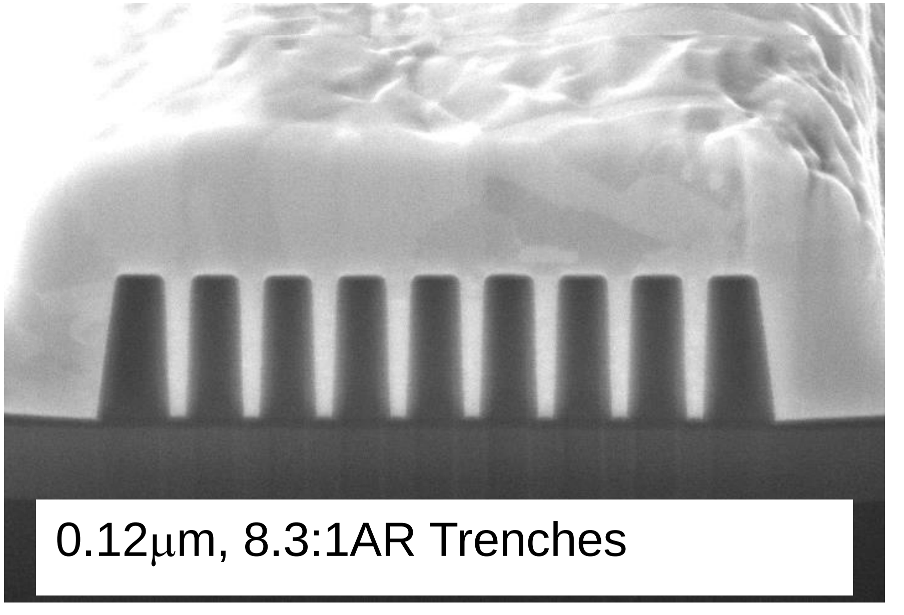


AMD's 9 Cu Levels

Courtesy: SEMITOOL

Key Parameters for Gap-Fill

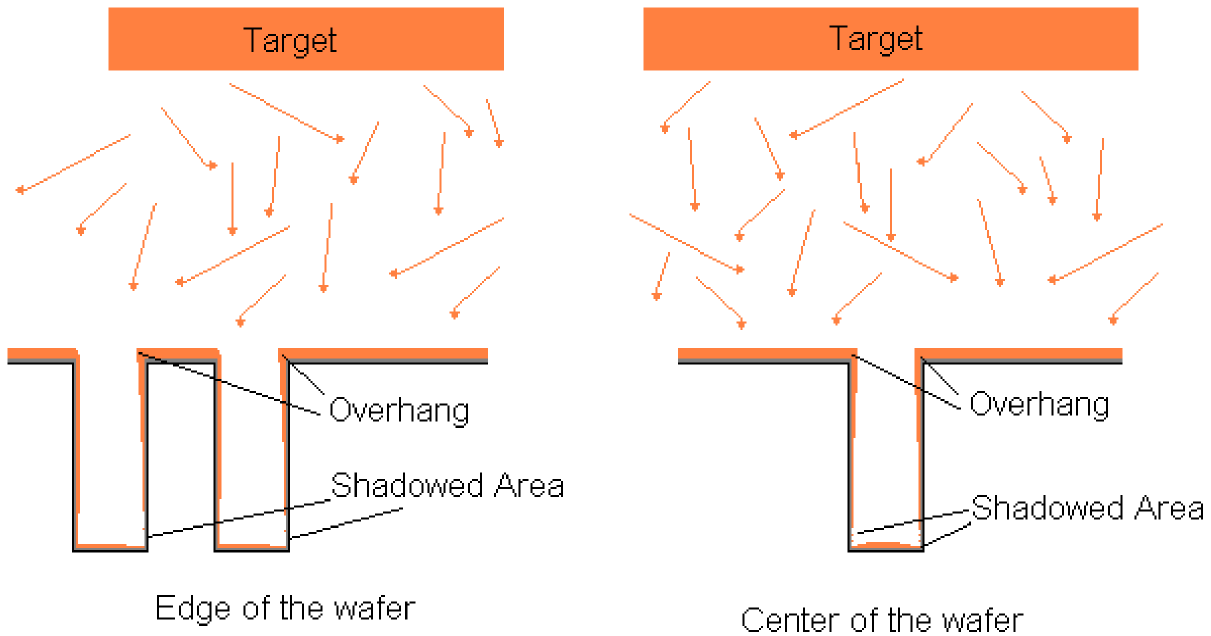
1. **Seed and Barrier Layers**
    1. Uniformity
    2. Thickness
2. **Plating Recipe**
    1. Hot Start (Initiation)
    2. Fill Current Density
    3. Waveform
3. **Plating Chemistry**
    1. Inorganic
    2. Organic



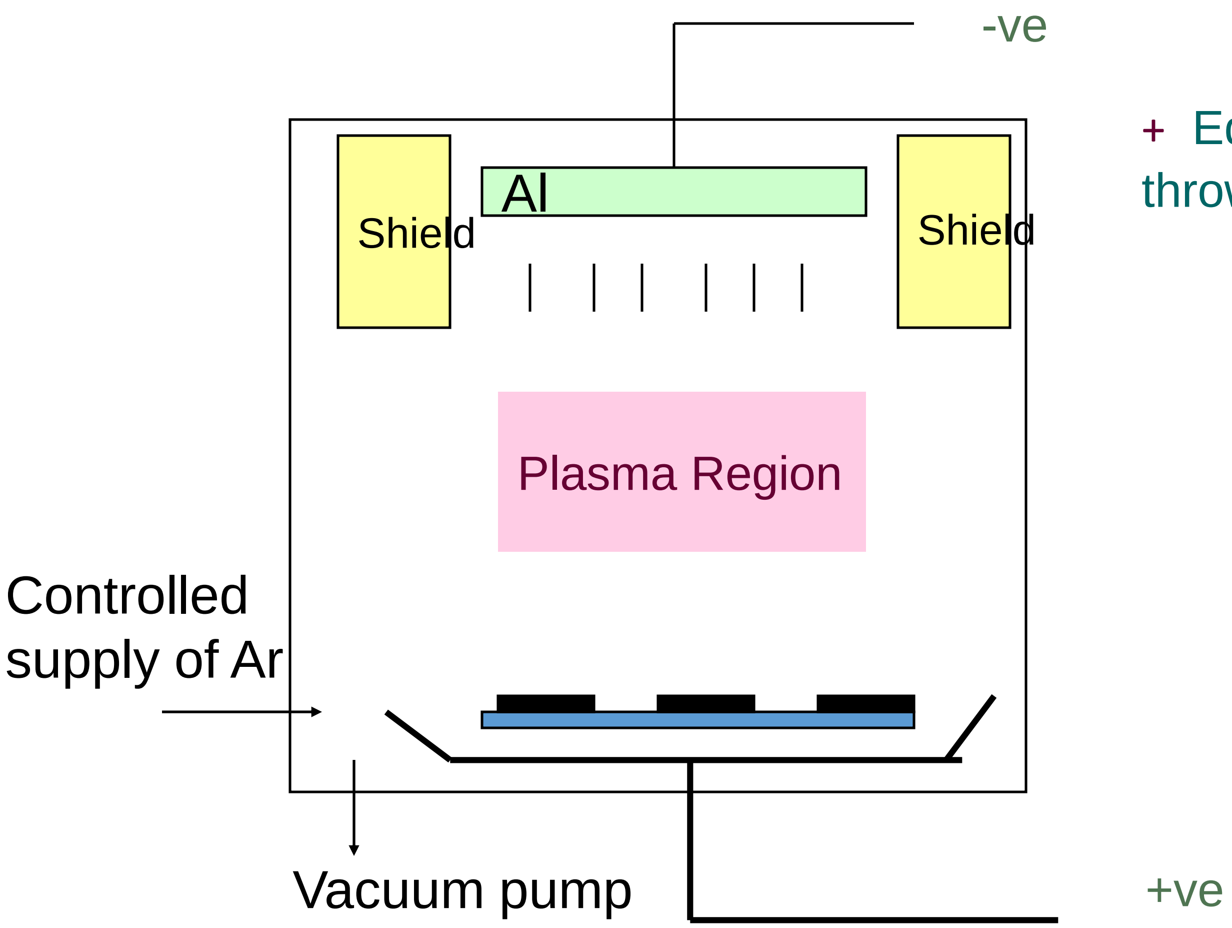
0.12μm, 8.3:1AR Trenches

Seed and Barrier Layers

Physical Vapor Deposition (PVD) Effects

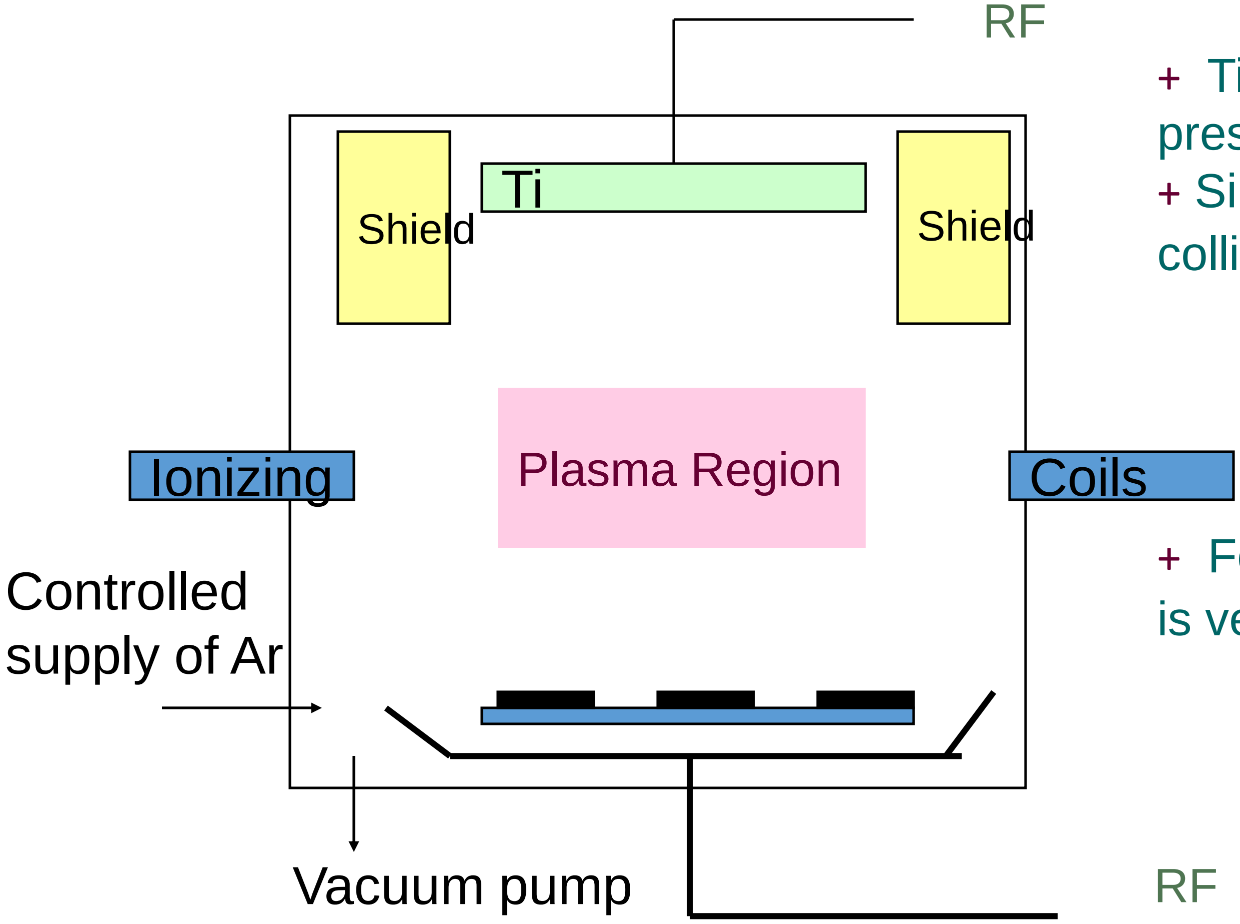


PVD: Al
Collimated Beam



- Equivalent to long throw

PVD: Ti



+ Ti ions also present
+ Similar to collimated

+ For liners, IMP Ti is very common

Types of Fill: SEM

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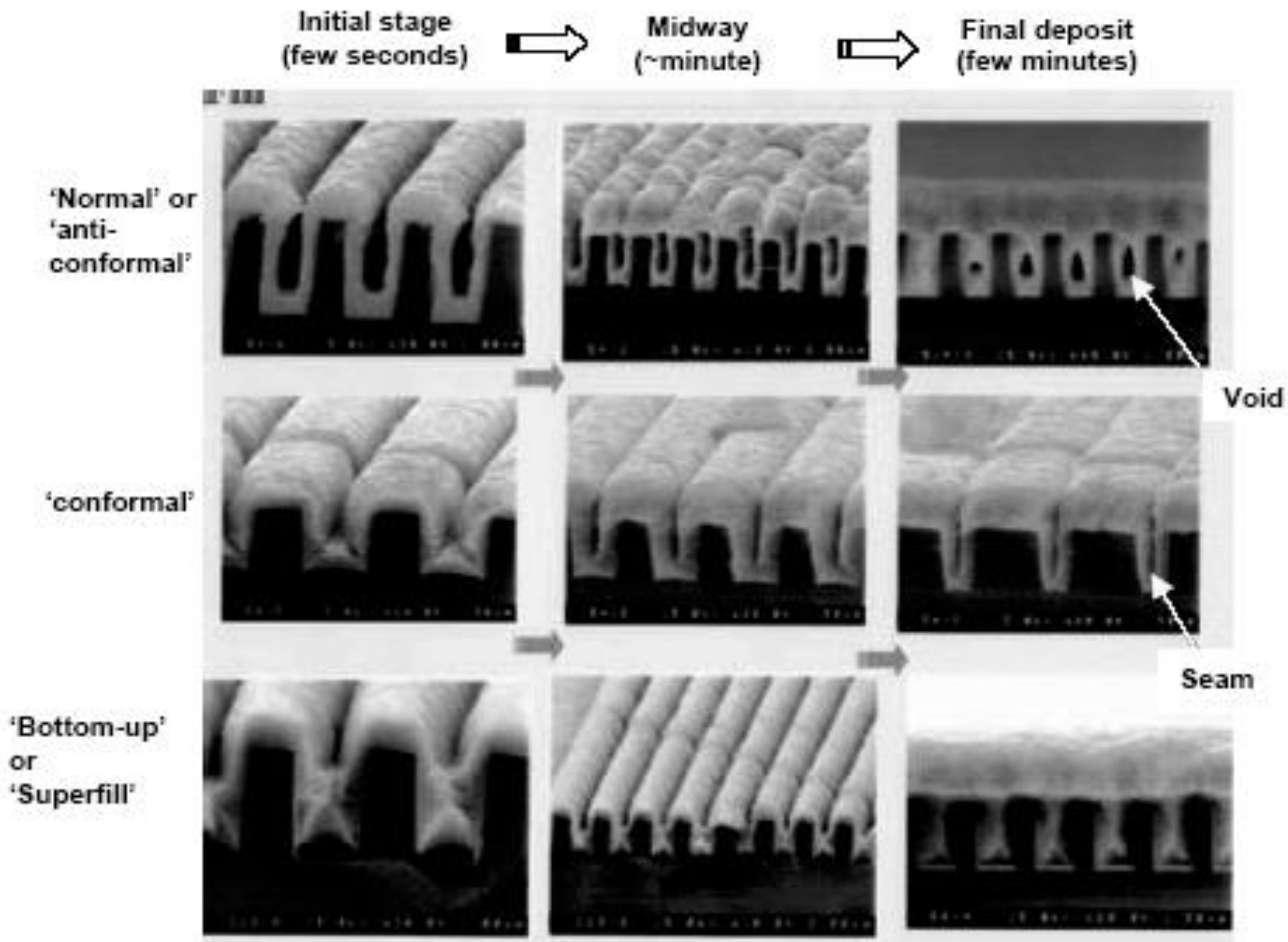


Types of Fill: Schematic

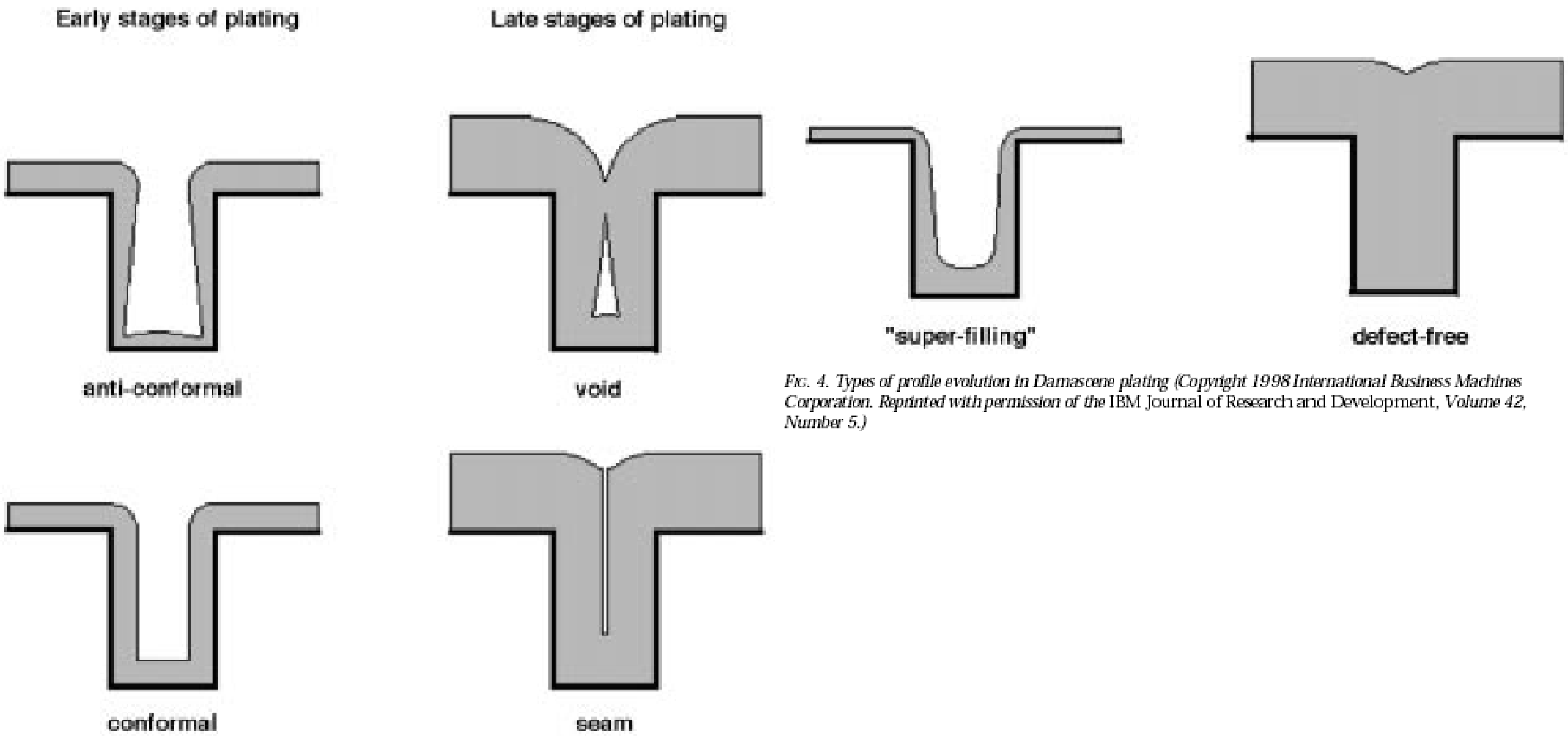
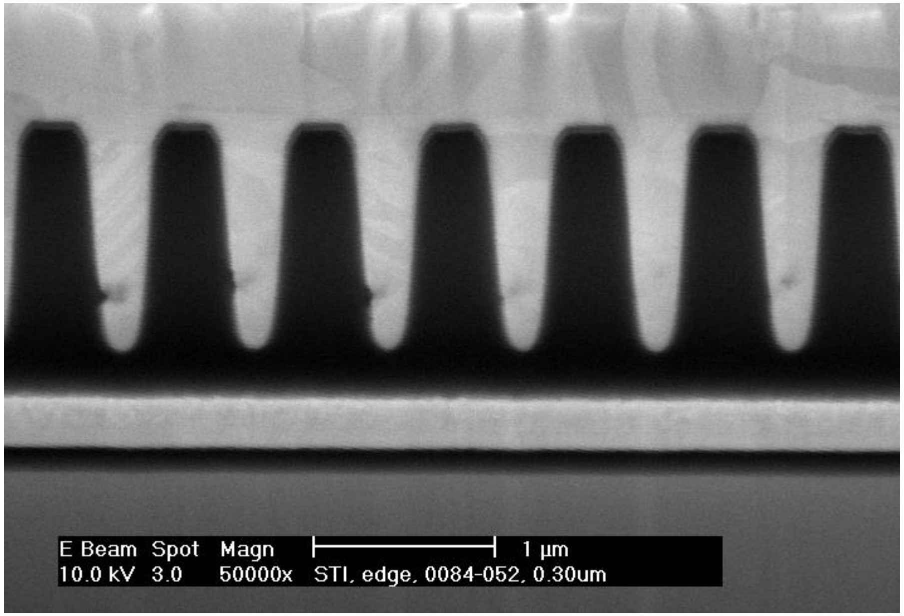
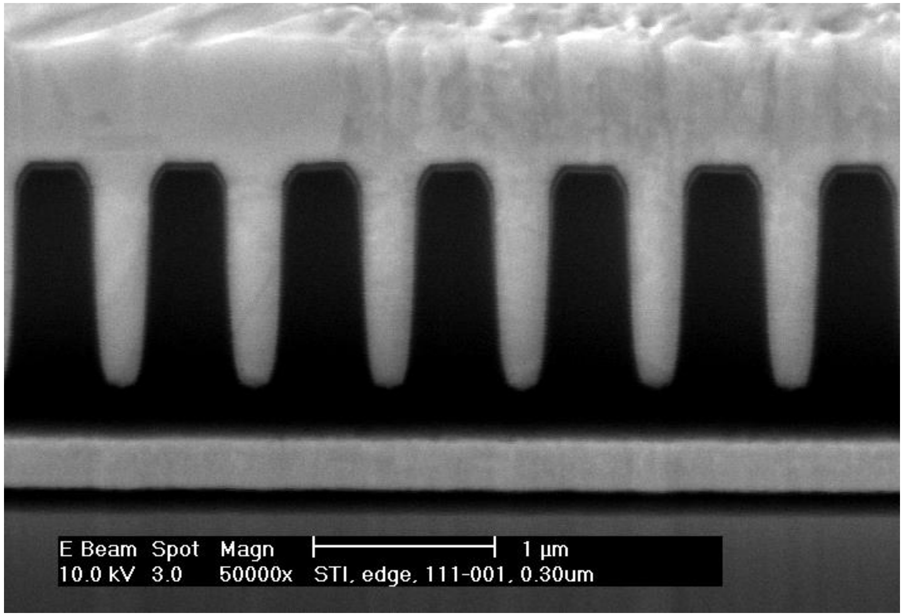


FIG. 4. Types of profile evolution in Damascene plating (Copyright 1998 International Business Machines Corporation. Reprinted with permission of the IBM Journal of Research and Development, *Volume 42, Number 5.)*

Seed and Barrier Layer Uniformity

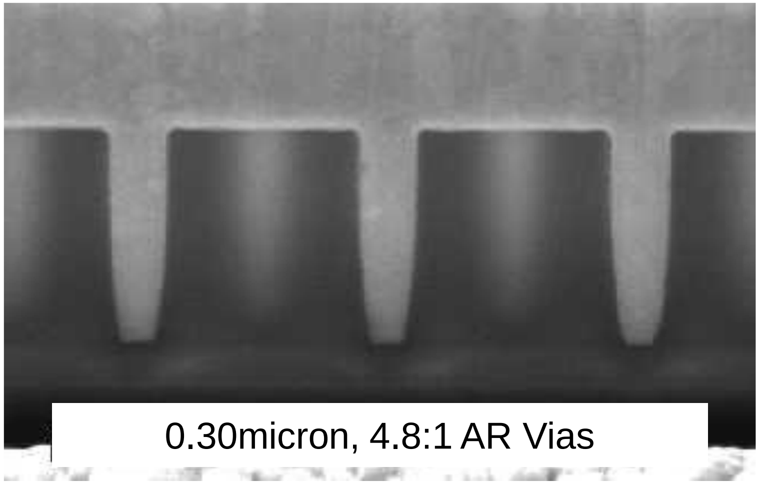


Edge Shadowing

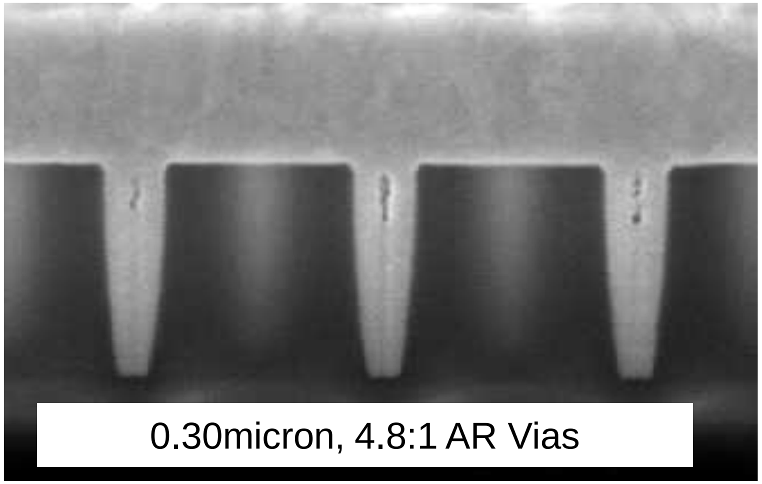


Optimized Seed Layer

Seed and Barrier Layer Thickness



1500Å Total Seed Thickness

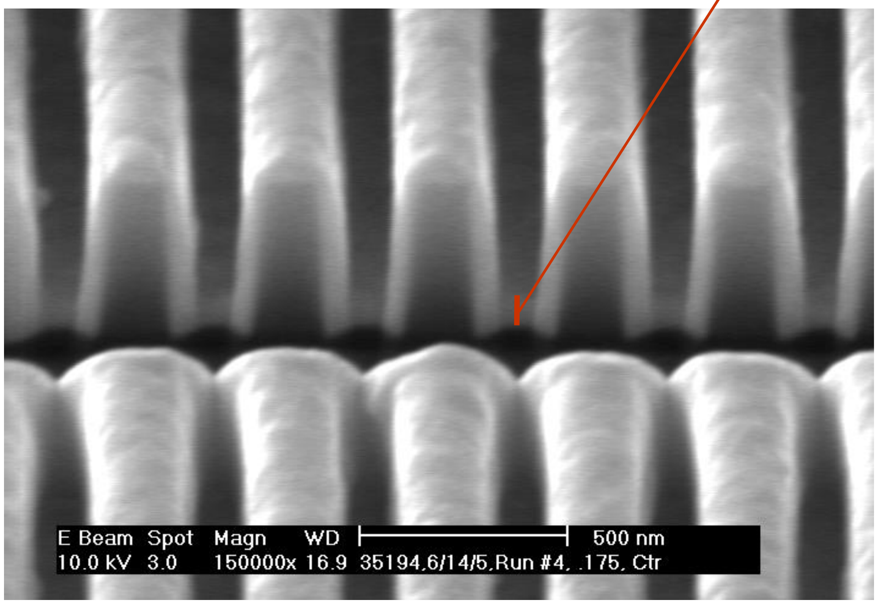


2000Å Total Seed Thickness

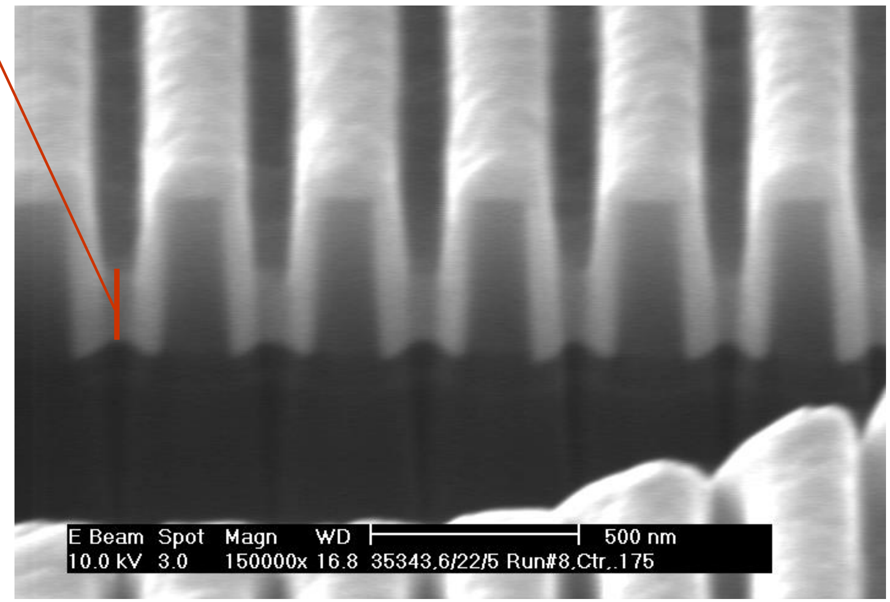
Plating Recipe Hot Start

2X Fill Rate on the 2V Hot Start

No Hot Start



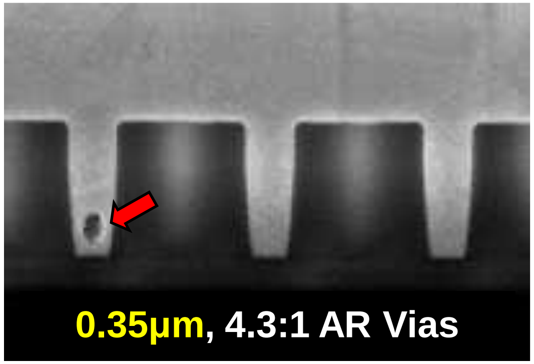
2V Hot Start



0.180 μm Line Width Trenches
48 Coulombs ECD

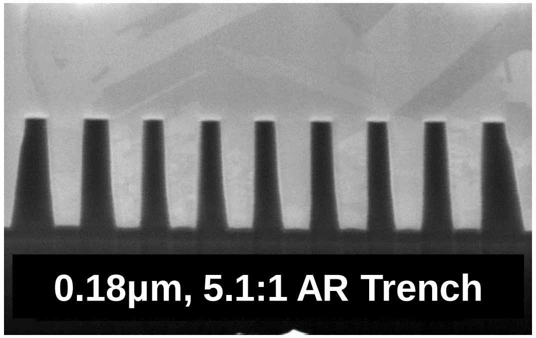
Plating Recipe Current Density

The Effect of Current Density upon Gap Fill



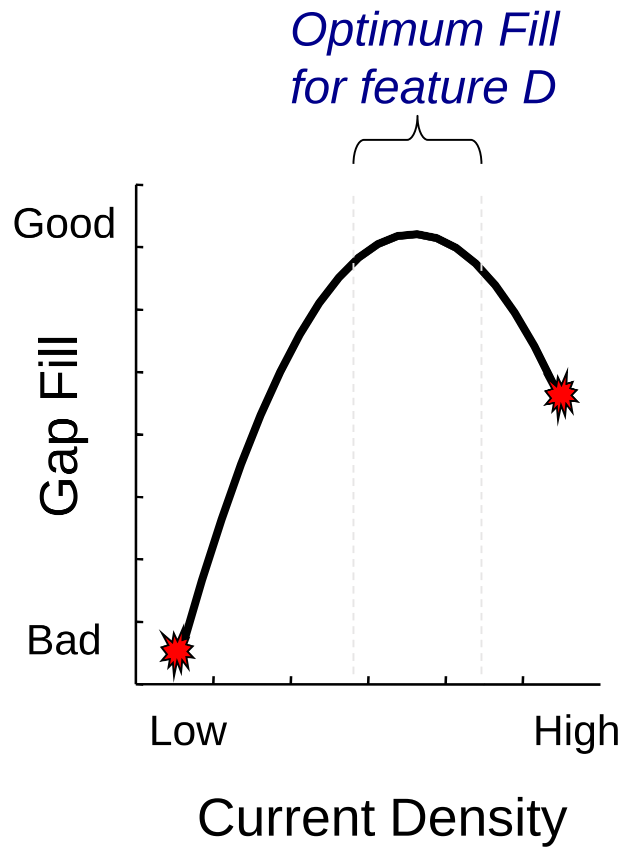
0.35µm, 4.3:1 AR Vias

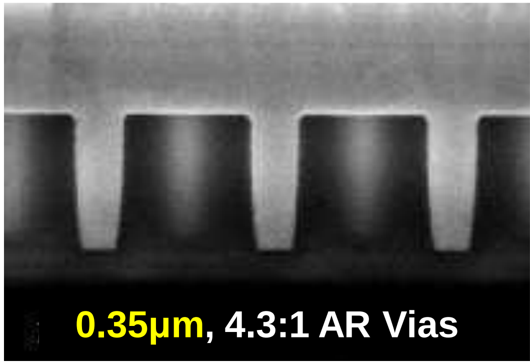
Current too Low



0.18µm, 5.1:1 AR Trench

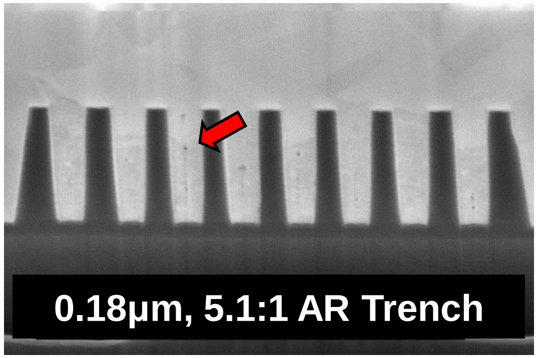
Optimum Current





0.35µm, 4.3:1 AR Vias

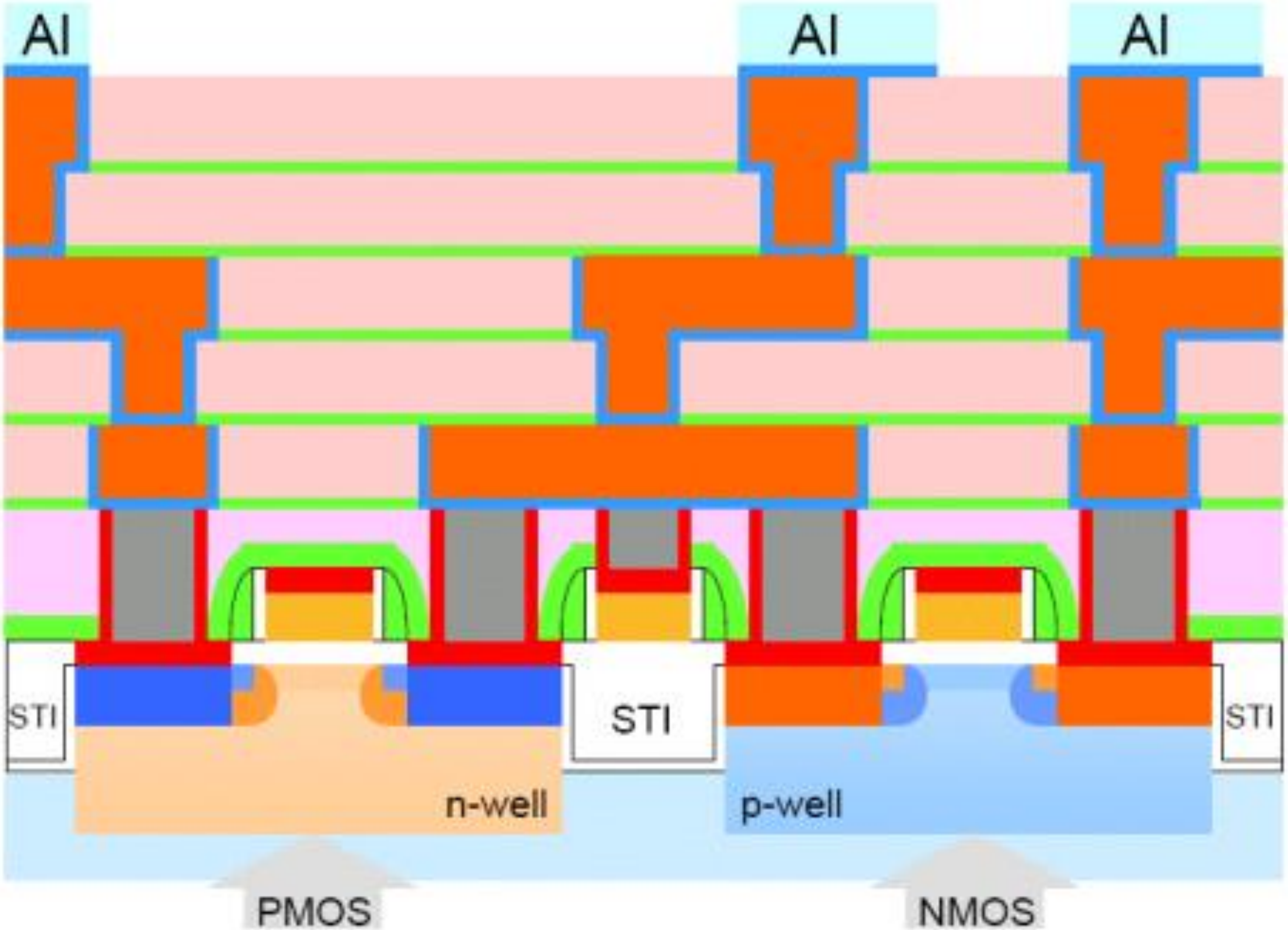
Optimum Current



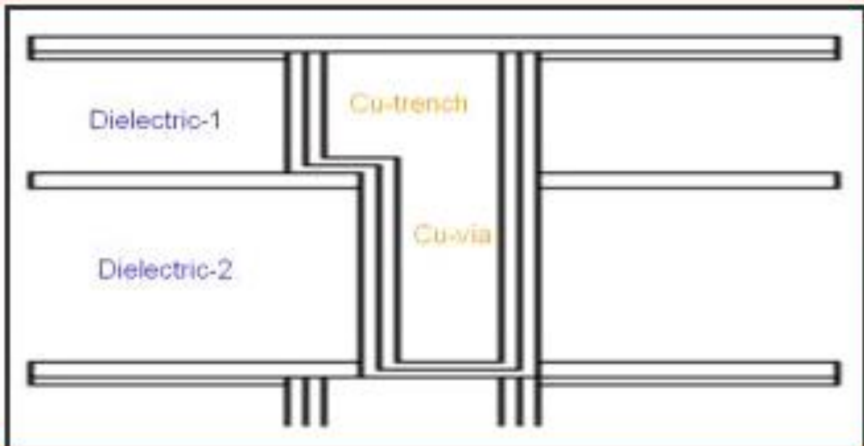
0.18µm, 5.1:1 AR Trench

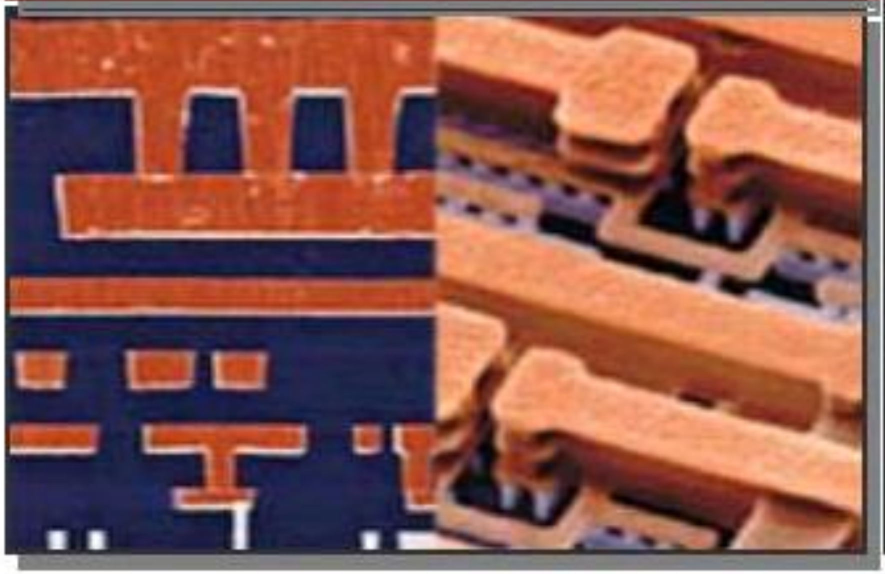
Current too High

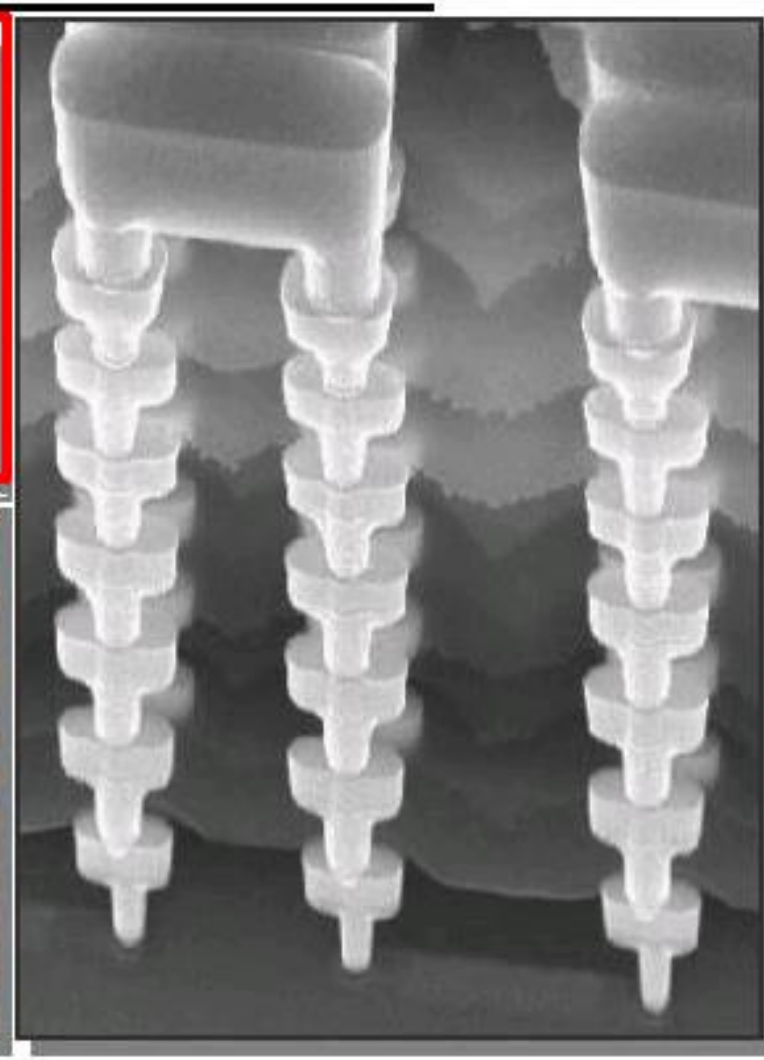
Metal Line Process Overview



Copper Scheme

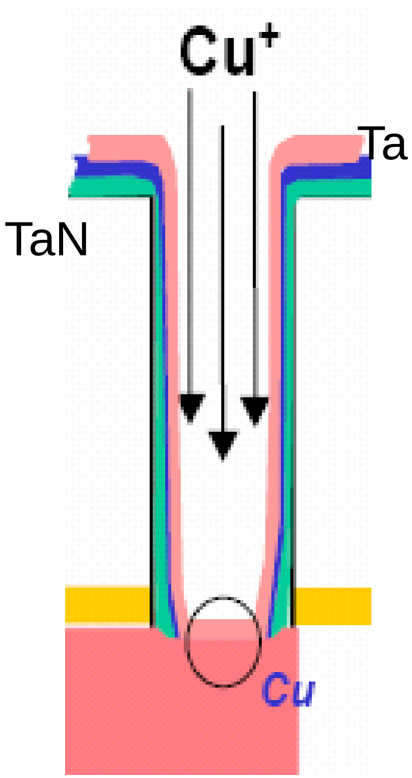


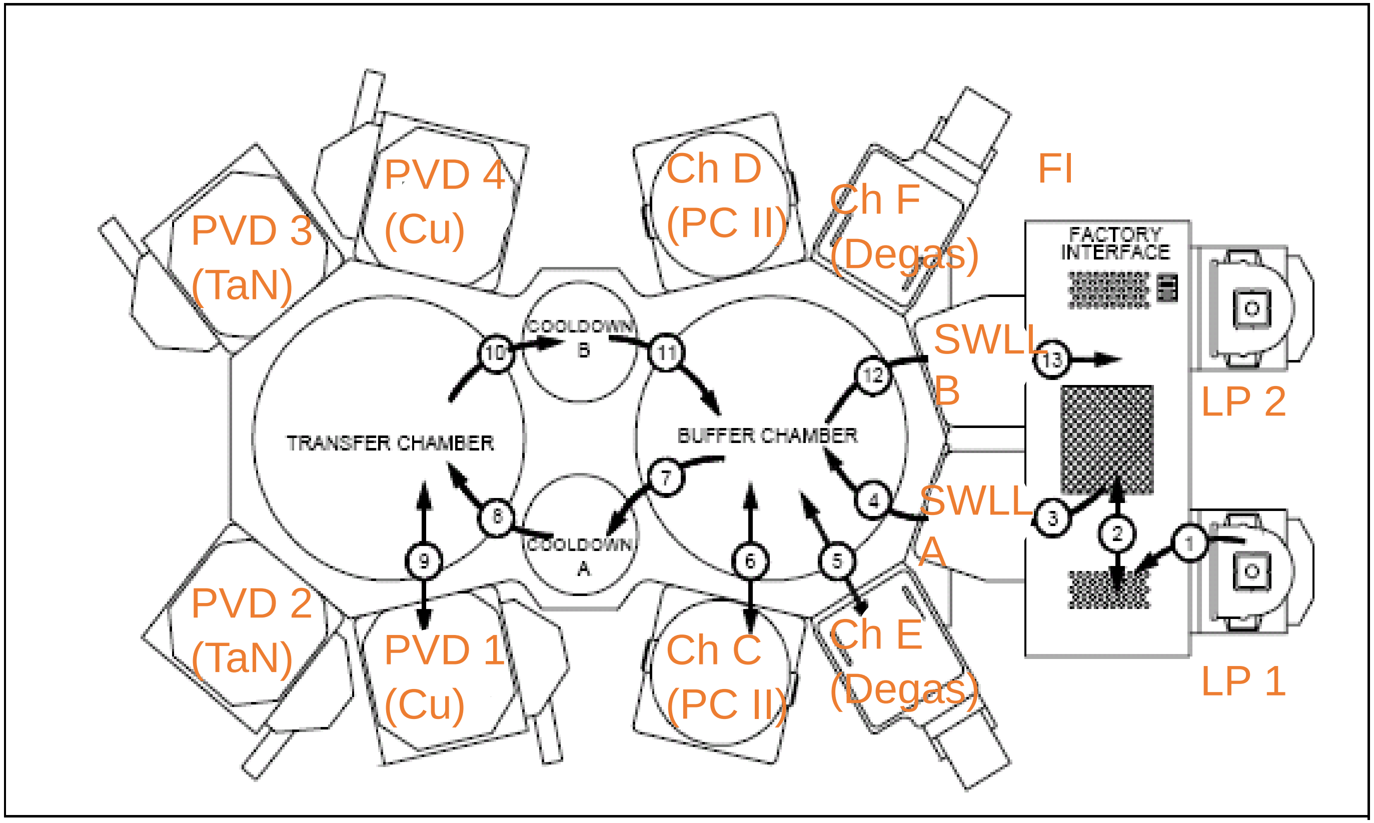




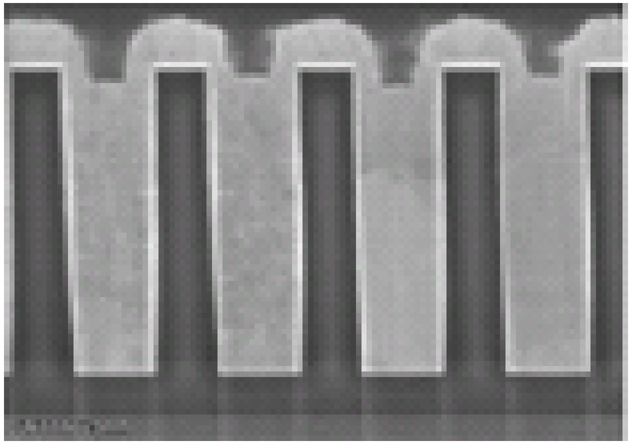
AMAT EnCoRe Barrier/Cu Seed

AMAT EnCoRe Barrier/Cu Seed

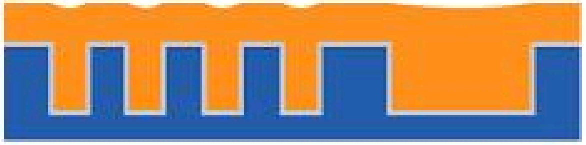


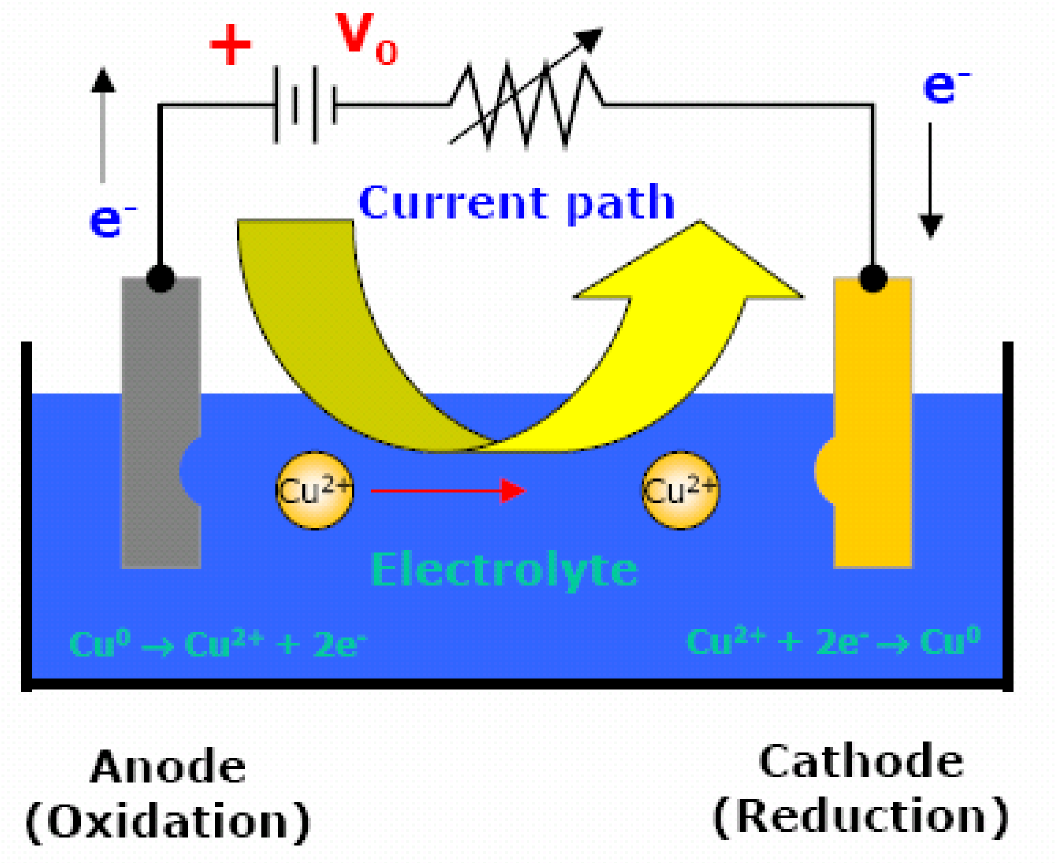


ECP (Electric Chemical Plating)



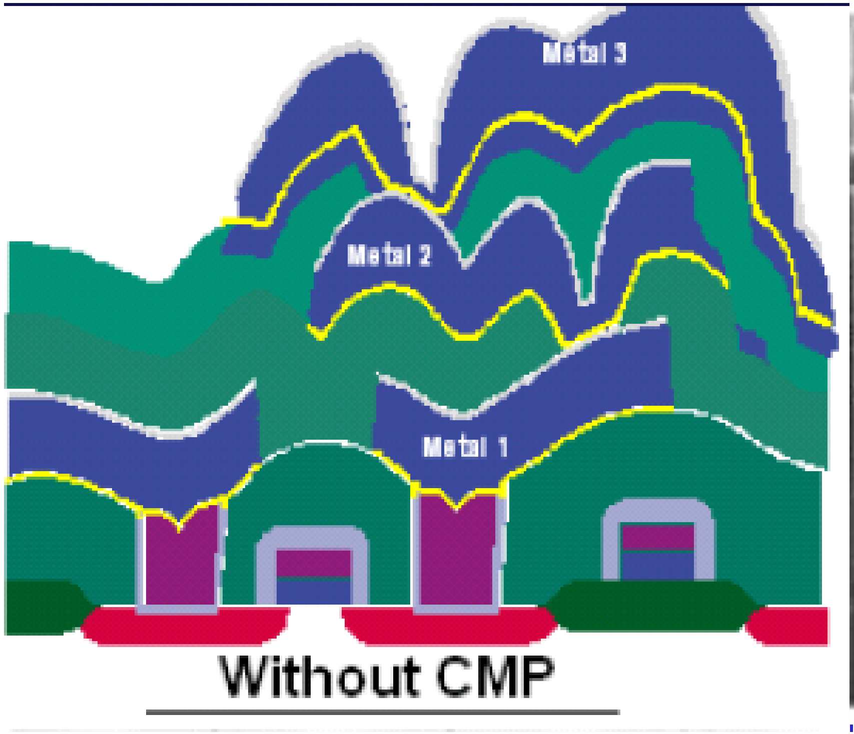
Un-Cleared Wafer Regions
Over polish Required

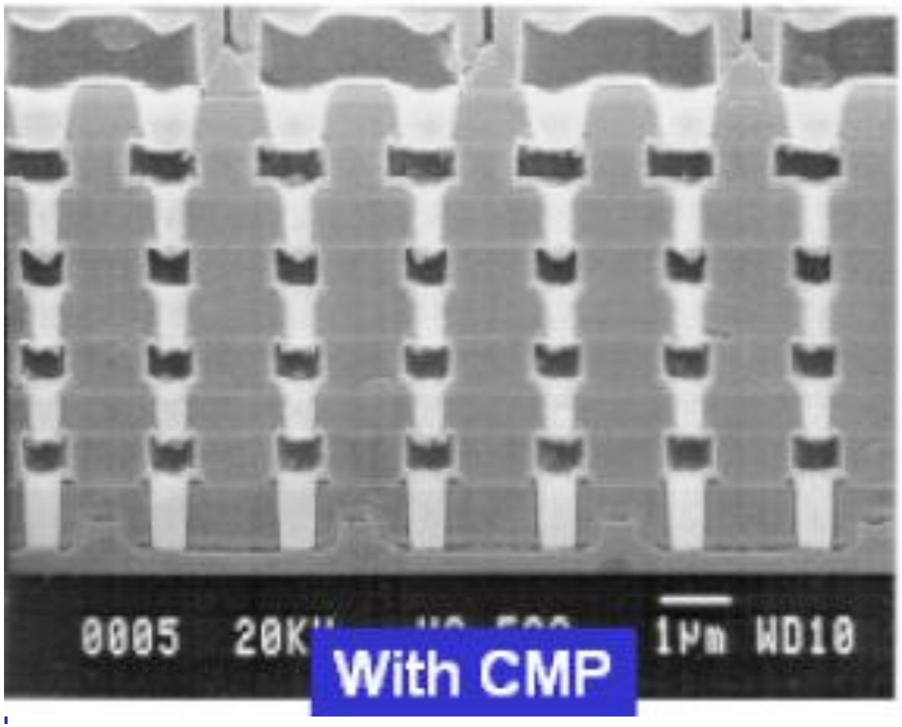




NVLS Sabre ECP

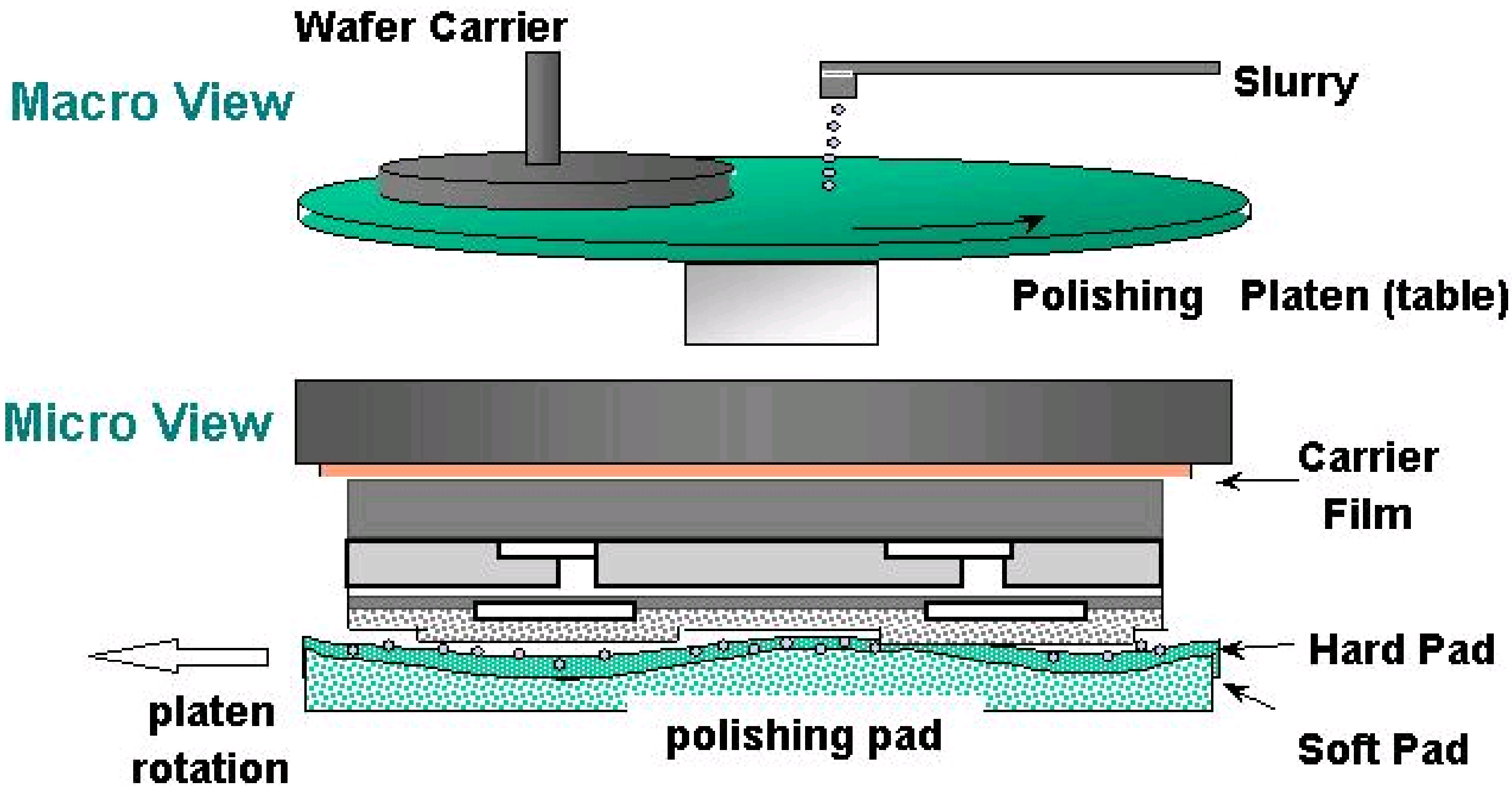
CMP (Chemical Mechanical Polish)





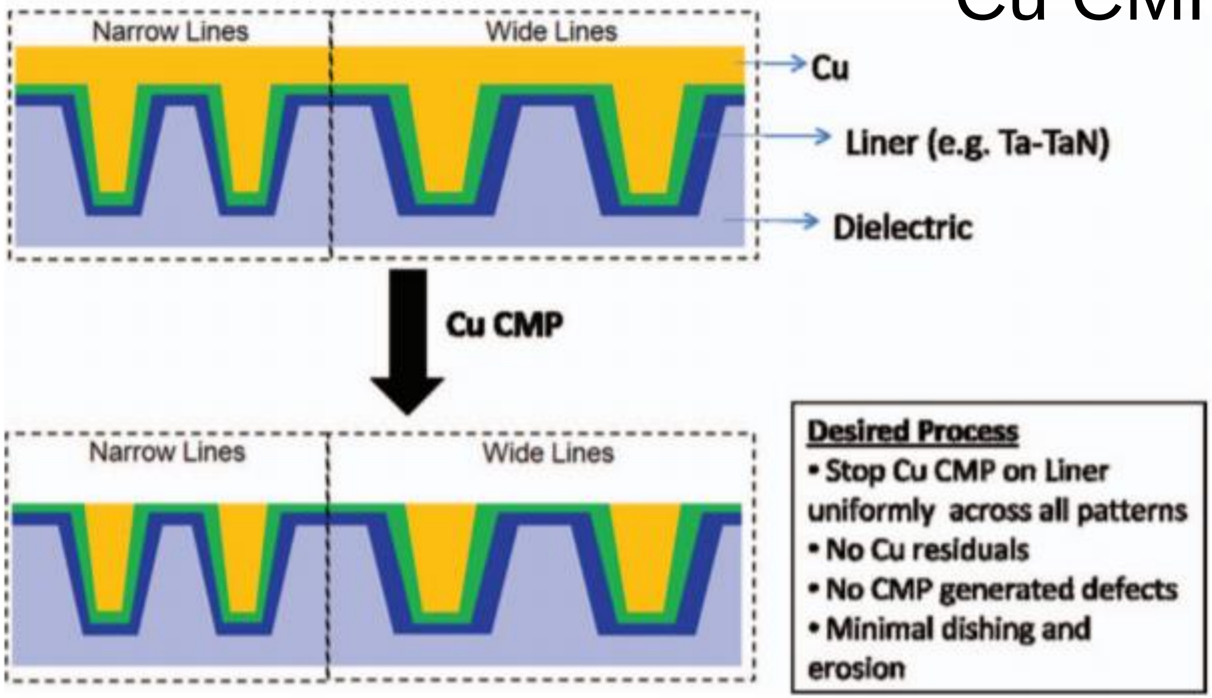
AMAT Reflexion CMP

Schematic of CMP Process



CMP is Chemical Mechanical material removal for wafer Planarization

Cu CMP - Fundamentals



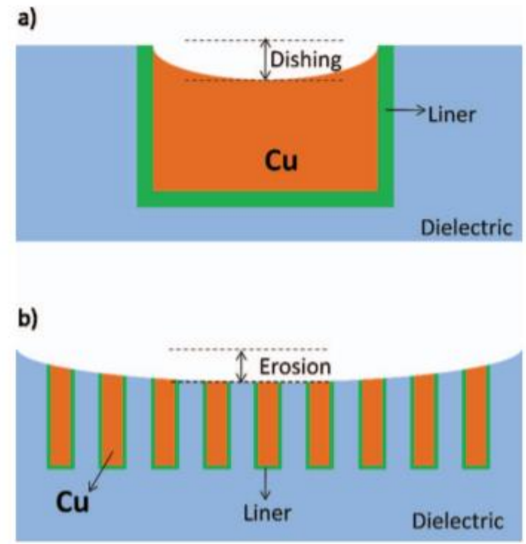
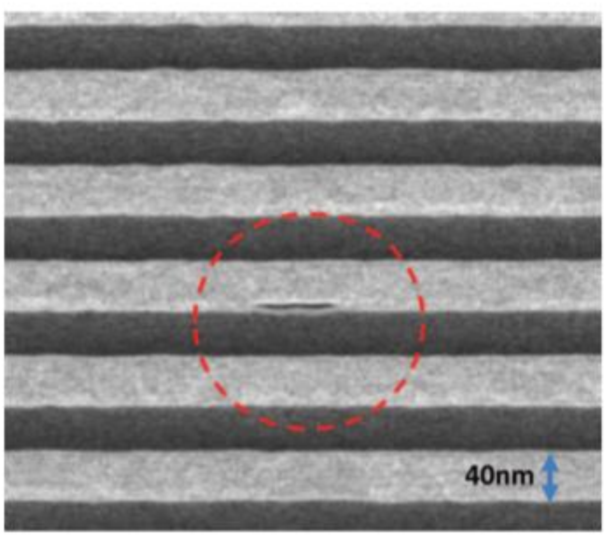


Figure 2. Conceptual framework showing dishing and erosion after barrier CMP as referred to in this manuscript.



Influence of Slurry on corrosion defects