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Dual graphene films growth process based on plasma-assisted chemical vapor deposition

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ABSTRACT

Graphene has been given great attention to overcome current physical limits in electronic devices and its synthesis routes are developing rapidly. However, graphene film manufacturing is still hindered by either low throughput or low material quality. Here, we present a low temperature PE-CVD assisted graphene growth process on nickel thin films deposited on silicon oxide. Furthermore, our process leads to the formation of two separated graphene films, one at the nickel surface and the other at the Ni/SiO_2 interface. A mixture of methane and hydrogen was employed as carbon precursor and activated by DC plasma. We found that the number of graphene layers on top of nickel can be controlled by carbon exposure time, from 1 to around 10 layers. Further annealing process of samples allowed us to achieve improved graphene films by the dissolution and segregation-crystallization process.

Keywords: Graphene synthesis, PECVD, Low temperature, Raman spectroscopy, High Resolution Transmission Electron Microscopy

1. INTRODUCTION

Graphene[1], a 2D crystal made only of sp^2 carbon atoms arranged in a honeycomb network, is often viewed as the mother block of fullerene and nanotubes. Since its first isolation in 2004, it has been the focus of an intense research activity due to its astonishing properties such as ultra-high room temperature carrier mobility up to 250,000 cm^2/Vs [2], ballistic conductivity due to its band structure and transparency due to its atomic thickness[3], quantum hall effect even at room temperature[4] and a thermal conductivity[5] higher than copper.

The original technique used to firstly isolate graphene, was the micromechanical exfoliation of HOPG[1]. Although it can produce high quality graphene sheets, this technique has critical limitations in size of the sheets, yield and reproducibility and is mainly suitable for initial fundamental research. Recently proposed chemical exfoliation routes[6,7] are very promising techniques due to their low costs, but such wet process generally yields small size graphene flakes with many structural defects. Epitaxial graphene growth has also been proved but unfortunately it is only possible with very specific substrates[8] and it requires high temperature treatments under ultra high vacuum. Newly introduced chemical vapor deposition techniques offer huge potential for transfer to the microelectronics industry, as they allow growing large scale graphene films[9-11] on various catalysts[12-14]. However, they also generally require high synthesis temperatures around 900°C and the as-produced graphene sheets need post-growth transfer to appropriate substrates, process that can significantly deteriorate the sheet quality.

In 2007, there was a first attempt to grow graphene by plasma enhanced chemical vapor deposition[15]. However, their method used high temperature and long time process up to 90 minutes. Here, we present a plasma-assisted CVD large area graphene growth method, at temperatures as low as 450°C. An annealing process can then be applied to further enhance the graphene films crystalline quality. One outstanding feature of our approach is the possibility to form two separated graphene films, one at the catalyst surface and the other one at the catalyst/substrate interface, regardless of the fact that a further annealing step is performed or not.

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Not long ago, Ismach et al.[16] introduced a direct chemical vapor deposition of graphene on dielectric surfaces. However, their approach requires the evaporation of the catalyst copper layer to depose the grown graphene film on the underlying insulating substrates. This method is thus not far from a transfer technique and induces additional stress on graphene films. In comparison, the method we propose can yield an interface graphene film directly on a dielectric substrate suitable for further devices processing. We can eliminate thus the transfer step to suitable substrates which is an extremely elaborate process and generally induces huge stress on the films. Moreover the synthesis temperature could be lowered in order to increase compatibility with a wide substrates range including glass.

2. EXPERIMENTAL

The graphene films were prepared by plasma-enhanced chemical vapor deposition (PE-CVD) of carbon, using a methane-hydrogen mixture as precursor gas. The PE-CVD setup has already been described elsewhere [17,18]. The catalyst metals, 200 nm of nickel, is uniformly evaporated by e-beam technique on silicon substrates covered by a 300 nm thick thermal oxide (Si-Mat, N++/As, 100). Since our approach demonstrates dual graphene growth, especially one film at the interface between the nickel layer and the SiO_2, we took special care to avoid any carbon contaminations. In details, the oxidized silicon substrate was dipped into trichloroethylene (TCE) for 30 minutes, and then rinsed in acetone, 2-isopropanol (IPA), and deionized (DI) water. Finally, the silicon substrate was cleaned from any residual organic contamination by bathing it into a H_2SO_4 95%.:H_2O_2 33% (3:1) solution for 30 minutes at a temperature not exceeding 150 °C. After thorough rinsing with DI water and N_2 drying, a 200-nm nickel layer was subsequently e-beam evaporated on the substrate. These precautions allow us to unambiguously assert that the interface graphene films were fully generated by the plasma-assisted CVD process.

Before each PE-CVD deposition, the reactor was cleaned by oxygen plasma so that chamber walls do not supply unintended carbon. The substrate temperature is increased with a rate of 25°C per minute in a hydrogen atmosphere. As the substrate temperature reaches 450°C, a pre-treatment under hydrogen plasma is performed for 2 minutes (Figure 1. (a)), to help reducing the native oxide formed at the nickel layer surface. As schematized in figure 1. (b) and (c), DC plasma is first generated in a diode setup (between the anode grid and an intermediate cathode grid) by applying a 0.17 kW power to a CH_4:H_2 mixture (20sccm:50sccm). Pressure in the chamber was maintained at 2 mbars during the sample exposure to plasma. Once the primary plasma is established, a 160V bias is applied to the substrate holder in order to extract reactive species from the primary plasma at 50 mA intensity. Plasma exposure was varied from 1 to 12 minutes After this step the substrates are allowed to cool down while the reactor chamber is pumped out.

Further vacuum (10^{-5} mbars) annealing steps can be performed using a second furnace. The sample is charged on a quartz boat, allowing its transfer from the hot zone of the oven to a much cooler one (~150°C) at any time. The annealing procedures were as follows: *(i)* the sample is first transferred from the cool zone to the pre-heated hot zone (900°C) (see also figure 1.(e)), and annealed for 18 minutes. This annealing time is optimized to obtain relatively less number of layers and high crystalline quality. *(ii)* The heating is then shutdown and sample allowed to slowly cool down to 750°C before - *(iii)* being quenched down to 150°C (figure 1. (g)). Such quenching is assumed to freeze the graphene growth and to avoid the formation of thick graphene layers.

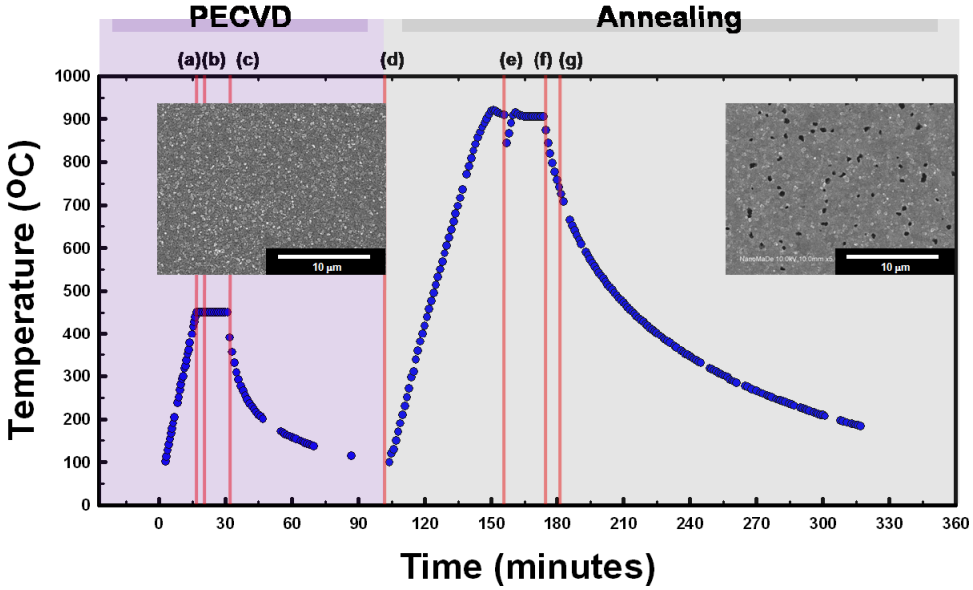

Figure 1. General graphene growth process based on plasma-assisted chemical vapor deposition (a) hydrogen plasma pre-treatment (b) carbon plasma exposure on nickel surface at 450 °C (c) cooling down and pumping out (d) amorphous carbon etching by oxygen plasma (e) sample holder loading into hot zone, 900 °C (f) cooling down (g) sample holder quenching out at 750 °C.

After the PE-CVD growth and the eventual additional annealing treatment, both the nickel surface and respectively its interface with SiO_2, were found to be covered by distinct graphene films. Subsequently the Ni layer was wet etched using commercial nickel etchant (Nickel Etchant TBF - Transene), either for transferring the top layer graphene to other substrates, or for freeing up the interface graphene attached to the silicon oxide. Top layer graphene on nickel surface may easily attach to, or get mixed with the interface graphene during this process. Accordingly, in the cases where we want to keep only the interface graphene, we applied strong water plasma prior to the nickel etching in order to remove all carbon-based materials on the nickel surface. Figure 1 summarizes the process of film fabrication.

The surface morphology of the films was probed using scanning electron microscopy (SEM) and their structure by transmission electron microscopy (TEM) and Raman spectroscopy. SEM was performed using a Hitachi S-4800 FE-SEM working at an accelerating voltage of 10 kV. TEM was performed at 120 kV using a Topcon 002B microscope. The cross-sectional samples for TEM were prepared by slicing and polishing using the tripod technique down to the thickness of ~5 µm and then ion milling. Raman spectra were acquired using a high-resolution (0.1 cm^{-1}) spectrometer (Labram HR800 from HORIBA Jobin Yvon) in a confocal microscope backscattering configuration. The objective used in this study was a 100× (NA = 0.9) objective from Olympus. Excitation was provided by a tunable Ar laser from Melles Griot (514-nm wavelength). For all the Raman analysis the collection time was 5 seconds with 2 accumulations.

3. RESULTS AND DISCUSSION

We have found that in our approach, the carbon exposure time is one of the dominant factors for graphene synthesis. This complete study will be later published; we will focus here only on the 12 minutes carbon-containing plasma exposure process.

Figure 2 shows TEM observations of the samples at different stages of our process. Interfacial graphene is found to be present after PE-CVD exposure as well as after annealing. The graphene films appear continuous over areas as large as several tens of nm and, quite surprisingly, more so before the additional annealing step. Plan-views of the top layer films transferred on classical TEM holey grids, indicate that the films consist of two phases: (1) a continuous background, and (2) bulky graphite blocks. Annealing has a visible effect on the latter: numerous with nanometre size before annealing, they are larger but fewer after annealing. Moreover, their structure consists in pillars or onions, with (002) planes parallel to the beam before annealing (002 diffraction spots visible in fig. 4b2), while they are flat with (002) planes in the substrate plane after annealing (no 002 diffraction spots visible in fig. 4d2). On the other hand, the graphene films

exhibit similar contrasts before and after annealing (but appear more sensitive to the electron beam before annealing). The selected area electron diffraction patterns (figs 4b1 and d1) show no obvious effect of the annealing on the structure of that background graphene: it appears in the two cases to consist of nano-crystalline grains, with random orientations in the plane. The line width indicates a coherence length smaller than 4 nm, which gives an order of magnitude of the size of the nano-grains. The absence of the 002 and 004 reflections confirm that the graphene crystallites are all oriented in the plane, as shown by the cross-sectional views.

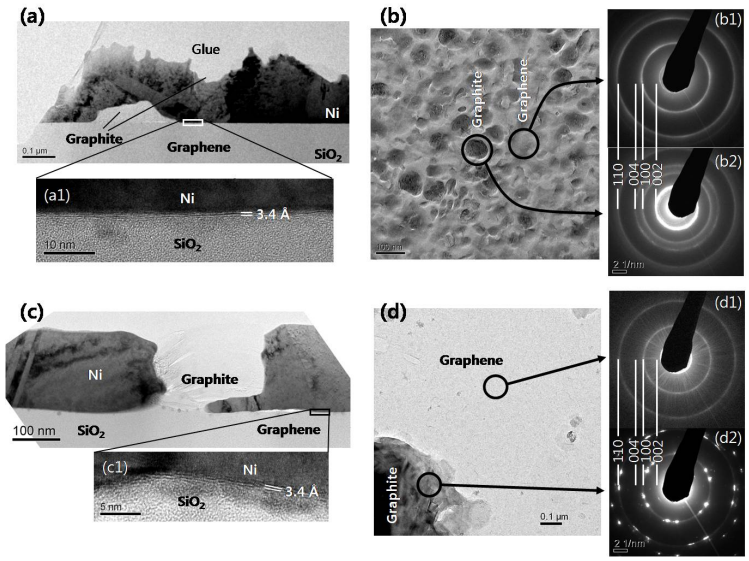

Figure 2. TEM images of the samples after growth by PE-CVD at 450°C for 12 min (a,b), and after an additional annealing treatment in vacuum at 900°C for 18 min (c,d). (a, c) cross-sections where graphite blocks and interfacial graphene can be seen in the two cases. The latter (a1, c1) appears continuous over several tens of nanometers, and more so before annealing. (b, d) plan views obtained after Ni etching, and depositing the remaining layer on a TEM holey-carbon grid. Images recorded in holey regions (no contribution of amorphous carbon). The diffraction patterns (b1 and d1) indicate that the background consists of nano-crystalline graphene, with random orientation of the nano-grains in the plane. Note the absence of 002 and 004 reflections indicating a good alignment of the graphene layers in the plane. The graphite blocks are small pillars or onions, with (002) planes parallel to the beam before annealing (b2), while they are flat with no (002) planes visible after annealing (d2)

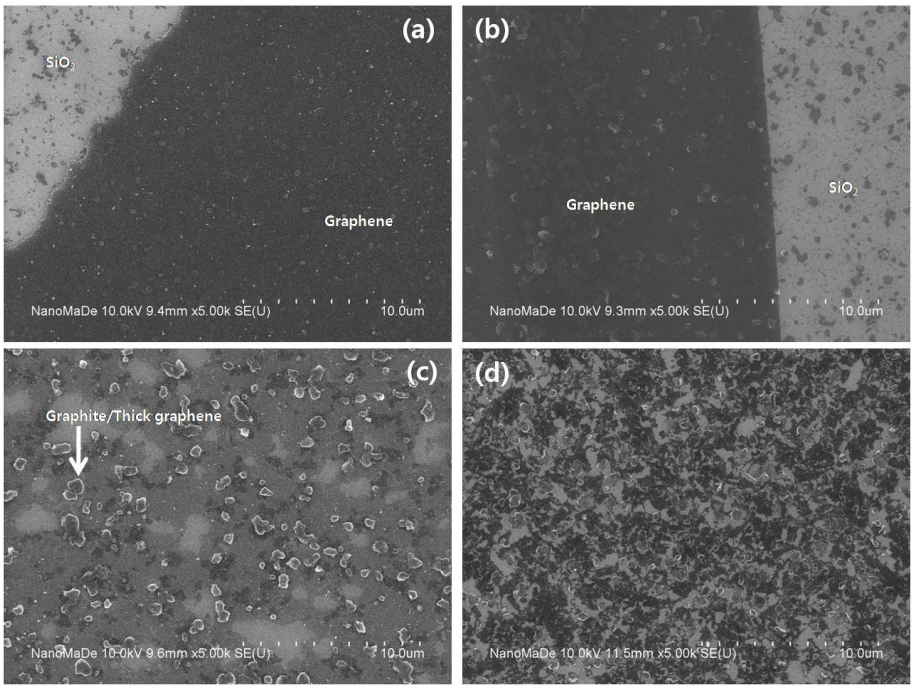

Figure 3. SEM images of the different types of graphene layers (a) Top layer graphene before annealing, (b) Top layer graphene after annealing, (c) Interface graphene before annealing (d) Interface graphene after annealing.

Figure 3 shows SEM observations of various graphene layers, at each processing step (before and after annealing) and for both locations (on nickel surface and respectively at the interface with the substrate). Figures 3 (a,b) were intentionally recorded at the edge of the graphene film in order to evidence a clear boundary with SiO_2 substrate. The graphene films grown on the nickel surface were transferred to SiO_2(300nm)/Si substrates by a conventional wet etching process. Let us mention that during this process, some of the interface graphene could also be mixed with top layer graphene, by Van der Waals interaction. In order to isolate uniquely the interface graphene, the top (on surface of the Ni layer) graphene film had to be removed prior the wet etch of the Ni layer. Our PE-CVD system is already equipped with water vapor plasma capability which allows efficient etching of carbon-based materials (graphene, amorphous carbon etc.) on nickel surface. After high power water vapor plasma exposure for 10 minutes, Raman and AFM analysis confirmed the complete removal of the top layer of graphene (not reported here).

We remark that, before annealing, the top and bottom films do not exhibit obvious differences, showing a rather continuous film features on the silicon oxide (see in figure 3. (a,b)). By contrast, after the additional annealing treatment, the morphologies of the two films significantly differ. Annealing process results in graphite-pillar formation (arrowed in figure 3c) probably related to further segregation and re-crystallization of the carbon. Such graphite pillar inclusions are impacting the quality of the produced graphene films. We found that lower carbon plasma exposure time helps reducing their surface density and can lead to the formation of continuous and uniform graphene layers.

The Raman analysis of the top/interface films confirms the SEM/TEM observations (Figure 4). Clearly, through additional annealing, the quality of the top layer graphene is enhanced, as the I_D/I_G ratio decreases from 1.7 to 0.8 and the I_{2D}/I_G ratio increases from 0.4 to 1.2. Concerning the interfacial graphene layer, the overall quality of the film does not change and we noted a clear trend towards increasing the number of graphene layers upon annealing.

Although the structure of interface graphene is still defective, regardless of annealing step, our study clearly paves the way to realizing the graphene films without transfer process. Further optimization of the plasma process and theoretical prediction in thermal-related carbon dynamics let us think that a cost effective, low temperature and large-area direct graphene growth process is achievable.

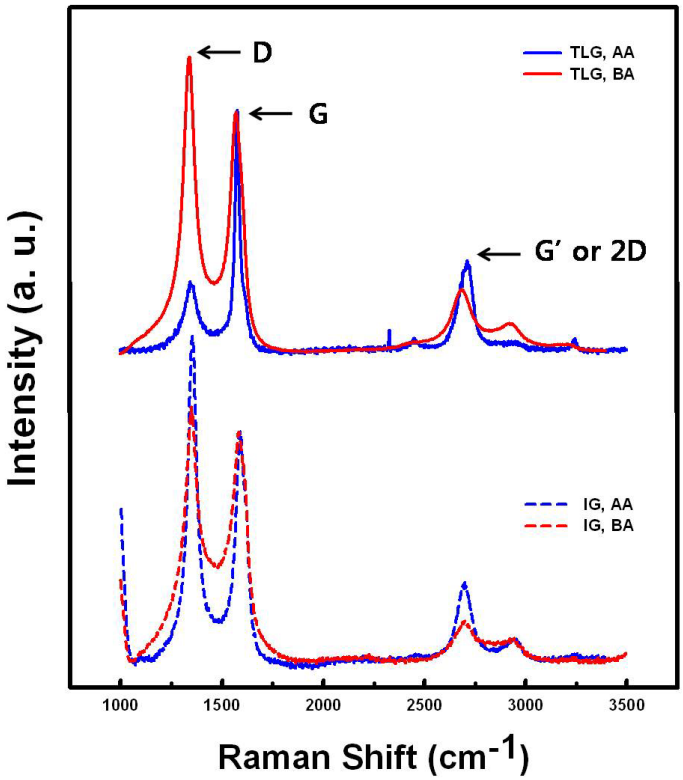

Figure 4. Raman spectra of transferred graphene layer at each step and at each position . TLG: transferred graphene, IG: interface graphene, BA: before annealing, AA: after annealing.

4. CONCLUSION

In conclusion, we have introduced the first low-temperature, dual graphene films growth process based on plasma-assisted chemical vapor deposition. Moreover, the crystalline quality of top layer graphene is observed to be enhanced through an additional annealing process, whereas the quality of the interface graphene does no significantly improve. Annealing process can also induce a structural change through the formation of graphite pillars into the nickel layer. These structures generally interconnect between the two distinct graphene layers.

Our approach, allowing the growth of graphene films directly on insulating substrates at low temperature (450 °C), could be extremely useful to override the transfer step still required by the classical CVD synthesis techniques. Finally, the films grown seem to be made of an arrangement of nanometric crystals rather than large graphene crystals. At this point, work is still under strong development, focusing on the understanding of the phenomena allowing the carbon species delivered by the plasma at the surface of the catalyst to diffuse to the nickel/silicon oxide interface. Understanding these phenomena will be crucial for further increasing the quality of the interface graphene film during the low-temperature process itself.

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