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C-Plane Sapphire and Catalyst Confinement Enable Wafer-Scale High-Quality Graphene Growth

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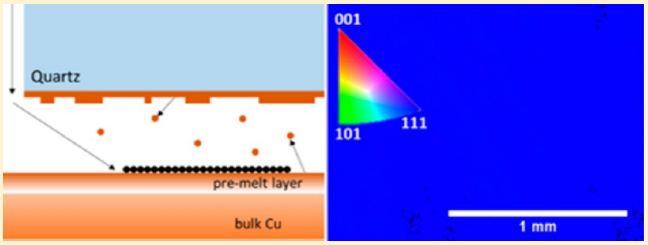
Supporting Information

ABSTRACT: Herein we report a systematic study elucidating the role of H_2 in wafer-scale graphene synthesis on a Cu thin film using catalyst confinement (CC) and a C-plane sapphire substrate. Our process results in extremely flat and wrinkle-free graphene when coupled with a dry transfer process. The role of H_2 was investigated by variation of the H_2:CH_4 flow ratio that, when optimized, was able to mitigate Cu catalyst roughening. This allows the Cu catalyst to maintain large monocrystalline grains extending several centimeters across growth wafers and predominantly in the Cu(111) orientation. The ultimate results are high-quality, continuous, and large-area graphene sheets. A comparison of graphene formation using the CC process with C-plane sapphire substrate and SiO_2/Si wafers was conducted. The results highlight the benefits of using C-plane sapphire as substrates in contrast to SiO_2/Si wafers on which highly roughened catalyst surfaces are usually formed leading to a high density of wrinkles in the graphene sheets as well as bilayer graphene growth at the Cu grain boundaries. Throughout the investigation, graphene quality was evaluated by Raman spectroscopy and Cu catalyst orientation was determined by electron backscatter diffraction (EBSD). Graphene field effect transistors (GFETs) were fabricated to examine the electronic properties by transferring the graphene from the Cu/C-plane sapphire wafers and from Cu/SiO_2/Si wafers to SiO_2 substrates using a dry-transfer process developed in house. The CC and Cu/C-plane sapphire-based GFETs exhibit a charge carrier mobility as high as 3781 $cm^2\ V^{-1}\ s^{-1}$.



INTRODUCTION

Graphene has attracted considerable attention since its first experimental isolation owing to its exceptional properties.[1−4] Initial isolation was achieved with mechanical exfoliation of natural graphite crystals, but the method was not suitable for mass production.[5] Although various fabrication methods have been investigated, chemical vapor deposition (CVD) is recognized as an effective technique to achieve the goal of high-quality, large-area graphene sheets suitable for electronic device fabrication. For CVD growth of graphene, the catalyst is one of the most critical parameters. First attempts were made with nickel (Ni) and iron (Fe) catalyst materials resulting in inhomogeneous films dense in bilayer regions when attempting to tune toward monolayer graphene using carbon segregation.[6] Later, rapid thermal annealing (RTA) was introduced to produce monolayer graphene.[7] Copper (Cu) catalysts were first introduced by Li and co-workers and were demonstrated to exhibit a self-limited growth characteristic, which was attributed to the relatively low carbon solubility in Cu as compared to Ni and Fe.[8] Recent advancements in CVD graphene using Cu catalyst have greatly refined this process and even identified the parameters required to grow multilayer graphene resulting from variations in the Cu surface morphology.[9] Other critical parameters were investigated such as hydrogen (H_2) concentration relative to carbon precursor and gas versus liquid phase precursors.[10−12] The vast majority of high-quality graphene to-date has been grown using Cu foils as both catalyst and substrate. There are several suppliers offering Cu foil, such as Sigma-Aldrich and Alfa Aesar, suitable for this fabrication technique, which has resulted in a handful of successful companies offering graphene to both industrial and academic customers.

CVD of Cu foil-based graphene has become ubiquitous in academic research; however, it still presents several challenges for adoption into the semiconductor industry. For back end of the line (BEOL) applications, which include interconnects and dielectrics utilized for connection of individualized devices, the most critical requirement is the need for a low-temperature direct deposition process, preferably on a dielectric, for an appropriate-quality graphene for the given, specific application. For a front end of the line (FEOL) application where devices are formed and isolated in a planar geometry application, a growth and mechanical transfer process may be feasible although many improvements are still needed for both the growth and transfer steps. For integration, growth temperature is generally not an issue. Reliability and repeatability of the transfer process and the challenges associated with the lack of rigidity of metal foils and variability of the Cu foils from

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different suppliers (related to quality, cleanliness, and morphology) are of critical importance. Using thin film Cu as the catalyst supported by a wafer presents a solution to many of these problems. For example, consider the following four benefits: (1) the Cu catalyst is supported by a rigid wafer substrate that prevents mechanical deformation of the graphene/Cu film, (2) Cu thin films can be deposited by several low-cost physical vapor deposition (PVD) methods such as sputtering, thermal evaporation, electron beam evaporation, and electroplating, (3) purity of the Cu thin film can be easily controlled by aforementioned PVD processes, and (4) wafer-based synthesis of graphene is most compatible with current semiconductor industry fabrication processes.

Despite the advantages offered by utilizing a Cu thin film catalyst on rigid substrates, other challenges have prevented widespread adoption from this technique as it has a larger sensitivity to process parameter variations due to the crystalline uniformity of Cu thin films ~1 μm or thinner compared to thick Cu foils ~25 μm thick. Additionally, Cu has an intrinsically poor adhesion to SiO_2, the most commonly employed catalyst support for Cu thin films, which results in pinholes, voids, and sometimes complete delamination of the Cu thin film from the SiO_2 wafer during a growth process. To prevent pinhole and void formation, one could increase thickness of the Cu layer; however, the growth temperature must be increased in compensation.[13]

To improve mechanical stability, some have introduced caps to place over the growth substrate where they used folded pockets of Cu foils to improve graphene growth characteristics and achieved graphene crystal domains up to 0.5 mm on a wafer substrate using a tube furnace CVD system.[14] Following this development there has been effort to recreate the Cu foil pocket growth with other CVD reactor configurations such as a vertical cold-wall furnace resulting in reduced process time.[15] Although these improvements afforded by analogous pocket growth have resulted in better graphene with large single crystal domains, they still present issues with scalability, graphene handling, and transfer as well as the lacking of control for Cu source materials when using Cu foils as a graphene catalyst.

In the literature, there are several examples of studies comparing growth of graphene on various Cu crystalline orientations has indicated that Cu(111) results in the highest-quality graphene demonstrated by the reduced Raman D:G intensity ratio ($I_{D/G}$).[16−18] Scanning tunneling microscope (STM) studies comparing graphene grown on Cu(100) versus Cu(111) reveal that a uniform sheet of graphene is grown on Cu(111) surfaces with quality dictated by grain boundaries whereas graphene grown on Cu(100) results in incomplete graphene growth with nanoscale edges and enhanced $I_{D/G}$.[19] To further pursue the formation of large-scale Cu thin film with a Cu(111) orientation, many of the aforementioned studies have utilized C-plane sapphire[20] to form epitaxial Cu films while specific Cu thickness and process conditions could result in a predominantly Cu(111) orientation of a recrystallized Cu on SiO_2/Si.[13] Although these studies advanced the understanding of graphene growth on crystalline Cu thin film supports, the study for how to precisely control the Cu catalyst morphology in relation to the optimization of other growth parameters in a confined growth environment toward achieving high-quality and wafer-scale graphene is missing.

In this paper, we demonstrate for the first time that high quality and large areas of graphene can be achieved using the combination of C-plane sapphire supported Cu thin films and a cold wall reactor system equipped with catalyst confinement (CC) capability. This growth process was able to achieve thin film Cu grains spanning from hundreds of micrometers to several centimeters. The largest Cu grains result in the flattest graphene with fewest wrinkles and bilayer islands. Also, high stability of the Cu catalyst was attained due to improved adhesion of the Cu catalyst to the C-plane sapphire in comparison to Cu catalyst on SiO_2. A comparative study presented in this report reveals the advantages of using Cu/C-plane sapphire for graphene fabrication versus using Cu/SiO_2/Si, with both being studied in a CC environment. It was also found that H_2 has three important roles in a CC growth environment by modulating the roughness of the Cu catalyst, controlling the crystallization of Cu, and catalyzing the generation of reactive $(C_xH_y)_s$ radicals for nucleation of graphene growth.

A photo of the reactor used for this study is depicted in Figure 1a. For the graphene growths presented in this study, a typical thermal profile illustrating the recipe used is presented in Figure 1b.

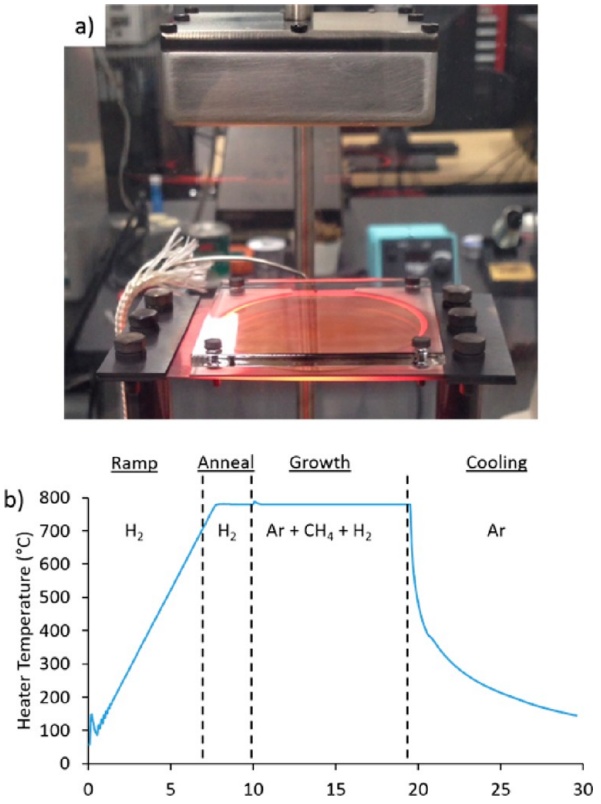

Figure 1. (a) Photo of graphene growth reactor used in this study, in-process. Note the quartz plate fixed above the C-plane sapphire/Cu wafer to enable the catalyst confinement environment. (b) Measured heater temperature versus process time demonstrating the different stages of the graphene growth process used in this study.

The cooling phase is achieved by removing power from the resistive heater upon completion of the growth time.

RESULTS AND DISCUSSION

C-Plane Sapphire-Supported Cu Graphene Growth. The particular orientation of C-plane sapphire was chosen due to the crystalline symmetry and low lattice mismatch compared to Cu(111), which subsequently provides the ideal Cu substrate

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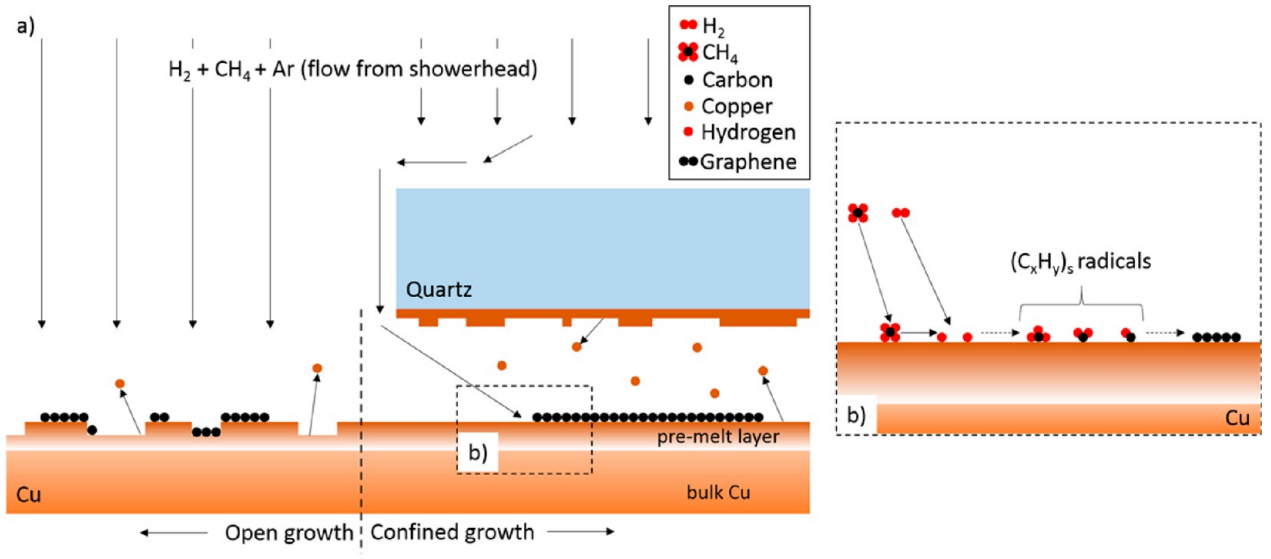

Figure 2. (a) A schematic comparison between open and confined graphene growth. Open growth allows direct flow of gases from the showerhead and the largest vacuum gradient between the evaporating Cu from the premelted layer and the chamber. In contrast, the confined growth method blocks the direct flow of gases to the Cu surface and localizes the evaporated Cu catalyst thereby increasing the surface-bound lifetime of Cu and C surface species during graphene growth thereby enhancing graphene stability during growth. (b) An expanded view of the chemical reactions occurring on the surface is depicted to the right.

for epitaxial graphene growth. Because of the improved stability, the Cu/C-plane sapphire wafers are able to maintain uniformity without production of Cu film voids while varying the level of H_2 and keeping the CH_4 flow constant at the lowest attainable level with our current setup (10 sccm). The flow rate of CH_4 was kept low to further reduce nucleation density of graphene, thereby increasing the average graphene grain size. The distance between the quartz plate, to achieve CC, and the Cu/C-plane sapphire wafer was kept constant at 3 mm and will hereafter be referred to as the offset. The growth series for C-plane sapphire-supported Cu was defined as varying the flow of H_2 from 690 sccm (maximum of mass flow controller on current setup) to 100 sccm and defined the H_2:CH_4 values of 69:1, 50:1, 30:1, 20:1, and 10:1. H_2 serves a critical role in both the production of graphene and the crystallization of Cu. H_2 delivered to the surface of the Cu catalyst results in dehydrogenation of methane, resulting in the production of highly reactive and surface-bound $(C_yH_x)_s$ molecules that are able to serve as a seed for graphene growth.[10] This effect is illustrated in Figure 2a,b where a schematic of the overall growth in Figure 2a demonstrates the difference between open and confined growth and the inset of Figure 2b is then expanded to depict the formation of $(C_xH_y)_s$ radicals. These radicals stick to the Cu surface and form graphene crystals once the $(C_xH_y)_s$ radicals have come to a critical size where they begin to expand into a graphene as opposed to evaporating with the most energetic atoms of the premelted Cu metal surface.

H_2 also enables etching of carbon resulting in varying graphene growth morphology dependent upon the partial pressure of H_2 during growth.[10] Besides directly influencing the formation of graphene, H_2 is known to increase the mobility of surface Cu atoms during thermal processing and, at certain concentrations, will produce wedge-like grain boundaries where Cu atoms are highly mobile during the thermal process due to surface diffusion of Cu.[21] In contrast to SiO_2-supported growth where an abundance of twinning and wedge-like morphology is observed, C-plane-supported Cu has predominantly Cu(111) crystallographic orientation due to the underlying sapphire acting as a template during thermal processing. However, we do observe the formation of wedge-like grain boundaries only at high H_2 partial pressures. These defects were most likely accompanied by combination of screw and edge dislocations known to exist between nearby Cu(111) crystal grains.[18] This effect is clearly demonstrated in Figure 3a,d,g,j,m as H_2 partial pressure is decreased, the apparent roughening of the as-grown graphene surface decreases. The roughest graphene surface (as shown in Figure 3a–c) appeared when a high H_2:CH_4 ratio of 69:1 was applied.

For every H_2:CH_4 flow ratio used, the Cu catalyst demonstrated a majority Cu(111) orientation as depicted in the inverse pole figure-z (IPF:Z) maps in Figure 3b,e,h,k,n. However, the relative orientation and grain boundaries varied for each H_2:CH_4 flow ratio and relative Cu grain orientation was monitored with Euler maps as seen in Figure 3c,f,i,l,o. The Cu crystal orientation of the Cu catalyst thin film coalesces to single orientation (i.e., single crystal) at H_2:CH_4 of 30:1 and 20:1 as indicated by both IPF:Z plots (Figure 3h,k) and Euler maps (Figure 3i,l). These samples were mapped over a millimeter scale (hemispherical pole figures of all growths available in Supporting Information SI.1) and exhibited the same crystallographic characteristics as depicted in Figure 3. At the lowest H_2:CH_4 tested, 10:1, the Cu film still maintains the orientation of Cu(111) (Figure 3n); however, the Euler map (Figure 3o) demonstrates a lack of a single Cu crystal orientation. This effect demonstrates one of the major, three roles that H_2 plays with Cu thin film graphene growth. First, H_2 controls the mobility of the Cu during thermal processing. As H_2 flow is increased, it is likely the Cu mobility (i.e., surface Cu diffusion rate) increases proportionally. At a H_2:CH_4 of 10:1, where the H_2 is at the lowest level studied, the smoothness of the graphene surface is much improved. However, the overall orientation is not allowed to approach a single crystal due to lack of H_2. An increase to 20:1 decreases in-plane orientation mismatch (Figure 3l) while still maintaining Cu(111) orientation (Figure 3k).

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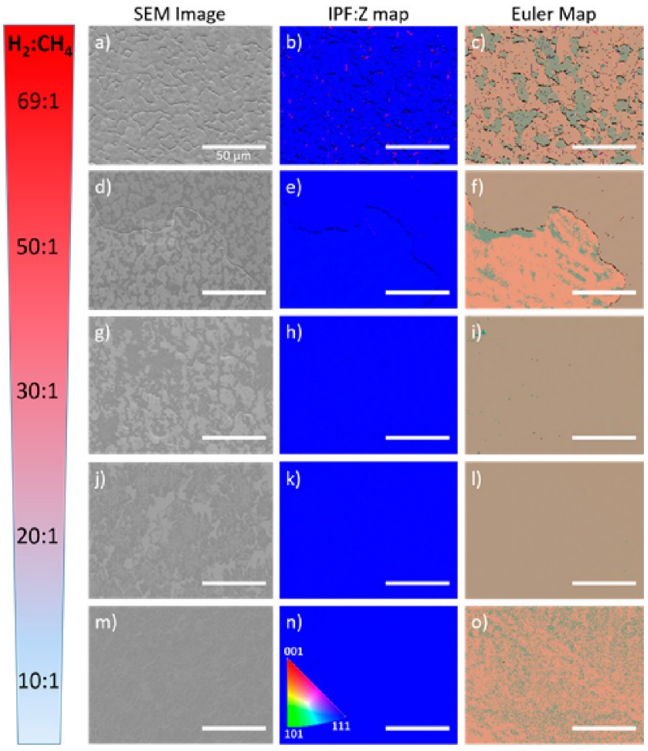

Figure 3. SEM images with corresponding electron backscatter diffraction (EBSD) inverse pole figure-z (IPF:Z) maps, Euler maps, and IPF:Z plots for H_2:CH_4 flows of 69:1 (a–c), 50:1 (d–f), 30:1 (g–i), 20:1 (j–l), and 10:1 (m–o). All scale bars represent 50 μm. Data were acquired at 20 keV.

Second, H_2 is also utilized for control of the graphene morphology and growth dynamics.[22] It absorbs onto the Cu catalyst surface and dehydrogenates a CH_4 molecule, thereby creating a reactive $(C_xH_y)_s$ species capable of nucleating graphene growth. At the same time, H_2 etches weak C–C bonds favoring the hexagonal structure of graphene in the presence of Cu.[23] These effects are demonstrated in Figure 4 where SEM characterization was performed for samples made at different H_2:CH_4 ratios. First, the graphene nucleation density can be inferred from the bilayer density present of the surface of the as-grown graphene monolayer. At a H_2:CH_4 of 69:1, the bilayer density is the highest (Figure 4a) with bilayer density gradually decreasing as the H_2 flow was decreased (Figure 4a,c,e,g,i). The bilayer island density versus H_2:CH_4 flow was extracted using image analysis over several regions of each sample and is presented in Figure 4k. The bilayer island density follows an exponential relationship (blue dashed line represents exponential fit) and demonstrates the importance of H_2 in graphene growth dynamics.

Third, the effect of H_2 can be seen with the shape of the graphene bilayer islands. As the H_2:CH_4 flow ratio is decreased, the bilayer islands go from a hexagonal shape (Figure 4b) to a gradually more amorphous structure as seen in Figure 4j. Presumably, the reduction of H_2 will reduce the number of weak C–C bonds, which results in a continuum of graphene morphology from symmetric circular shapes to highly dendritic.[22] The onset of dendritic-like growths appear at a H_2:CH_4 of 50:1 as seen in Figure 4c (dark veins with lobed edges) and continue to increase in dendritic form from 50:1 to 10:1.

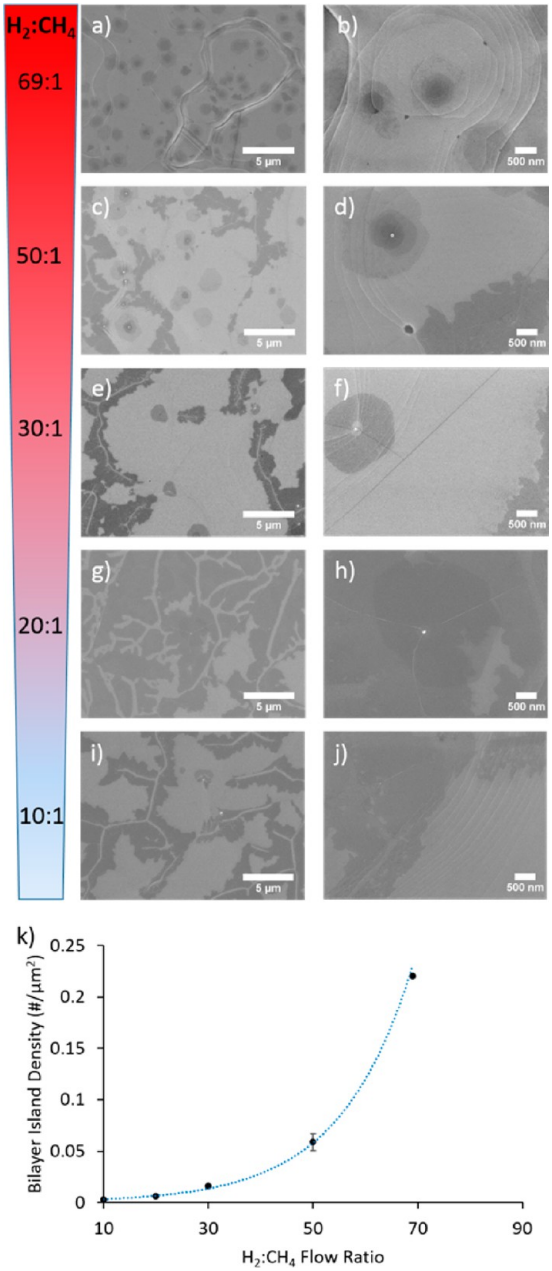

Figure 4. SEM images of the graphene growth series varying the flow rate of H_2 while holding the CH_4 flow rate constant for H_2:CH_4 values of 69:1 (a, b), 50:1 (c, d), 30:1 (e, f), 20:1 (g, h), and 10:1 (i, j). (k) Bilayer island density versus H_2:CH_4 flow ratios for the entire graphene growth series. The bilayer density was extracted with SEM image analysis over several sites on each as-grown graphene wafer. Bilayer density as a function of H_2:CH_4 flow rates follows an exponential trend with increasing H_2. Low-magnification SEM images (left column) are supplied to demonstrate the differences in graphene bilayer island density while high-magnification SEM images (right column) supply detailed graphene morphology on the Cu thin film catalyst. SEM images were acquired at 5 keV.

In order to relate the morphology of the as-grown graphene to its quality, all samples were transferred to SiO_2/Si wafers with 300 nm of thermal oxide. During this study, a unique transfer method was developed that was inspired by work from Lee et al.[24] To assess graphene quality, Raman spectroscopy of each transferred graphene wafer was performed by recording spectra from the top, bottom, left, right, and center of each

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transferred graphene wafer. The five spectra for each wafer were then averaged and are plotted in Figure 5a for each H_2:CH_4

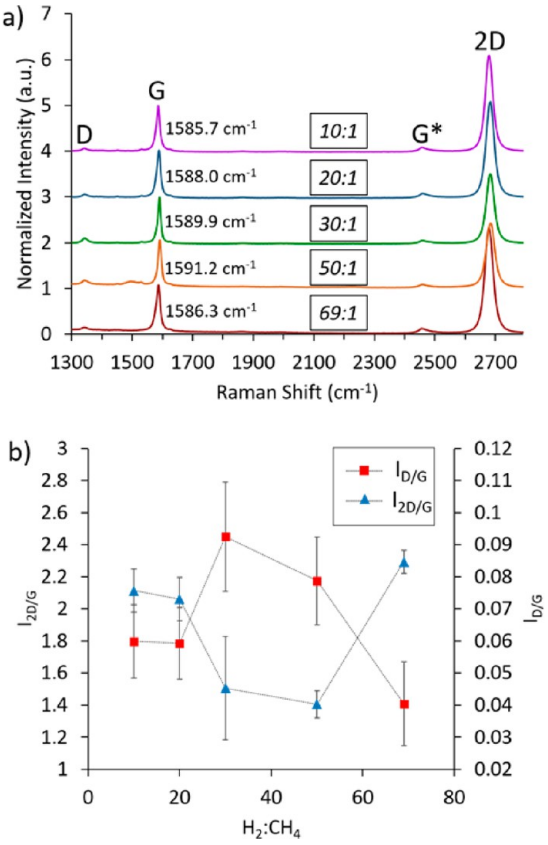

Figure 5. (a) Stacked Raman spectra plot (all normalized to G peak intensity) for each H_2:CH_4 with 69:1 (purple), 50:1 (blue), 30:1 (green), 20:1 (orange), and 10:1 (red). All spectra were averaged from five positions on the transferred graphene wafer (bottom, left, right, center, top). G-peak positions are labeled for each spectrum. (b) $I_{D/G}$ and $I_{2D/G}$ plotted versus all H_2:CH_4 growth conditions. Average values and error bars derived from five different sampling locations as in (a).

flow ratio. Each of the five spectra was analyzed individually to create a plot exhibiting the trend of $I_{D/G}$ and $I_{2D/G}$ with H_2:CH_4 as seen in Figure 5b. The G-peak position for each average Raman spectrum is presented in Figure 5a. All but the sample with a H_2:CH_4 of 20:1 have G-peak positions between 1580 and 1590 cm^{-1} indicating low doping levels.[25] Interestingly, the sample with the lowest G-peak position (H_2:CH_4 of 69:1) also possesses the most promising values of $I_{D/G}$ = 0.040 and $I_{2D/G}$ = 2.29. The next, most promising samples have a H_2:CH_4 of 20:1 ($I_{D/G}$ = 0.059, $I_{2D/G}$ = 2.06) and 10:1 ($I_{D/G}$ = 0.060, $I_{2D/G}$ = 2.11) as demonstrated in Figure 5b. Increasing H_2 from 20:1 both increases $I_{D/G}$ and decreases $I_{2D/G}$ until 69:1.

Both H_2:CH_4 flow ratios of 10:1 and 69:1 result in the best graphene quality suggested by Raman spectroscopy results. Contrary to other graphene growth studies using thin film Cu, a high flow ratio of H_2:CH_4 is necessary to attain the best quality graphene as determined by Raman spectroscopy; however, graphene bilayer density increases exponentially from H_2:CH_4 flow ratios of 10:1 to 69:1 as shown in Figure 4k. In addition to the samples with H_2:CH_4 of 10:1, and 69:1 resulting in low $I_{D/G}$ and high $I_{2D/G}$ values, they were the only samples to exhibit a 2D peak fwhm <30 cm^{-1} of 29.7 and 28.8 cm^{-1}, respectively, further indicating the majority presence of monolayer graphene. However, as seen in Figure 4k, the bilayer density for a H_2:CH_4 flow ratio of 69:1 is by far the highest at ~0.22 bilayer islands per μm^2. It has been established that bilayer graphene sheets, which deviate from AB stacking have a red-shifted G peak.[26] Here, the H_2:CH_4 flow ratio of 69:1 results in both a red-shifted G peak and narrowed 2D peak; however, the 2D peak was red-shifted compared to other growths. The CC growth regime allows H_2, with a higher diffusivity than that of CH_4, to have an even higher H_2:CH_4 partial pressure ratio inside the CC chamber compared to the remainder of the growth chamber. Then, it is likely the H_2 will etch the graphene anisotropically, and Zhang et al. established that 800 °C is the optimal temperature for etching graphene anisotropically with an angle of 120° and dominated by the zigzag edge.[23] This can explain both the reduced $I_{D/G}$ (Figure 5a) and hexagonal shape of the graphene bilayer islands (Figure 4b) for growths with a H_2:CH_4 flow ratio of 69:1. The graphene growths with a H_2:CH_4 flow ratio of 10:1 has nearly 7 times less H_2 and results in less anisotropic etching as evidenced with a larger $I_{D/G}$ (Figure 5a). However, this does not account for the increased $I_{D/G}$ for every other H_2:CH_4 flow ratio used. We believe the graphene growths with H_2:CH_4 flow ratios of 50:1, 30:1, and 20:1 have a mix of zigzag and nonzig zag terminations forming during the growth process as evidenced by the shift from hexagonal graphene bilayer islands to circular bilayer islands as depicted in Figure 4b,d,f,h going from H_2:CH_4 flow ratios of 69:1 to 20:1. A typical growth and transfer of graphene using 69:1 is demonstrated in Figure 6. The as-grown graphene sample is

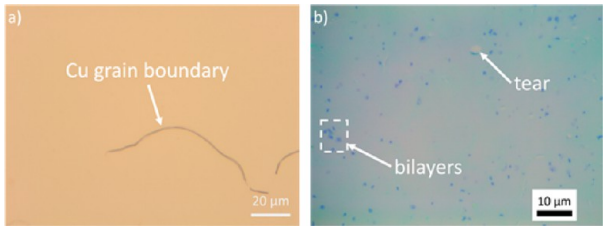

Figure 6. (a) Optical bright-field image of as-grown graphene on Cu thin film on C-plane sapphire substrate and (b) graphene transferred to a SiO_2/Si wafer with 300 nm of thermal oxide.

quite flat in appearance due to the Cu(111) orientation provided by the C-plane sapphire template and optimized growth conditions (Figure 6a). After implementing our dry transfer technique, the graphene demonstrates little to no tears and no visible graphene wrinkles by optical inspection (Figure 6b).

The best sample as indicated by both Raman spectroscopy and SEM inspection for lower bilayer density with a H_2:CH_4 flow ratio of 10:1 was then transferred to a SiO_2/Si wafer with degenerately doped Si for fabrication of graphene field effect transistors (GFETs). Each GFET consisted of a graphene nanoribbon (GNR) patterned into a six-terminal hall bar with noninvasive contacts that allowed four-point measurements and determination of intrinsic channel electronic transport properties. The degenerately doped Si substrate was used as a global backgate with a 300 nm SiO_2 gate dielectric. Typical graphene ribbon dimensions with width of 3.5 μm and channel length of 9 μm were used for the purpose of extracting the most accurate intrinsic graphene carrier mobility. An optical bright-field image of an as-fabricated GFET is pictured in Figure 7a. The hole and electron mobility were extracted by utilizing the global backgate, and the resulting curve is presented in Figure 7b.

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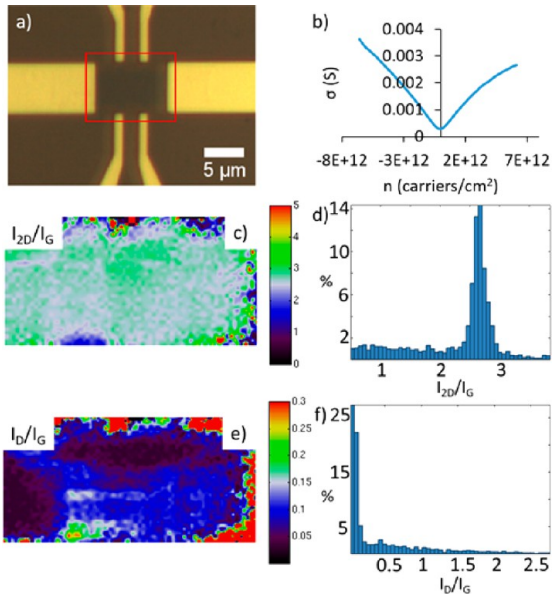

Figure 7. (a) Optical bright-field image of a six-terminal GFET fabricated from the dry-transferred graphene growth with a H_2:CH_4 = 10:1. (b) Dirac curve of the GFET pictured in (a) demonstrated μ_{max} = 3781 $cm^2/(V\ s)$. $I_{2D/G}$ (c) and $I_{D/G}$ (e) Raman map of the GFET channel with corresponding histograms (d, f). Raman maps and histograms were processed using GRISP v1.2[30].

The electron and hole mobility were determined by using the following relationship[27]

$$R_{tot} = R_c + R_{ch} = R_c + \frac{L/W}{e\mu\sqrt{{n_0}^2 + {n_{BG}}^2}}$$

where R_{tot} is the total resistance of the device under test, R_c is the contact resistance, R_{ch} is the graphene channel resistance, L/W is the aspect ratio of the graphene channel, e is the unit charge of an electron, n_0 is the residual charge carrier concentration, and n_{BG} is the charge carrier density, which is dependent upon the backgate voltage. Peak electron and hole mobility was measured to be 3437 and 3781 $cm^2/(V\ s)$, respectively. A Raman map was acquired for the device pictured in Figure 7a. The $I_{2D/G}$ map in Figure 7c along with the histogram in Figure 7d, generated from the $I_{2D/G}$ map, demonstrate that the graphene is predominantly monolayer with an average $I_{2D/G}$ = 2.3 and the mode $I_{2D/G}$ = 2.6. The $I_{D/G}$ map and histogram (Figure 7e,f) indicate the graphene channel has a low $I_{D/G} \sim 0.05$ with some areas shown $I_{D/G} < 0.1$ likely due to the effect of device fabrication processing.

SiO_2-Supported Cu Graphene Growth. To compare the quality of graphene grown on Cu supported by C-plane sapphire with that of Cu supported by SiO_2, we conducted a series of graphene growth experiments. Our results suggest that Cu supported on SiO_2 is difficult to optimize for thermal graphene growth due to weak adhesion of Cu to SiO_2. Without using CC, the Cu film destabilizes from the SiO_2 and forms voids, pinholes, and sometimes completely delaminates during the ramp phase of the growth recipe.

The quartz plate offset and the Cu/SiO_2/Si wafer was varied between 9 and 3 mm. At an offset setting of 9 mm, the Cu film loses its stability and allows large voids to be formed during the growth process (Figure 8a). This causes a significant amount of Cu to be evaporated onto the quartz plate. Low-quality graphene is found within the voids and is presumably left

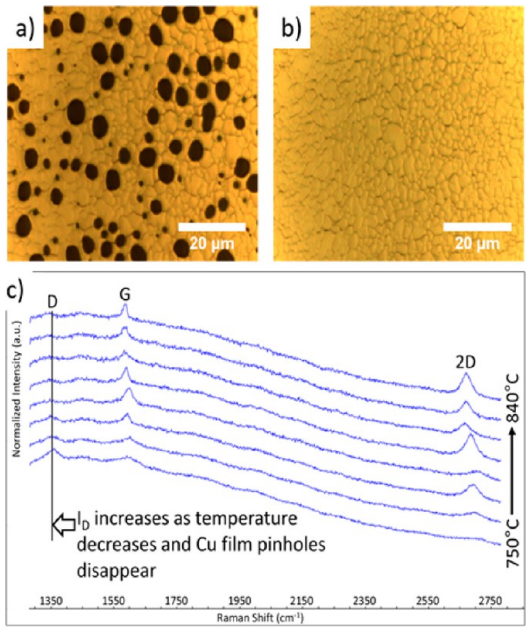

Figure 8. (a, b) As-grown graphene on Cu/SiO_2/Si wafer using 9 and 3 mm spacer offset, respectively. Note the pinholes and voids present in the Cu catalyst due to increased Cu evaporation in (a) when using 9 mm spacer offset. (c) Raman spectra of graphene on Cu, using a 3 mm spacer offset, for a thermal growth series demonstrating the reduction of the D peak. Growths were accomplished from 750 to 840 °C in 20 °C increments. However, at 780 °C the Cu film loses stability and resulted in pinholes, voids, and sometimes delamination during the growth process.

behind after the Cu has evaporated during the growth phase.[28] By reducing the number of alumina spacers to achieve an offset distance of 3 mm, the voids are mitigated and the resultant growth was uniform across the entire wafer (Figure 8b). This result was obtained using the same growth conditions as when using a 9 mm offset and allowed for uniform graphene growth at elevated growth temperatures.

Raman spectroscopy was used to monitor the graphene on Cu to monitor the reduction of $I_{D/G}$ with increasing growth temperature (Figure 8c) and $I_{D/G}$ reduced with increasing temperature and the Cu film would develop voids above 780 °C. Therefore, 780 °C was chosen as the optimized growth temperature—a compromise between Cu film stability and graphene quality.

To achieve both low defect density and improve the grain size of the Cu film, our results suggest that the quartz plate must be cleaned of evaporated Cu from a previous growth, also known as "seasoning", so that Cu grains can increase in size with increasing growth temperature (Figure 9a–c). Contrary to results in Figure 8, which used a seasoned quartz plate, the growth temperature could be increased while maintaining Cu film stability with a cleaned, quartz plate. Any growth processes performed >790 °C resulted in pinholes and voids forming within the Cu thin film, therefore disrupting continuity. After transfer, the optimized, 790 °C growth on SiO_2/Si demonstrated cracking likely derived from large gaps formed between Cu grains.

Without cleaning of the quartz plate, the residual Cu layer from "seasoning" prevents the Cu grains from increasing in size and is insensitive to growth temperature. The onset of Cu crystal grain growth was observed at a heater temperature of 770 °C (Figure 9a), increasing gradually at 780 °C (Figure 9b)

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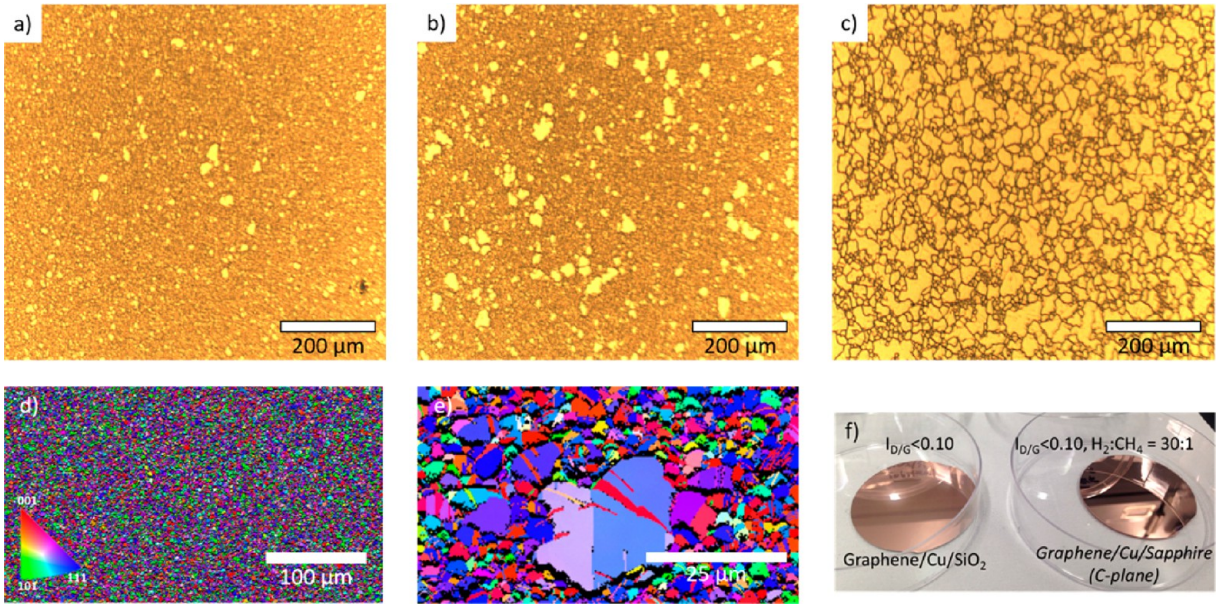

Figure 9. (a–c) Optical bright-field microscope images of as-grown graphene of 770, 780, and 790 °C, respectively. The average Cu grain size enlarges as temperature is increased only by using catalyst confinement. Beyond 790 °C the Cu film destabilizes and results in delamination and pinhole formation, thereby disrupting continuous graphene sheet growth. (d) SEM EBSD map of the 790 °C sample over a large area. (e) Enlarged section of map in (d) demonstrating large amounts of Cu grain twinning and heterogeneity of crystal lattice projected out of plane. (f) Photos of as-grown graphene wafers supported by SiO_2 (left) and C-plane sapphire (right). The inherent smoothness of the sapphire supported sample is demonstrated with less diffuse reflection.

and reached a maximum size at a heater temperature of 790 °C (Figure 9c). The largest Cu crystal grains observed were up to ∼80 μm in length, which are some of the largest observed using similar methods, yet the offset used in this study is much larger at 3 mm and the total growth process is 35 min. In comparison to the C-plane sapphire supported Cu graphene growths, the resulting Cu crystalline orientation was more random as demonstrated in Figure 9d and the enlarged map in Figure 9e. A macro view of the 2 in. diameter as-grown graphene wafers comparing SiO_2 and C-plane supported Cu thin film catalyst is depicted in Figure 9f. The C-plane sapphire supported Cu is shinier due to the larger Cu grains, and in the case of Figure 9f, which depicts the as-grown graphene wafer with a H_2:CH_4 flow ratio of 30:1, the Cu grains extend over several millimeters.

To compare between the differences in graphene quality on the different resultant Cu grain sizes depicted in Figure 9a–c, the graphene was transferred to SiO_2/Si wafers with 300 nm thermal oxide. It was found that there exists a compromise between graphene quality as determined by Raman spectroscopy and the resulting morphology post-transfer. The as-grown graphene wafers with the smallest Cu grains were grown at a heater temperature of 770 °C and resulted in a transfer with excellent uniformity and lacking any visible cracks or wrinkles (Figure 10a). However, $I_{D/G}$ for this sample is ∼0.15, which is relatively low-quality graphene (Figure 10d). In contrast, the as-grown graphene wafer with emergence of large Cu grains and a heater temperature of 780 °C results in $I_{D/G} \approx 0.11$. This trend continues as the density of cracks in the transferred graphene increases along with a decrease of $I_{D/G}$ to ∼0.06 for a growth temperature of 790 °C (Figure 10c). The compromise is then observed in Figure 10c where cracks form in the graphene post-transfer following the increase in gaps formed at Cu grain boundaries. This graphene has improved quality as determined by Raman spectroscopy; however, it is not ideal for device array fabrication with such a high crack density.

To summarize our findings using both Cu/C-plane sapphire and Cu/SiO_2/Si support wafers, graphene growth by a cold-wall reactor equipped with CC empowers a unique fabrication system more amenable to semiconductor industry owing to utilization of rigid wafer supports (as compared to flexible Cu foils) and relatively short process times. Especially, the resistive graphite heater offers rapid heating and cooling capability while the use of thin-film Cu derived from a high purity PVD sputter process allows for control of film quality, thickness, and as-deposited purity in contrast to extruded Cu foils. Without CC, the direct gas flow from the showerhead will impinge upon the Cu catalyst film resulting in turbulent flow (Figure 2a, open growth). This direct gas precursor bombardment not only results in a larger evaporated Cu pressure gradient but also causes the Cu losses to increase thereby decreasing the surface-bound lifetime of each absorbed carbon atom. Also, the graphene seed nucleation density is high due to direct flow from the showerhead. The result is a graphene film with relatively small graphene crystalline domains. After the addition of a quartz enclosure or CC, direct flow of gases from the showerhead is blocked and the gases must diffuse inward from the sides (Figure 2a, confined growth). H_2 has a higher diffusivity than CH_4 in a blocked growth regime and results in suppressed convection and slow transport of CH_4 to the Cu surface.[29] This further reduces the amount of available carbon precursor species relative to H_2, which results in an overall reduction in graphene seed nucleation density. During graphene growth, this effect is coupled with the confinement of evaporated Cu from the premelt layer due to the usage of a quartz enclosure. In the meantime, graphene nucleation density is controlled by optimized by adjusting the H_2:CH_4 flow ratio. This allows the graphene domains to continue growth outward, resulting in larger graphene domains.

The evaporated Cu during the growth of graphene will coat the inner walls of the reactor chamber thereby presenting an

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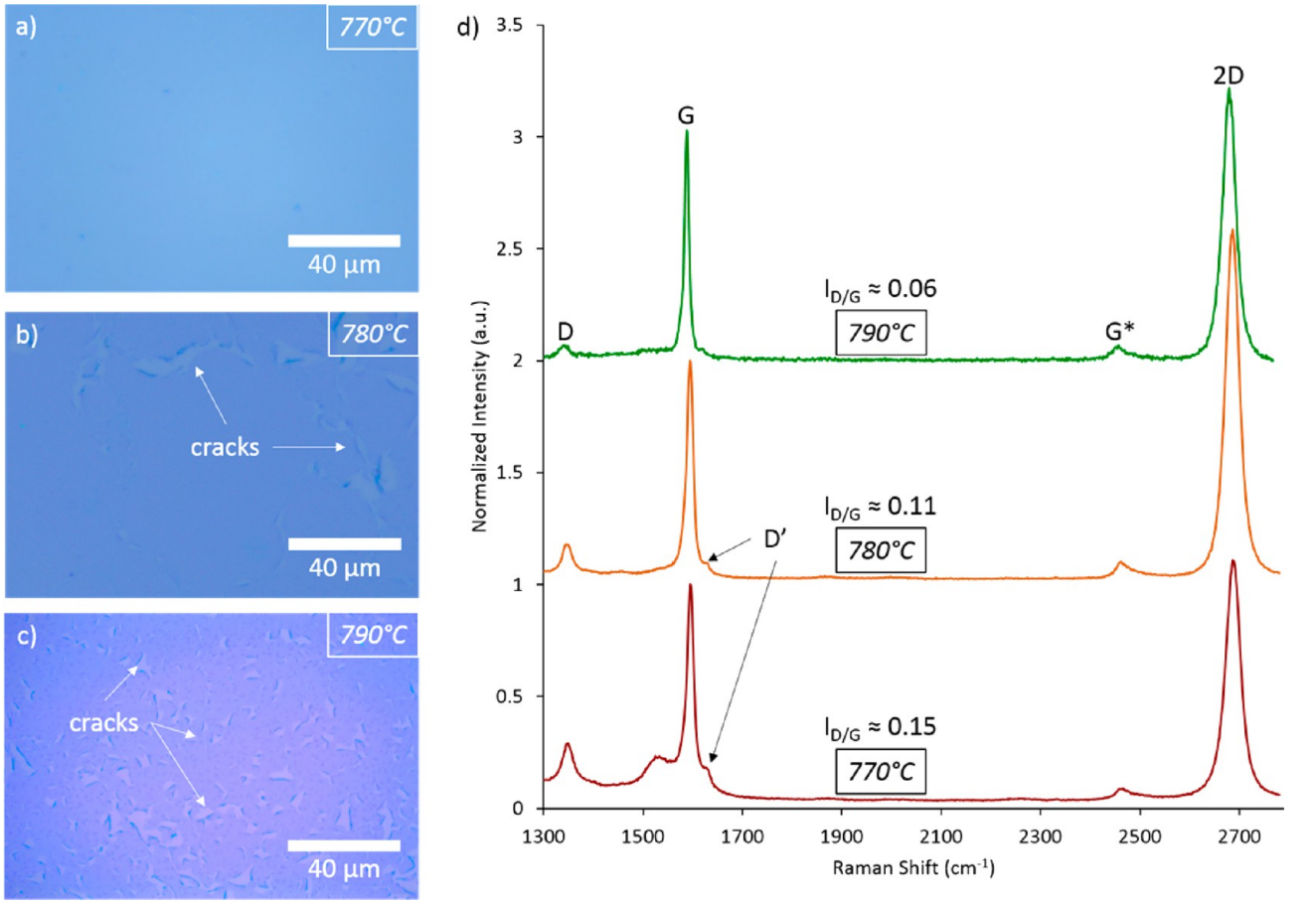

Figure 10. (a–c) Optical micrograph of graphene transferred to SiO_2/Si substrate with 300 nm thermal oxide of unseasoned quartz cap CC growths at 770, 780, and 790 °C, respectively. The as-grown graphene samples corresponding to these transfers are featured in Figure 9a,c. Note the cracks derived from the large gaps between Cu grains that are formed after transfer. (c) Raman spectra of each graphene sample transferred to SiO_2/Si wafers with 300 nm thermal oxide for 770, 780, and 790 °C using an unseasoned quartz cap or CC. The $I_{D/G}$ decreases with increasing growth temperature and Cu grain size; however, the large gaps between Cu grains cause cracks to occur post-transfer.

undesirable process. This issue is further exacerbated with the usage of SiO_2 as a Cu catalyst support due to sometimes unpredictable stability during thermal graphene growth. Therefore, C-plane sapphire and CC allows for these issues to be mitigated as Cu thin films have excellent adhesion to C-plane sapphire and the CC setup prevents coating of Cu onto the walls of the reactor chamber. CC also lessens the loss of Cu during processing allowing for lengthened growth periods while driving nucleation density lower and resulting in larger-domain graphene. We have established a baseline understanding of the growth process and the role of H_2 in this study. This work will aid in advancement of wafer-scale graphene using Cu thin films amenable for the semiconductor industry using a thermal CVD process that will, however, still require a mechanical transfer step for potential applications

CONCLUSIONS

In this study, we systematically investigated the growth conditions and identified the optimum growth parameters required for epitaxial formation of monolayer graphene on Cu(111) thin films supported on C-plane sapphire using the catalytic confinement (CC) method. Growth conditions were examined at the growth temperature of 780 °C by varying H_2:CH_4 flow ratios. For comparison, graphene was grown using CC and a SiO_2/Si support wafer instead of a C-plane sapphire support wafer. For graphene grown on Cu(111) templated by C-plane sapphire, the effect of H_2 was investigated. H_2 plays several important roles in determining the growth outcome: (1) as H_2 flow is increased, bilayer island density increases exponentially; (2) increased H_2 is associated with roughening of the Cu thin film catalyst due to increased Cu atom mobility during thermal processing, which can also lead to higher graphene nucleation seed density; and (3) a H_2:CH_4 of 69:1 produces graphene with both the lowest $I_{D/G}$ = 0.04 and the highest $I_{2D/G}$ = 2.3 within this study. GFETs were fabricated with this optimized graphene and achieved a peak mobility of 3781 cm^2 V^{-1} s^{-1} at a carrier density of 4 × 10^{12} carriers/cm^2.

In contrast to C-plane sapphire supported Cu thin-film graphene growth, optimization of graphene growth on SiO_2/Si support wafers is more difficult and results in a smaller process window of growth matrix parameters due to Cu thin film instabilities that exist in the growth regime targeting high-quality graphene ($I_{D/G}$ < 0.1). Additionally, to the best of our knowledge, no other published paper has combined quartz cap CC, vertical cold wall CVD, and Cu thin films supported by C-plane sapphire wafers in a single work. Our opinion is the combination of these three components in addition to careful optimization and transfer technique is critical for high quality graphene synthesis. In addition to the CVD graphene synthesis route, we have developed a dry transfer method that is required to effectively utilize the graphene without inducing tearing. The

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adhesion of Cu onto C-plane sapphire is higher than on SiO_2, and therefore graphene transfer is a challenge since chemical etch routes for releasing graphene will take a long time for wafer-scale growths. Using a bubbling transfer with a thermal transfer tape/PMMA support enables rapid delamination of the graphene from the Cu while leaving the Cu completely intact on the sapphire wafer. This is in contrast to SiO_2/Si wafers where the Cu and graphene stack delaminate together, requiring additional chemical etch of the Cu.

In conclusion, we have presented here a CVD growth method with CC on PVD Cu thin films supported on C-plane sapphire that enables high-quality, wafer-scale graphene.

EXPERIMENTAL METHODS

We first found the optimal H_2:CH_4 flow ratios for graphene growth with Cu/C-plane sapphire using CC and then completed a growth comparison with Cu/SiO_2/Si. Growth pressures ranged from 14.9 to 19.4 mbar, and growth temperature was held constant at 780 °C for Cu/C-plane sapphire growths while the temperature was varied for the Cu/SiO_2/Si growths due to observed Cu thin film instabilities. H_2 flow was varied from 690 to 100 sccm while holding CH_4 flow constant at 10 sccm (lowest flow setting for mass flow controller (MFC) used on reactor). For all growths, the recipe profile was held constant (Figure 1). Catalyst confinement was achieved by a custom-fabricated quartz plate with alumina alignment pins and alumina spacers for adjusting the offset from the Cu thin film during the graphene growth process. All graphene growths use a 1.0 μm dc sputtered Cu film achieved with a base pressure of $\sim 6 \times 10^{-9}$ Torr in a physical vapor deposition system.

Graphene Growth. A custom cold-wall reactor based upon the Aixtron BM Pro with capability of holding wafers up to a diameter of 50.8 mm was used for all graphene growths in this study. Supporting substrates were either SiO_2/Si wafers with 300 nm of thermal oxide (NOVA Electronic Materials) or C-plane sapphire (Precision Micro-Optics). Supporting substrates were coated with 1 μm of Cu using a Kurt J. Lesker Axxis PVD system and dc magnetron sputtering. An as-deposited Cu thin film on supporting wafer (growth wafer) was then placed directly into the growth chamber, and subsequently a quartz plate with alignment pins and alumina spacers was placed on top of the growth wafer. The growth chamber was then pumped down to base pressure ($\sim 10^{-3}$ mbar) with an automated growth recipe occurring directly afterward with growth pressures ranging from 16.7 to 20.1 mbar. During a typical growth, ultrahigh purity H_2 (assay) was injected into the growth chamber at the desired set point until a linear thermal ramp of the low-mass, carbon Joule heater had reached 780 °C, then holding at this temperature for 3 min. Next, ultrahigh purity Ar and CH_4 were injected at 650 and 10 sccm, respectively, holding at growth temperature for 9.5 min. Subsequently, all gas flows were closed and the heater was turned off and allowed to cool under vacuum. After sufficient cooling and pumping back to base pressure, the sample was further cooled under a 650 sccm flow of Ar. As-grown graphene wafers were then removed after at a heater temperature <150 °C.

Graphene Transfer. As-grown graphene wafers were first coated with two layers of poly(methyl methacrylate) (PMMA) solution (6% 995 kDa PMMA in anisole) by spin coating. The PMMA was then cured on purpose-built hot plates at 135 °C for 3 min. Next, thermal release tape was applied by hand with a thermal release transition at 150 °C (Nitto REVALPHA). The thermal tape/PMMA/graphene stack was then separated by H_2 bubbling transfer similar to work by others.[24] This stack was rinsed and dried then placed onto the target wafer and placed between two ground aluminum plates compressed with a linear screw clamp. The clamp assembly was then placed into a vacuum oven pumped to base pressure ($\sim 10^{-2}$ mbar) and heated to 140 °C for 1 h. Afterward, the thermal tape/PMMA/graphene stack was bonded well to the target wafer. The wafer was then moved onto a preheated purpose-built hot plate and linearly ramped to 165 °C. Once the hot plate reached the thermal release tape temperature, the tape was removed and the wafer was allowed to reach 165 °C, then removed, and allowed to cool to room temperature (RT). The remaining PMMA was removed with a RT bath of acetone for 3 h.

Sample Characterization. As-grown graphene films on Cu and transferred graphene films were analyzed for quality and relative doping levels with a bright-field optical microscope and a Horiba HR800 Raman spectrometer equipped with a mapping stage. As-grown graphene films and the Cu film crystallographic orientation were analyzed with a Zeiss Sigma VP scanning electron equipped with an Oxford Nordlys electron backscatter diffraction (EBSD) detector. EBSD mapping was performed at 20 kV while graphene SEM imaging was performed at 5 kV.

Graphene Field Effect Transistor Fabrication and Measurement. GFETS channels and source/drain contacts were defined using a Nanometer Pattern Generation System (NPGS) electron beam lithography (EBL) system installed onto a Zeiss Sigma VP SEM. Prior to patterning of graphene channels, the as-grown graphene was transferred onto degenerately doped Si wafers (which served as a global backgate) with 300 nm of thermal oxide. Metallization was achieved with a Kurt J. Lesker Axxis PVD system equipped with electron beam evaporation. Electrodes were fabricated with a serial deposition of 2.5 Å Ti, 20 nm Pd, and a 15 nm Au cap. Upon final lift-off, patterned devices wafers were placed into a Lakeshore vacuum probe station for measurement.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acs.jpcc.6b06459.

EBSD hemispherical pole figures of graphene on Cu for varying H_2:CH_4 flow ratios (Figure S1) and large-area IPF:Z EBSD maps for two H_2:CH_4 flow ratios, 20:1 and 30:1 (Figure S2) (PDF)

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Notes

The authors declare no competing financial interest.

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■ ABBREVIATIONS

CVD, chemical vapor deposition; RTA, rapid thermal annealing; PVD, physical vapor deposition; STM, scanning tunneling microscope; CC, catalyst confinement; EBSD, electron backscatter diffraction; IPF, inverse pole figure; fwhm, full width half-maximum; GFET, graphene field effect transistor; SEM, scanning electron microscope; NPGS, nanometer pattern generation system; PMMA, poly(methyl methacrylate); EBL, electron beam lithography.

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