31 28	827	7									16	15	87					<b>Instruction type</b>
Cond		0	Q	Ι	C	)po	CC	de	9	S	Rn	Rd		0pe:	ra	nd2		Data processing / PSR Transfer
Cond		0	0	0	0	) (	0	0	Α	S	Rd	Rn	Rs	1 (	)	0 1	Rm	Multiply
Cond		0	0	0	0	) [	1	U	A	S	RdHi	RdLo	Rs	1 (	)	0 1	Rm	Long Multiply (v3M / v4 only)
Cond		0	0	0	1	(	0	В	0	0	Rn	Rd	0 0 0 0	1 (	)	0 1	Rm	Swap
Cond		0	0 1 I P U B W L Rn Rd									Rd		Offset				Load/Store Byte/Word
Cond		1	0	0	F	Ţ	U	s	W	L	Rn		Regist	er 1	i	Load/Store Multiple		
Cond	T	0	0	C	F	ī	U	1	W	L	Rn	Rd	Offset1	1 5	3	н 1	Offset2	Halfword transfer : Immediate offset (v4 only)
Cond	0	0	) (	0	Р	ī	IJ	0	W	L	Rn	Rd	0 0 0 0	1 8	3	Н 1	Rm	Halfword transfer: Register offset (v4 only)
Cond	Ť	1	0	1	I							Offs	Branch					
Cond	7	0 (	0	0	1	T	0	0	1	0	1 1 1 1	1 1 1 1	1 1 1 1	0	0	0 1	Rn	Branch Exchange (v4T only)
Cond	Ť	1	<u> </u>	C	E	1	U	N	W	L	Rn	CRd	CPNum			Off	set	Coprocessor data transfer
Cond	Ť	1	1	1	. (			Oj	<b>—</b> p1		CRn	CRd	CPNum	Oj	2	0	CRm	Coprocessor data operation
Cond	Ť	1	1	1	. (		C	p:	1	L	CRn	Rd	CPNum	Oj	2	1	CRm	Coprocessor register transfer
Cond	T	1	1	1	. 1	SWI Number											Software interrupt	