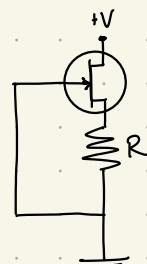


Physics IIIA Lab 4

Pre-Lab Questions

- 1) The maximum allowed gate current is 50mA. Exceeding it will burn out the gate.
- 2) As the voltage across the resistor increases, the gate will become negatively biased relative to its source, decreasing the current through it. This in turn will decrease the voltage across the resistor until the gate becomes positively biased relative to its source. This will in turn increase current through the gate, and repeat the feedback loop till a stable equilibrium is reached.
- 3) Load line analysis can be used by finding when the current through the resistor equals the current from the gate, and this would be the equilibrium current.
- 4) As R_s increases, the voltage into the gate will decrease. This results g_m to decrease as well since V_{in} and g_m have a direct relationship. This decreases performance since a lower g_m results in a slower response time from the gate.

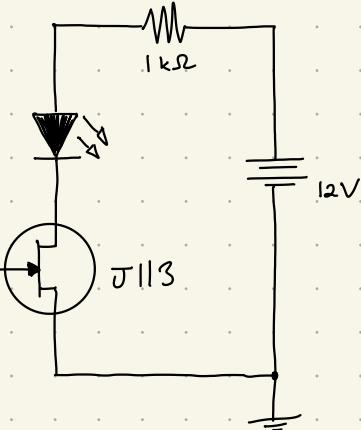
Lab Exercises:

Problem R4.1:

Pins	DMM Measurement
G S	0.762
G D	0.759
S D	0.05

The measurement started larger and then decreased.

Problem R4.2:



the LED still turns on and off when switching between ground and -12V through a resistor.

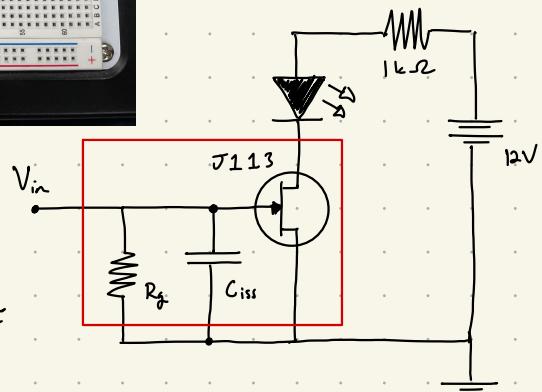


Problem R4.3

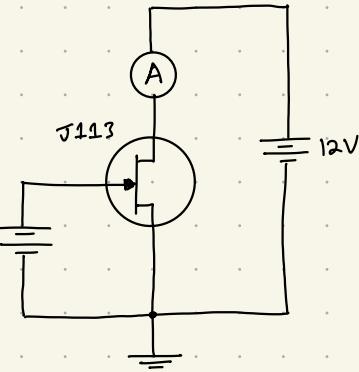
$$C_{ext} = 330 \text{ pF}, t = 32 \text{ s} \\ = 4.7 \text{ nF}, t = 35 \text{ s}$$

$$a) R_g C_{ext} = t \Rightarrow R_g = \frac{t}{C_{ext}} = \frac{35 \text{ s}}{4.7 \times 10^{-9} \text{ F}} = 7.45 \times 10^6 \Omega = 7.45 \text{ G}\Omega$$

$$b) t = R_g C_{iss} < 0.15 \text{ s} \Rightarrow C_{iss} < \frac{0.15 \text{ s}}{7.45 \text{ G}\Omega} = 0.0201 \times 10^{-9} \text{ F} = 20.1 \text{ pF}$$



Problem R4.4



a) Var VS (v) | I_D (mA)

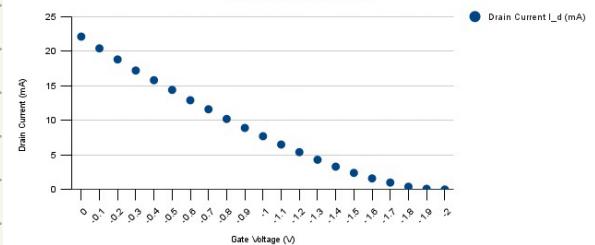
0	22.1
-0.1	20.4
-0.2	18.8
-0.3	17.2
-0.4	15.8
-0.5	14.4
-0.6	12.9
-0.7	11.6
-0.8	10.2
-0.9	8.9
-1.0	7.7
-1.1	6.5
-1.2	5.4
-1.3	4.3
-1.4	3.3
-1.5	2.4
-1.6	1.6
-1.7	1.0
-1.8	0.5
-1.9	0.1
-2.0	0

$$b) I_D = I_{DSS} [1 - (V_{GS}/V_P)]^2$$

$$I_D = 22.1 [1 - (-\frac{V_{GS}}{2})]^2$$

$$I_D = 22.1 [1 + \frac{1}{2} V_{GS}]^2$$

Gate Transfer Characteristic

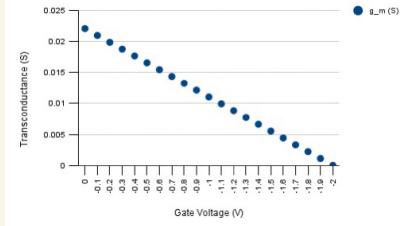


$$c) I_D = 0.022 [1 + \frac{1}{2} V_{GS}]^2$$

$$\frac{dI_D}{dV_{GS}} = 0.0442 [1 + \frac{1}{2} V_{GS}] (\frac{1}{2}) = g_m$$

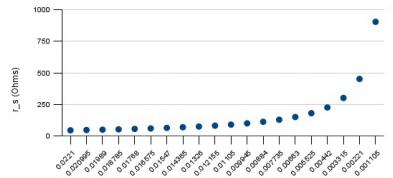
$$g_m = 0.022 [1 + \frac{1}{2} V_{GS}]$$

Gate Voltage vs. Transconductance

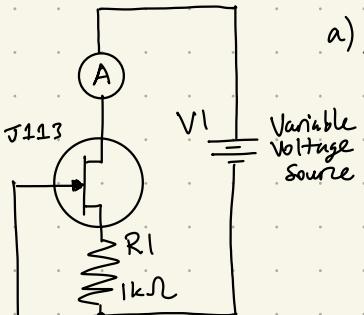


$$d) r_s = \frac{1}{g_m}$$

Transconductance vs. Source Resistance



Problem R4.5



a) Current Source Voltage (v) | Current Source Current (mA)

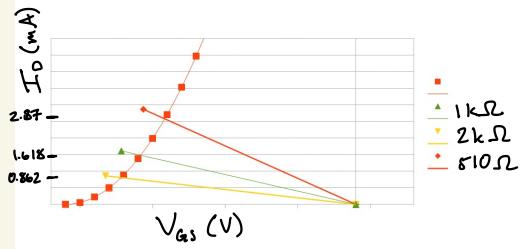
0	0
0.2	0.166
0.4	0.332
0.6	0.495
0.8	0.656
1	0.814
1.2	0.846
1.4	1.156
1.6	1.290
1.8	1.398
2	1.467
2.5	1.530
3	1.552
4	1.573
5	1.585
7.5	1.600
10	1.610
12	1.615
17	1.627
24	1.637

$$b) V_1 = +12V, I = 1.616 \text{ mA}$$

when warmed, $I = 1.618 \text{ mA}$

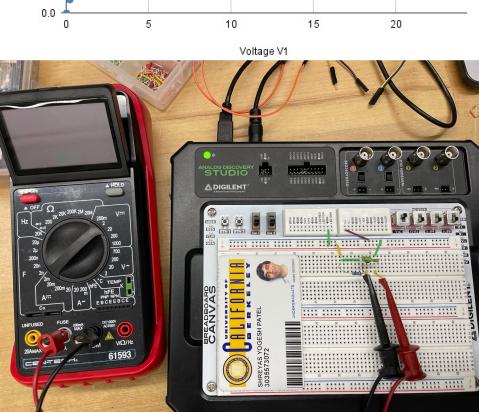
$$c) R_s = 510 \Omega, I = 2.87 \text{ mA}$$

$$R_s = 2 k\Omega, I = 0.862 \text{ mA}$$

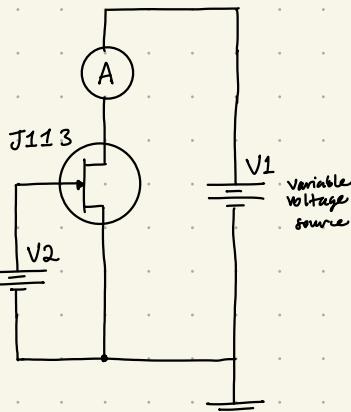


d) JFET | I_D (mA)

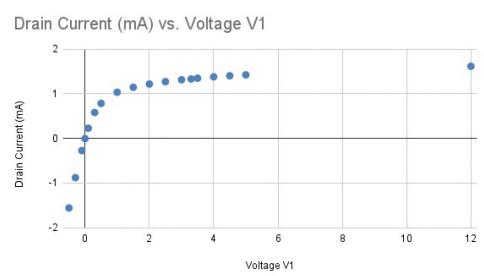
1	1.512
2	1.683
3	1.528



Problem R4.6

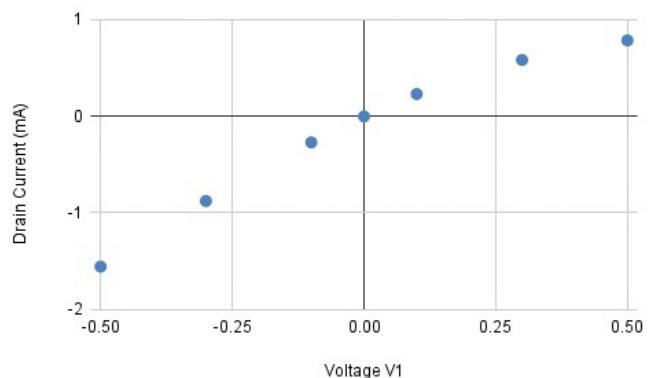


a&b)

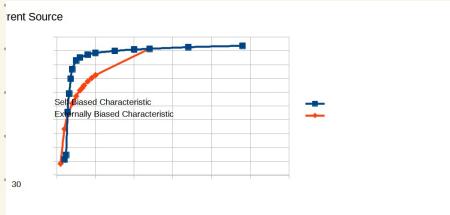


c)

Drain Current (mA) vs. Voltage V_1



Problem R4.7



$$R_{\text{eff}} = \frac{\Delta V}{\Delta I} = \frac{12}{0.022} = 545.5 \text{ k}\Omega$$

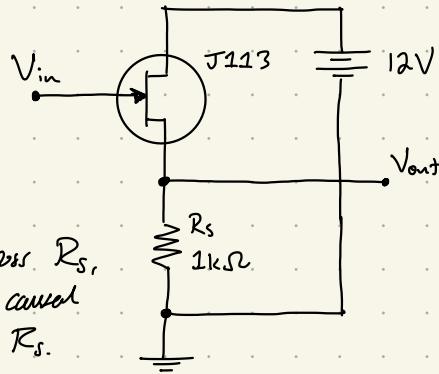
Problem R4.8

a) Sine: 100 mV, 1 kHz, 0V offset

$$V_{in} = 70.76 \text{ mV} \Rightarrow G = \frac{V_{out}}{V_{in}} = 0.87$$

$$V_{out} = 61.83 \text{ mV}$$

V_{out} and ground can be seen as a voltage divider across R_s , with V_{out} being the voltage across R_s . The offset is caused by the constant voltage drop from the 12V across R_s .



b) Max amplitude is $V \approx 2V$

c) $V_R = 1.608 \text{ V}$

$$I_D = \frac{1.608 \text{ V}}{1 \text{ k}\Omega} = 1.608 \text{ mA}$$

$$r_s = 226.4 \Omega$$

$$d) V_{out} = \frac{R_s}{R_s + r_s} V_{in} \Rightarrow \frac{V_{out}}{V_{in}} = G = \frac{R_s}{R_s + r_s} = \frac{1 \text{ k}\Omega}{1 \text{ k}\Omega + 226.4 \Omega} = 0.815$$

The expected gain is close to what was measured, with a % diff of 6.3 %

Problem R4.9

JFET	V_{ds}
1	1.509
2	1.682
3	1.526
4	1.704
5	1.340
6	1.648
7	1.570
8	1.635
9	1.684
10	1.512
11	1.467
12	1.621
13	1.705
14	1.426

JFET 2 & 9 are closest

Redoing R4.8 with 2

$$a) V_{in} = 71 \text{ mV} \Rightarrow G = 0.88$$

$$V_{out} = 62.5 \text{ mV}$$

b) max amplitude is $V=2.1 \text{ V}$

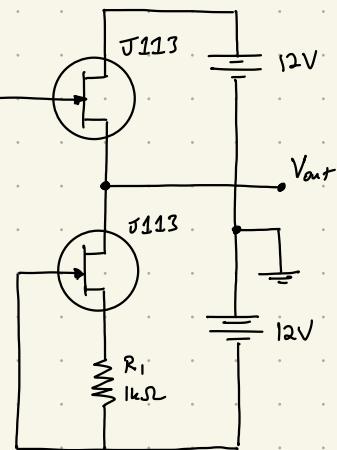
$$c) V_R = 1.682 \text{ V} \Rightarrow I_D = \frac{1.682 \text{ V}}{1 \text{ k}\Omega} = 1.682 \text{ mA}$$

$$r_s = 164 \Omega$$

$$d) G = \frac{R_s}{R_s + r_s} = \frac{1 \text{ k}\Omega}{1 \text{ k}\Omega + 164 \Omega} = 0.859$$

The expected gain is close with a % diff of 2.4 %

Problem R4.10



100 mV Sine, $f = 1\text{kHz}$, Offset = 0V:

$$V_{in} = 70.8 \text{ mV}$$

$$V_{out} = 71.3 \text{ mV} \Rightarrow G = 1.008$$

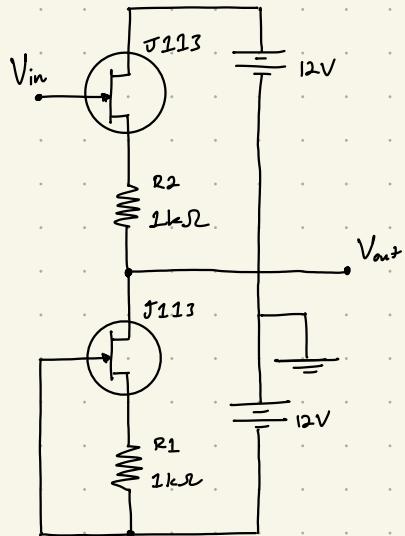
$$G = \frac{R_{eff}}{R_{eff} + r_s} = \frac{540\text{k}\Omega}{540\text{k}\Omega + 165\Omega} = 0.999697$$

The measured and expected gain are very close with % diff of 0.8%

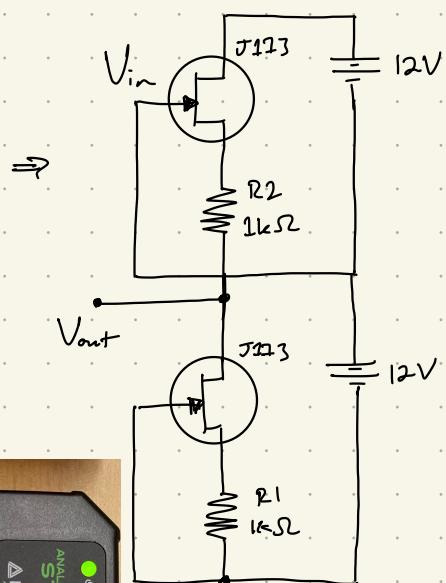
There is still an offset of around 1.8 V

The range of allowable input signal has also increased to atleast 5V.

Problem R4.11



$G = 0.997$ but offset is nearly zero



If V_{in} is a grounded circuit, then the V_{out} is measured at a point of symmetry between the two circuits, so $V_{out} = V_{in}$. This ends up eliminating any offset.

This can also be thought of as the bottom circuit and JFET act as a current source for the top circuit, supplying an equilibrium current I_S . With the addition of the resistor to the top circuit, the resistor and JFET closely copy the bottom circuit's characteristics and therefore also its equilibrium current.

