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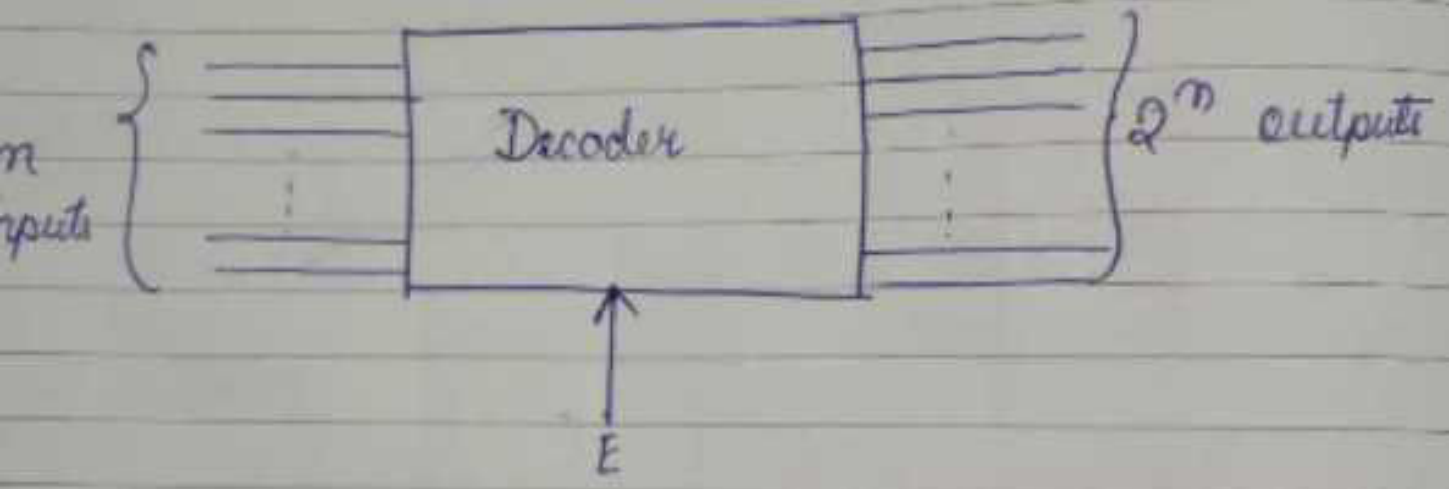
DECODERS

* Decoder is a multi-input, multi-output logic circuit which decodes 'n' inputs into 2^n possible outputs.



where E = Enable
- E=0, decoder is disabled. (OFF)
- E=1, decoder is enabled. (ON)

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Eg: If 2 inputs are provided we will get 2^n o/p

2 to 4 Decoder Design :-

2 i/p , 4 o/p

$n=3 \rightarrow n=2 \rightarrow n=1 \rightarrow n=0$

$2^3 \quad 2^2 \quad 2^1 \quad 2^0$

E	A	B		Y_3	Y_2	Y_1	Y_0
0	X	X		0	0	0	0
1	0	0	$n=0$	0	0	0	1
1	0	1	$n=1$	0	0	1	0
1	1	0	$n=2$	0	1	0	0
1	1	1	$n=3$	1	0	0	0

If E=0, without knowing i/p, o/ps are '0'.

when $n=0$, 2^0 is enabled
When $n=1$, 2^1 place enabled
so - on.

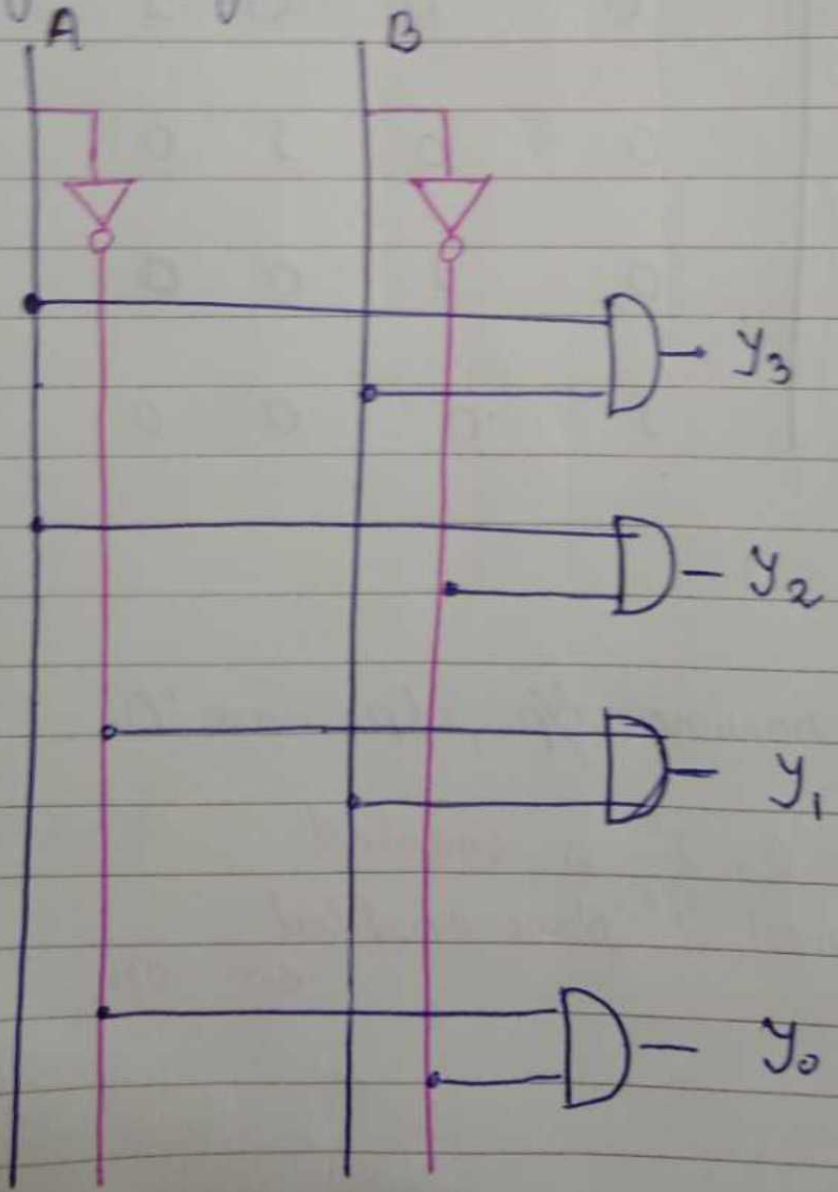
$Y_3 = A.B$

$Y_2 = A.\bar{B}$ (see the table)

$Y_1 = \bar{A}.B$

$Y_0 = \bar{A}.\bar{B}$

Logic Diagram:-

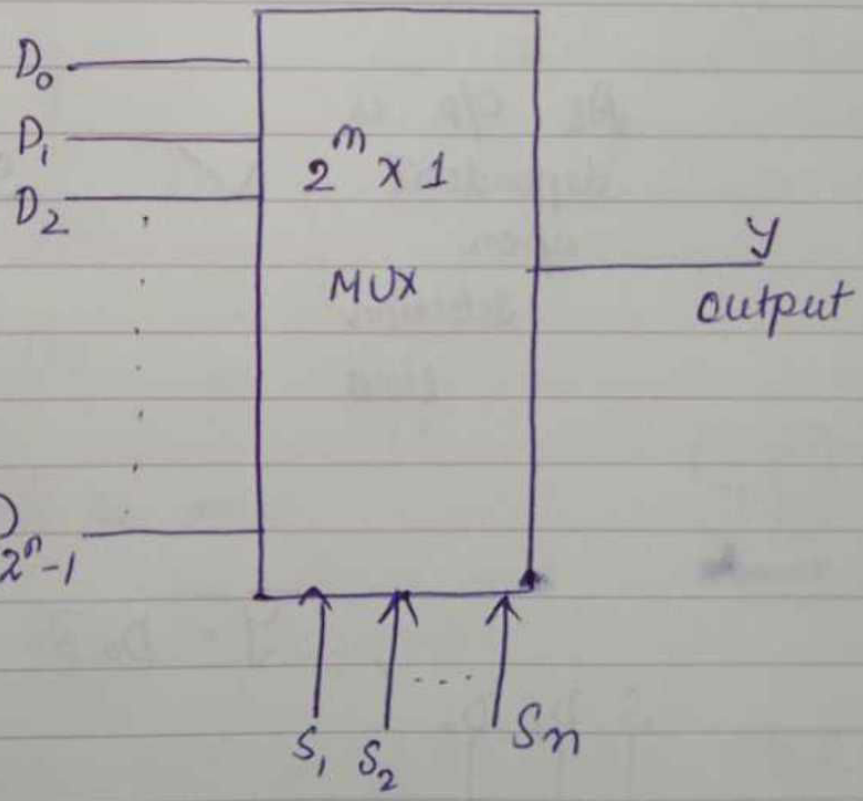


3 to 8 Decoder (Self Study)

$n=3$, $2^3 = 8$ o/ps.

MULTIPLEXER (MUX)

↳ Multiplexer is a combinational logic circuit used to select only one o/p (output) among several inputs based on selection lines.



↳ This can act as digital switch.

↳ This is also called as data selector.

↳ For a MUX, there can be 2^n i/ps, 'n' selection lines and only one o/p.

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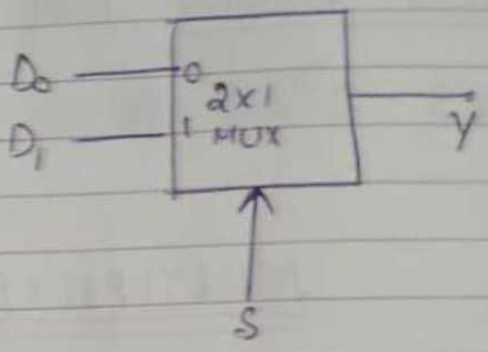
2 x 1 MUX Design :-



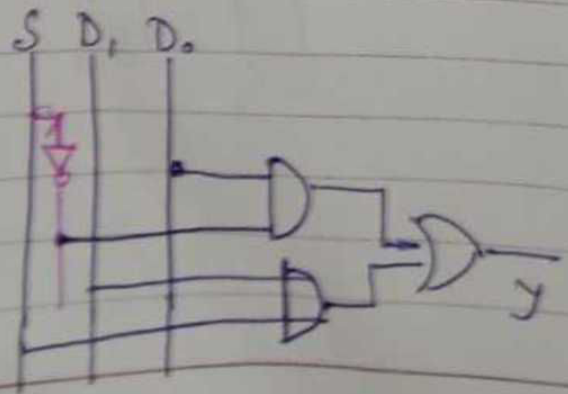
JJ

D_0	D_1	S	Y
X			

As O/p is dependent upon selection lines ✓

S	Y
0	D_0
1	D_1

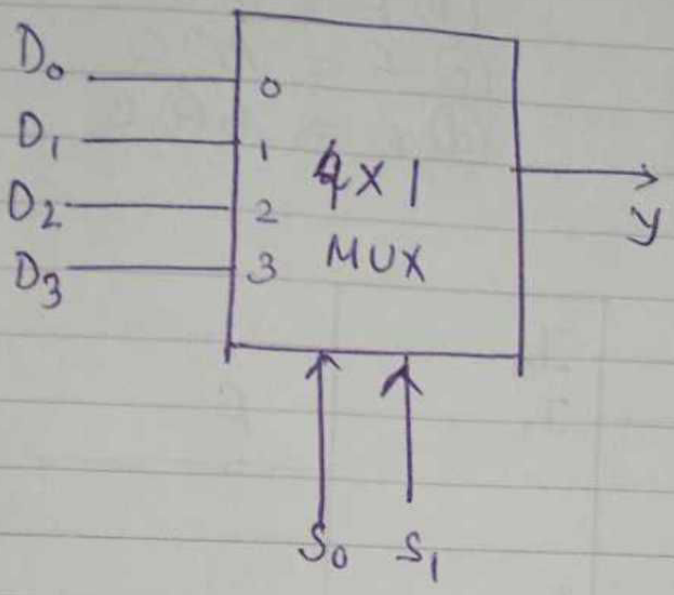
$$Y = D_0 \bar{S} + D_1 S$$



4×1 MUX :—

$2^n = 4$

$\therefore n = 2$



S_0	S_1	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

$$Y = D_0 \bar{S_0} \bar{S_1} + D_1 \bar{S_0} S_1 + D_2 S_0 \bar{S_1} + D_3 S_0 S_1$$

Logic Diagram → ?

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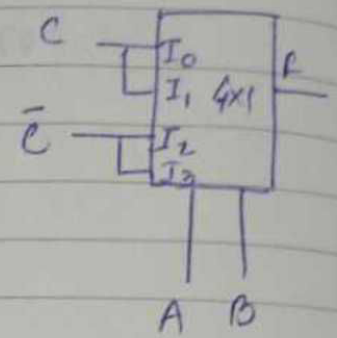
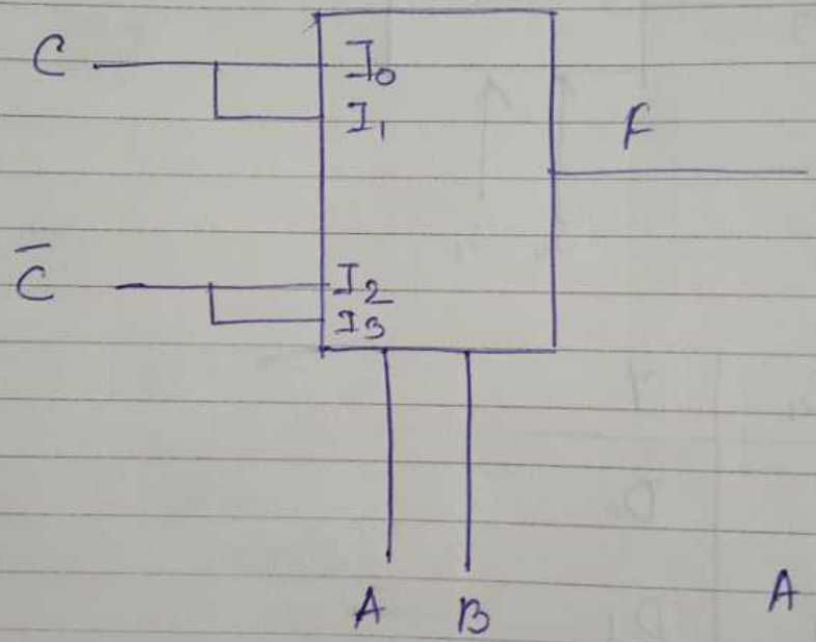
Q1 The logic realized by the circuit shown in the figure is —

(a) $F = A \odot C$
(b) $F = A \oplus C$
(c) $F = B \odot C$
(d) $F = B \oplus C$





A	B	F
0	0	C
0	1	C
1	0	$\bar{C}$
1	1	$\bar{C}$

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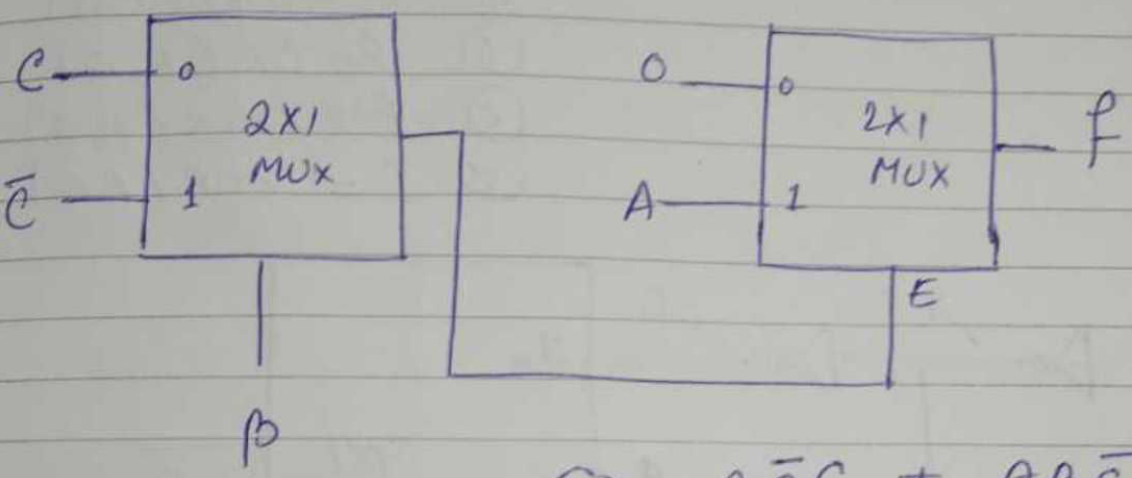
$F = C\bar{A}\bar{B} + C\bar{A}B + \bar{C}A\bar{B} + \bar{C}AB$

$= C\bar{A} + \bar{C}A$

$= A \oplus B$

Q2. The Boolean 'f' implemented in the figure using Two input multiplexers is



(a) $A\bar{B}C + AB\bar{C}$

(b) $ABC + A\bar{B}\bar{C}$

(c) $\bar{A}BC + \bar{A}\bar{B}\bar{C}$

(d) $\bar{A}\bar{B}C + \bar{A}B\bar{C}$

1st MUX

B	E
0	C
1	$\bar{C}$

$E = C\bar{B} + \bar{C}B$

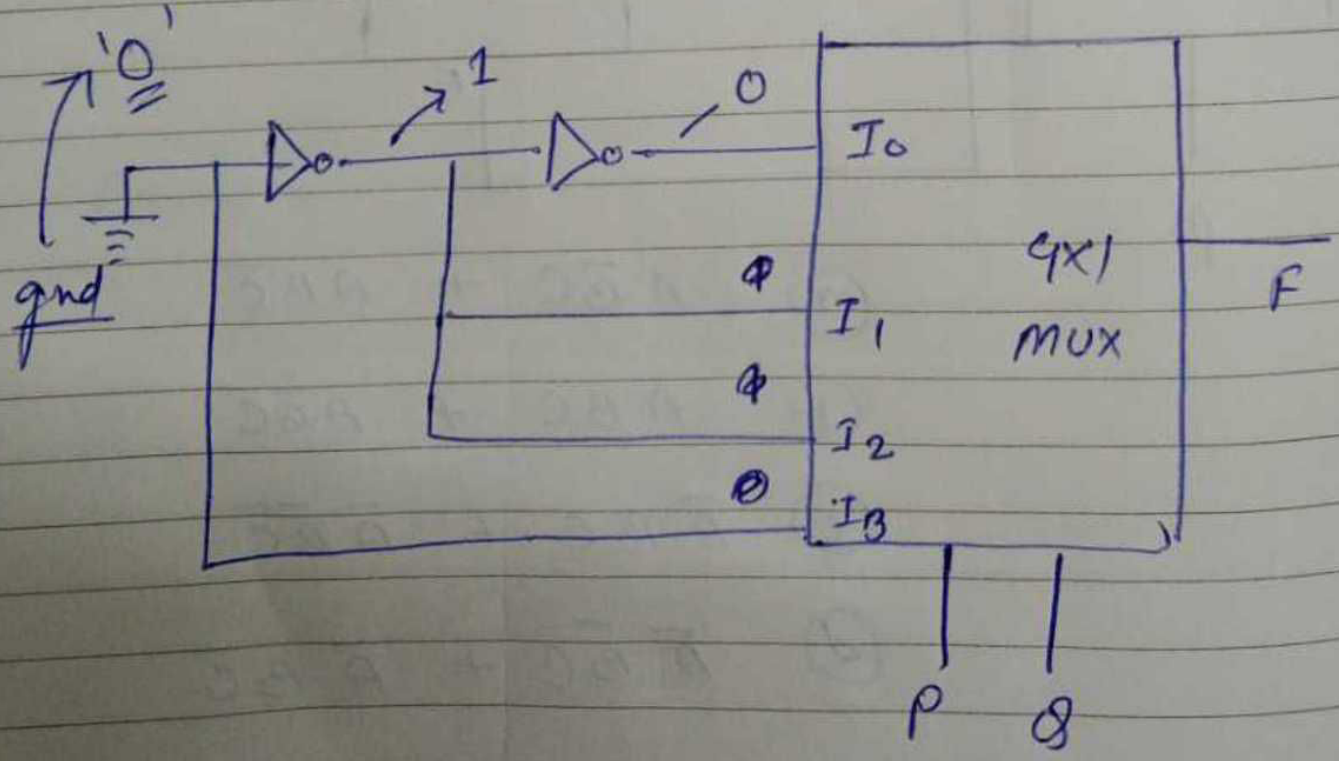
2nd MUX

E	f
0	0
1	A

$f = AE$
$= A(C\bar{B} + \bar{C}B)$
$= A\bar{B}C + AB\bar{C}$

Q3. The logic function implemented by the circuit below is —

(a) F = AND (P, Q)
(b) F = OR (P, Q)
(c) F = XNOR (P, Q)
(d) F = XOR (P, Q)



DEMULTIPLEXERS (DEMUX)

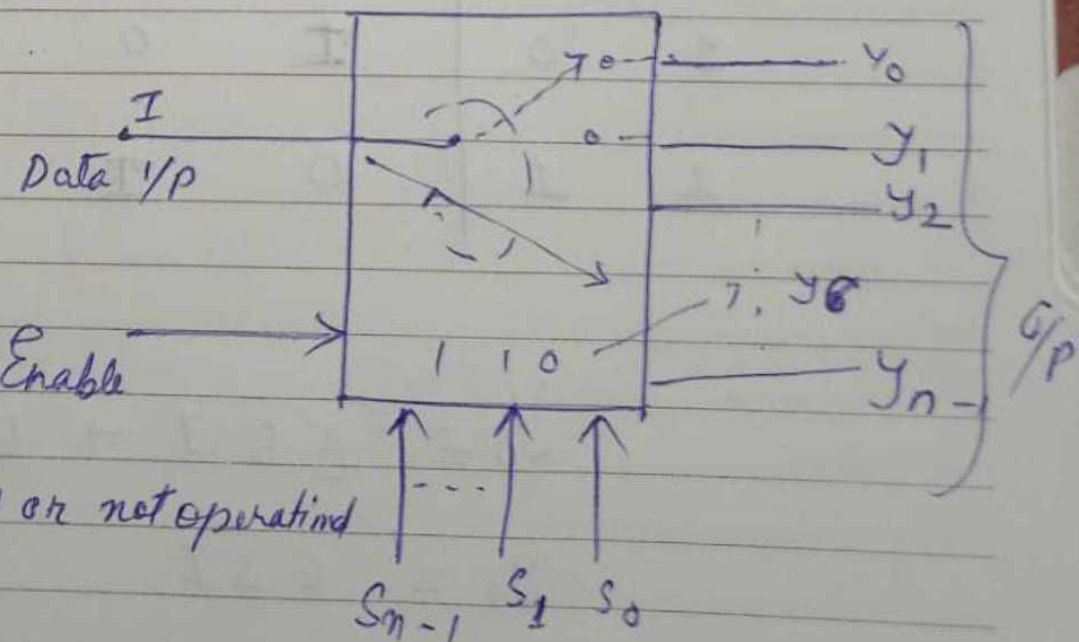
↳ one i/p and many o/ps.

↳ Reverse operation of MUX.

↳ Also called as Data Distributor.

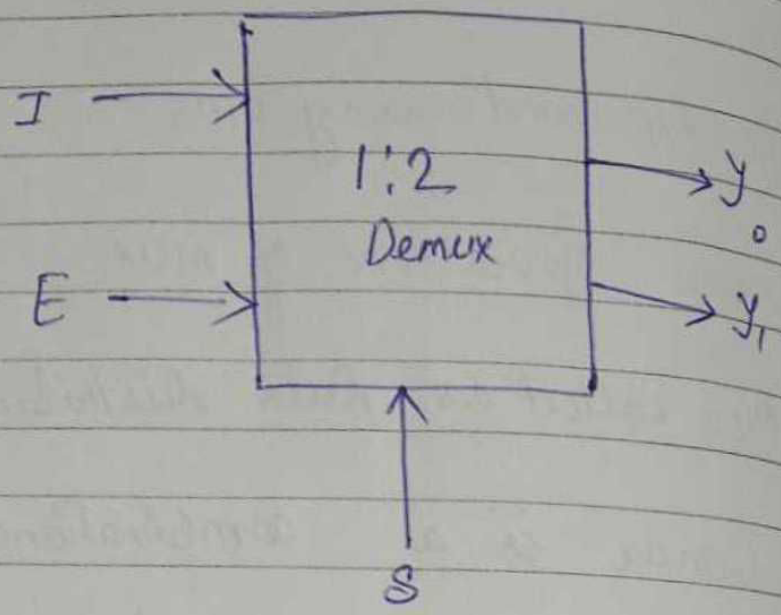
↳ Demux is a combinational ckt.

MUX	Demux
2:1 / 2x1	1:2 / 2x1
8:1 / 8x1	1:8
4:1	1:4



Select line 110 (6) the data i/p will go to Y6.

1 : 2 Demux



E	S	y_0	y_1
0	0	0	0
0	1	0	0
1	0	I	0
1	1	0	I

$$y_0 = E\bar{S}.I + ES.0$$

$$y_0 = E\bar{S}I$$

$$y_1 = ESI$$

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logic Diagram