

Consider page size = frame size = 4 bytes

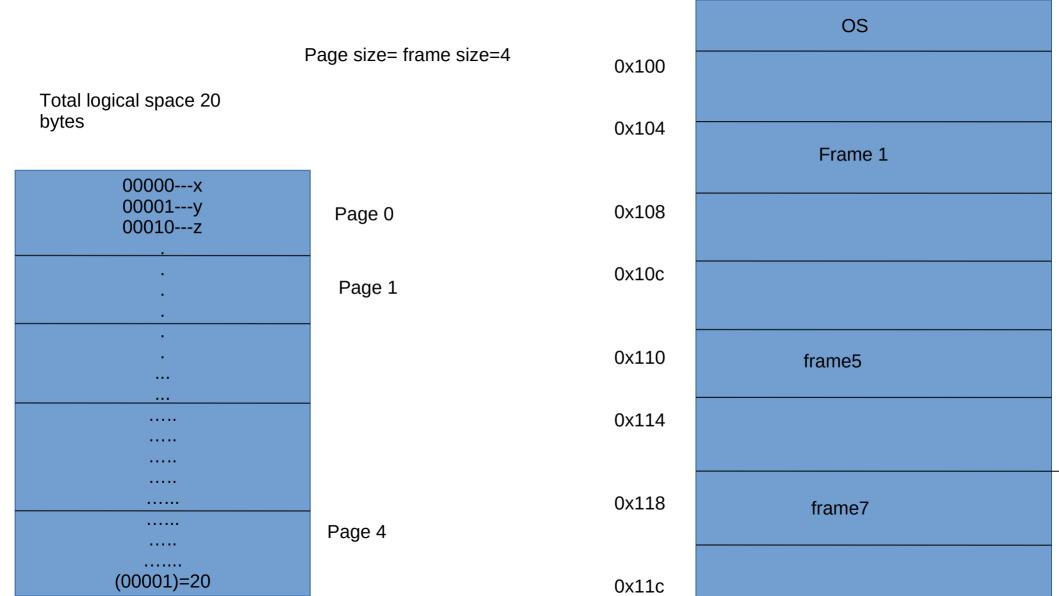
Suppose the logical address space for a process is 20 bytes.

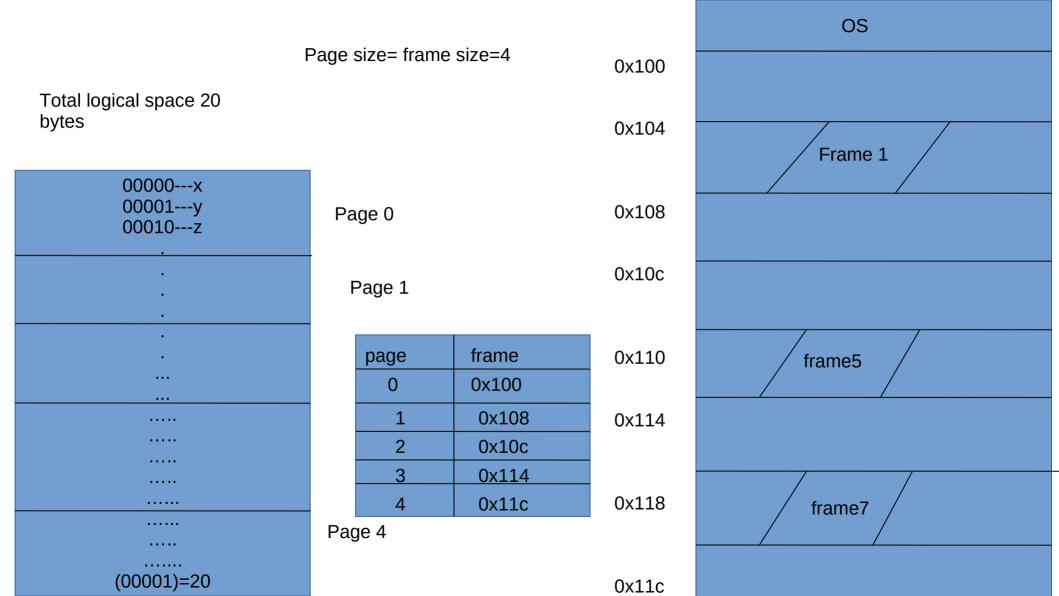
How many pages are there in this process?

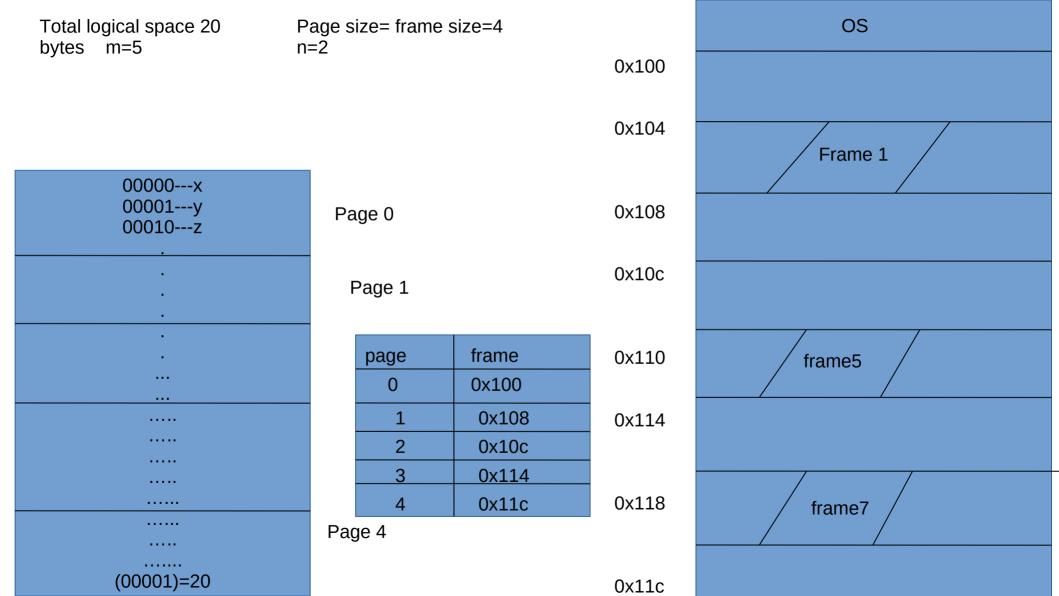
Draw the page table for this process.....

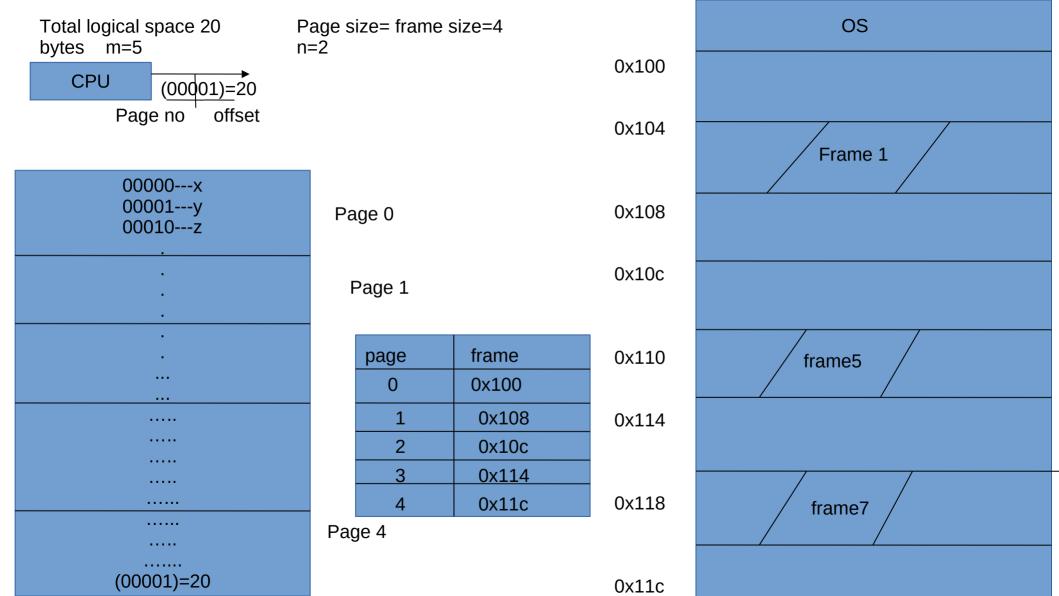
Solution? Multi level paging

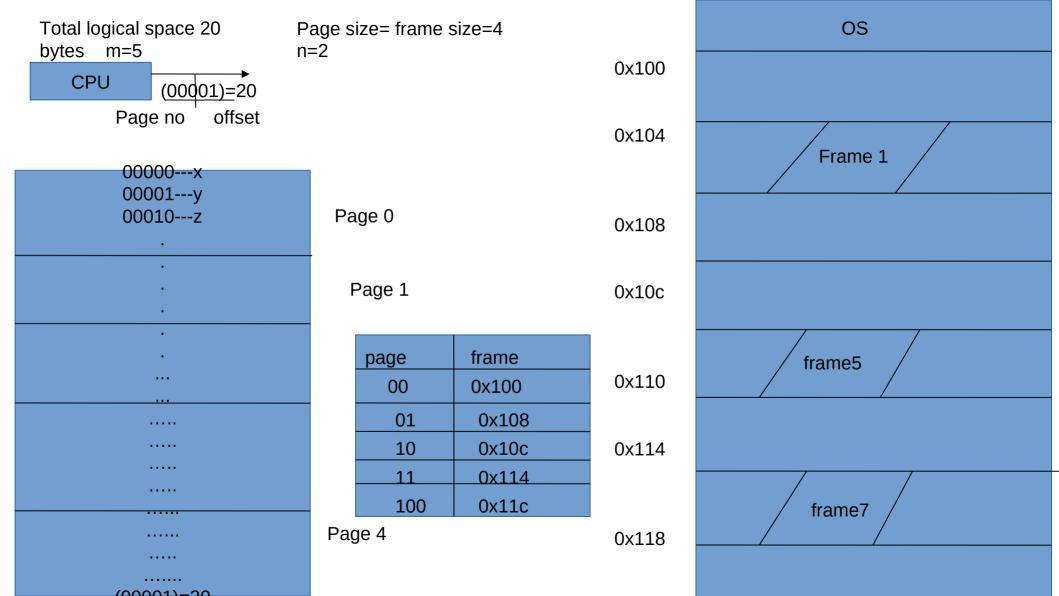
One way of getting around this problem is to use a two level paging scheme in which the page table itself is also paged.

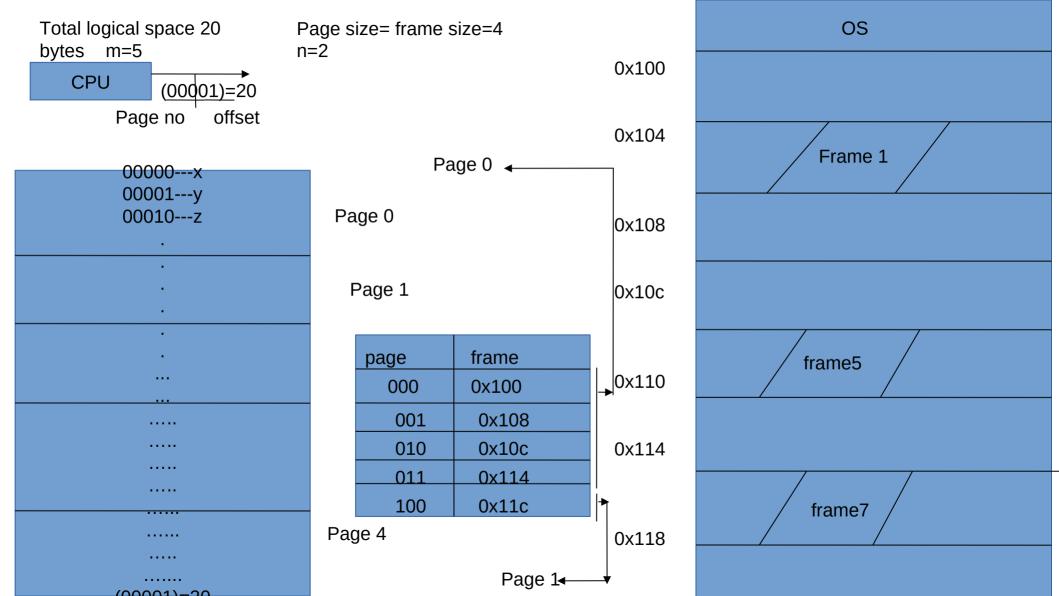


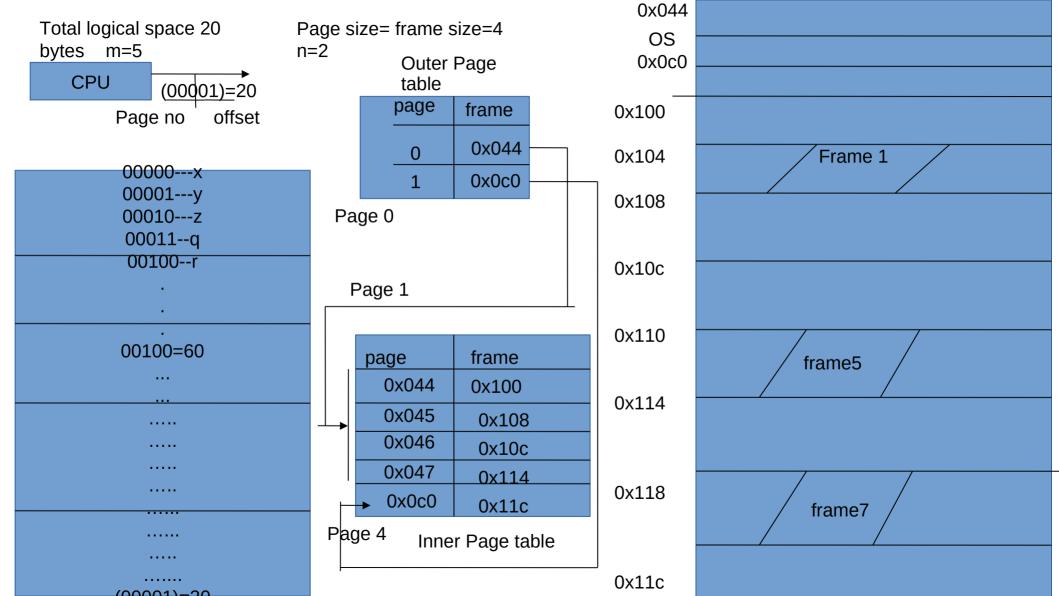












Disadvantage?

Page table for each process consume lots of memory......

Inverted page table

To overcome the disadvantages mention in the previous slides an inverted page table is used.

Inverted page table has one entry for each frame of memory.

Each entry consists of the logical(or virtual) address of the page stored in that memory location. With information about the process that owns it.

Therefore there is only one inverted page table in the system and it has only one entry for each frame of physical memory.

Each logical address in the system is consist of a triplet.

< process id, page number, offset>

each inverted page table entry is a paircess id,page number>.

When a memory reference occurs part of the logical address consisting of process id,page number> is presented to memory subsystem .

The inverted page table is then searched for this process id,page number>.

If the match is found say at entry I then the physical address <i, offset> is generated.

If no match is found an illegal address access has been attempted .

