Flare Reduction in EUV Lithography by Perturbation of Wire Segments

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***Abstract*—With growing demand for complex and high density integrated chips (IC), optical lithography with 193 nm immersion technology has become a bottleneck in the chip manufacturing industry. IC fabrication industry is looking forward to next generation lithography methods, for example, Extreme Ultraviolet Lithography (EUVL). While EUVL is capable of printing with a wavelength of 13.5 nm, it suffers from a major drawback called flare, due to the scattering of light on blank surfaces. Large flare and/or its large variation cause critical dimension (CD) violations. In this paper, we propose an Integer Linear Programming based method to mitigate the effects of flare in the post routing step through perturbation of wire segments. Experimental results on a set of synthetic circuits show significant reduction of flare and its standard deviation across the chip surface.**

I. Introduction

Advancement of technology has scaled down the process geometry to the nanometer range. Nowadays IC foundries have to use an optical lithography system with a larger wavelength of light to print the layout features (patterns) having much smaller dimensions on the wafer. This is referred as the sub-wavelength lithography gap [1] but it leads to huge CD distortion for printed metal features. One of the popular ways of printing at sub 20nm process technology nodes using 193i lithography system is referred as multiple patterning [9] which requires decomposition of the layout into multiple layout with larger values of the minimum spacing in order to make it compatible with the larger wavelength. It can be observed from the various works [9] [10] on multiple patterning that it needs multiple masks for printing a single layout thereby leading to increased mask cost. Multiple patterning also has the problem of CD distortion. EUVL, a next generation technique using light beam having wavelength of 13.5nm, is thus convenient to print modern technology nodes with smaller feature sizes. However 13.5nm wavelength of light is not transmitted but absorbed by most of the materials which is the main disadvantage of EUVL system. To solve this problem, reflective optical components and clear-field masks are used to print patterns. The layout patterns are formed by the absorbers on the clear-field mask, while reflective materials remain in the vacant regions. Incident light gets absorbed by the absorbers and the patterns get printed, whereas light reflects from the vacant regions.

Although reflective materials in the clear-field mask can prevent the light from getting absorbed, undesirable scattered light reflected due to surface roughness, reduces the contrast between bright (vacant regions) and the dark (layout pattern) regions on exposure to EUV light. Such undesired scattered light reflected from the vacant regions on the surface is called *flare* in EUVL. Figure 1 shows the clear-field mask and the scattering of light on the uneven surface of the photo reflective substance. The reduction of contrast between patterns and vacant regions causes high flare and CD distortion. Since flare is proportional to the surface roughness of the optical system and inversely proportional to square of the wavelength, EUVL suffers from rather high levels of flare compared to traditional lithography technologies [3]. Flare is the most prominent challenge for EUVL.

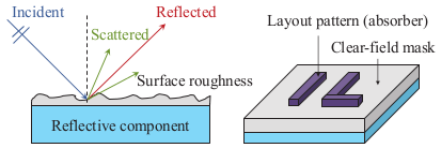

Fig. 1. Light scatters from the photo reflective coating on the mask and patterns are printed using the light absorbers (Courtesy [3])

There are few strategies to compensate the effect of flare in the literature, such as optical proximity correction (OPC) and dummy fills for CMP. It was observed that one percent of change in flare may cause a change of 10 nm in CD at the 22 nm technology node and may be considerably larger for more advanced technology nodes [4]. The non-uniformity of CD caused by large flare may not be fully compensated by global CD resizing techniques [3]. Instead, previous works [3] [5] on flare reduction have used dummification for reducing flare and its variation. Layout regions with less *pattern density* contribute more to the generation of flare than the regions with higher pattern density. Thus, vacant regions of the layout are filled with dummy (non-functional) metal features to increase the pattern density there, and reduce the flare. However dummification requires a large number of dummy features to be added to the layout which increases the mask cost. Moreover, large amount of dummy features may increase the coupling capacitance [6] between metals which can affect the circuit speed. Additional constraints are required to bound the coupling capacitance of metals (wire segments) within a threshold. In this paper, we propose the first work on minimization of flare at the post-routing stage without dummification as well as any performance degradation.

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It was shown in [4] that uniform pattern density does not induce uniform flare distribution. Typically, the flare in the central region of the chip is much higher than that in the peripheral regions. This phenomenon is referred as the *flare periphery effect* [3]. It is reported that conforming the *pattern density map* to the *flare map* minimizes the maximum as well as the average value of flare. In this work we propose a wire perturbation based strategy to minimize the peak flare, the mean flare and its standard deviation implying better control on CD uniformity without sacrificing the delay significantly. Previous works [13] [14] have used wire perturbation for conflict and stitch-awareness in Double Patterning Lithography. Wire perturbation provides only local changes in layout. Even though flare is a global phenomenon but can be reduced by judicial modification in the post layout stage. Wire perturbation can be an acceptable approach for layout modification.

In the rest of this paper, Section II details out how to compute flare, Section III describes our flare minimization problem and Section IV describes our proposed method. Experimental results appear in Section V and finally Section VI presents the concluding remarks.

II. Preliminaries

This section describes the existing model[11] [12] of flare computation in EUVL.

Computation of Flare: Flare in EUVL system is traditionally modeled as a *Point Spread Function* (PSF). The flare map is obtained by convolving the PSF with the original image intensity I_o of the layout. However, due to a large computation overhead, I_o is approximated to be the pattern density at every cell on a gridded layout as in [11] [12] to compute flare. As vacant regions on clear-field masks contribute to flare, vacancy density map is used in computation of flare map instead of pattern density. After dividing the entire layout into suitably sized rectangular grid cells, the flare $F(x, y)$ corresponding to each cell (x, y) is computed as

$$F(x, y) = D_v(x, y) \otimes PSF(x, y) \quad (1)$$

Here, $D_v(x, y)$ and $PSF(x, y)$ are respectively the vacancy density and PSF of the cell (x, y).

III. Problem Formulation

In this work, the layout for a particular interconnect layer is considered where the interconnect patterns are essentially arrangements of vertical and horizontal wire segments. This interconnect layer is referred as the layout henceforth, which is divided into rectangular fixed sized grid cells. The pattern density of each cell $D_p(x, y)$ is defined to be the ratio of the total area of its existing patterns and the maximum area of patterns that can be printed in this cell without violating the design rule. The vacancy density of a cell is thus defined as $D_v(x, y) = 1 - D_p(x, y)$. The initial flare map F for the layout can then be computed using Equation 1.

The horizontal and vertical segments of the patterns in a layout can be perturbed to change the pattern density map, and thereby the flare map. Here, perturbation of a wire segment refers to the movement of the entire segment onto a predefined routing track in a direction orthogonal to its orientation. However, moving a segment to a new location may disconnect the net, or even if it remains connected, may increase the wirelength. Hence, we define $S = \{s_i : 1 \leq i \leq n\}$ as the set of movable segments where each segment s_j can be perturbed within a *perturbation range* r_j depending on the geometry of pattern containing the segment. As flare depends on the pattern density map D_p of the layout, a target pattern density map D_p^t is computed so that it conforms with the flare map F of the gridded layout.The problem of flare minimization is defined as follows:

Given a grid based layout, determine S, the set of movable segments and perturb the segments to new locations such that the maximum flare and the variance of the flare map is minimized with minimal increase in wirelength.

In other words, the problem can be formulated as:

Given a flare conforming target density map D_p^t for a gridded layout, determine $S = \{s_j\}$, the set of movable segments with the perturbation range of r_j of each segment $s_j \in S$, and reassign these segments to the grid cells such that $\sum |D_p^t(x, y) - D_p(x, y)|$ over all grid cells is minimized.

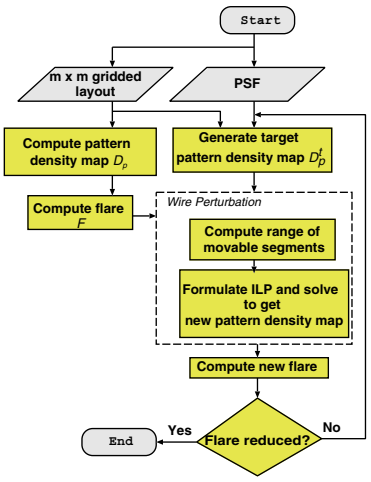

Fig. 2. Overview of flare optimization by wire perturbation

IV. Proposed Method

In this section we discuss our proposed method of minimization of flare by wire segment perturbation. Section IV-A describes the overall flow of the proposed method. Section IV-B illustrates the computation of flare conforming target pattern density map. Section IV-C elaborates the range computation for movable segments and Section IV-D presents the Integer linear programming (ILP) based formulation for the layout perturbation.

A. Overview

Figure 2 shows the overall flow of our flare minimization method. First, the pattern density map and the corresponding flare map are computed. Flare conforming target pattern density map D_p^t is estimated following the method described in Section IV-B. The perturbation range for each movable segment is computed using the method described in Section

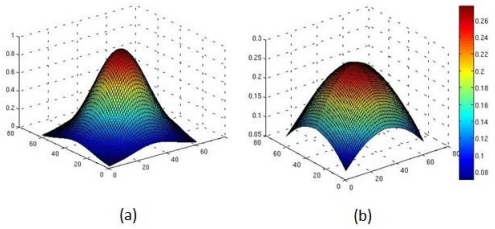

Fig. 3. (a) A 2D Gaussian function and (b) the flare map of a circuit layout

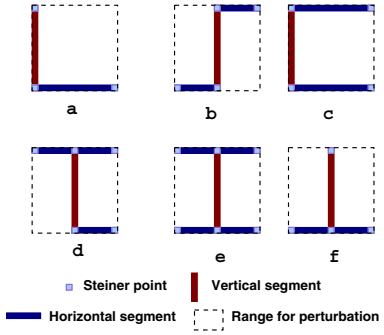

Fig. 4. Six types of patterns which can be perturbed

IV-C below. An ILP is formulated and solved to relocate the wire segments within their respective ranges. Next, the new pattern density and flare maps are computed, to check flare reduction with respect to the initial flare map. If the maximum flare has not improved, then the entire process can be repeated with a different target pattern density map.

B. Estimation of target pattern density

Flare periphery effect [3] causes higher flare at the center of the layout than the periphery in a EUVL system as discussed earlier. This phenomenon is modeled as a 2D Gaussian distribution [11]. Figures 3(a) and (b) illustrate this with a 2D Gaussian distribution and a flare map of a layout of size 61×61 grid cells respectively. As the flare of a layout always follows the Gaussian characteristics, a pattern density conforming to the flare map needs to be dense in the central region and gradually sparse towards the periphery. Thus, the target pattern density D_p^t is modeled as a Gaussian distribution with a standard deviation of σ, not necessarily same as that of the PSF.

C. Perturbation Range

In a layout, the possible patterns consisting of connected horizontal and vertical wire segments which can be perturbed with bounded increase in wirelength, are classified into six types of primitive patterns [2] as shown in Figure 4. In Figure 4 each segment is defined with two steiner points (vias) on either side. These vias are either movable, or fixed points that are connected to the pins of the blocks (terminals). This implies that a via connected to a terminal should remain fixed to maintain the connectivity with the block pin, but a via connecting two wire segments only can be moved during perturbation.

The perturbation range r_j of a wire segment s_j of a pattern is defined as the smallest enclosing rectangle containing the entire pattern. Note that the segment s_j can be moved only to a predefined routing track within the rectangular region $r_j = \{(X_{bl}, Y_{bl}), (X_{tr}, Y_{tr})\}$, where (X_{bl}, Y_{bl}) and (X_{tr}, Y_{tr}) are the co-ordinates of the bottom left and top right corners respectively, within which the perturbation of any wire segment should be confined in order to obtain a bounded increase of wirelength.

Figure 5 shows the perturbation range, and the effect of perturbation on wirelength for the pattern types shown in Figure 4(b) and (c). For the perturbation range corresponding to Figure 5(a), the Figures 5(a1), (a2) and (a3) show three possible cases of perturbation and their effects on wirelength. Let the rectangle $MNOP$ be the perturbation range r for a segment s, where N and P correspond to (X_{bl}, Y_{bl}) and (X_{tr}, Y_{tr}) respectively. The dotted arrows show the possible direction of the movement of segment s. Let, A and B be the two vias connecting h_1 and h_2 with s. The length of h_1 and h_2 may change depending on the type of the via, and the direction of the movement of s during perturbation. A perturbation with no change in wirelength is shown in the Figure 5(a1) for the pattern type in Figure 5(a), where A and B are both representing movable vias, and s is moved to the right by a distance of L_1. The length of h_2 decreases by L_1, and the length of h_1 increases by an equal amount. As a result, the total length remains same assuring no change in wirelength. The vias A and B are both moved and placed in the new positions. Similarly, s may be moved leftwards when it is connected to movable vias on both sides. In this case, the length of h_1 instead of h_2 decreases, and the length of h_2 increases by an equal amount.

Figures 5(a2) and (a3) describe the situations when the vertical wire segment has vias at the end which are connected to terminals.The pattern shown in Figure 5(a2) has via A attached to a terminal and cannot be moved. However, B is a movable via. The segment s is moved leftwards by L_2. The length of h_2 increases by L_2, and A remains intact to maintain the connection with the terminal, while a new movable via A_1 is used to keep the connection between s and h_2. The length of h_1 decreases by L_2 compensating the increase in h_2. A situation where a change in wirelength during perturbation is possible is illustrated in the Figure 5(a3). Here the type of vias A and B are same as in Figure 5(a2) but the segment s is moved rightwards by L_3 along with the movable via B connected to it. The length of h_1 increases by L_3. The length of h_2 remains same to maintain the connectivity with the terminal through fixed via A, and in order to retain the connection between s and h_2 a new movable via A_1 has to be introduced. This perturbation scenario shows increase in the total wirelength by L_3. However, this increment is restricted within the defined perturbation range.

In Figure 5(b1) and (b2) depicts the different possible situations during perturbation of the pattern shown in the Figure 5(b) in the presence of fixed and movable vias. The leftward movement of s is prohibited because any position to the left of s is outside the rectangle $MNOP$ defined for its range. Figure 5(b1) shows the rightward perturbation of s by L_4 where both A and B are movable vias. Both h_1 and h_2 decrease by L_4 which in turn decreases the wirelength. In Figure 5(b2), both A and B are fixed and s is moved rightwards by L_5 resulting in the need for two new vias A_1 and

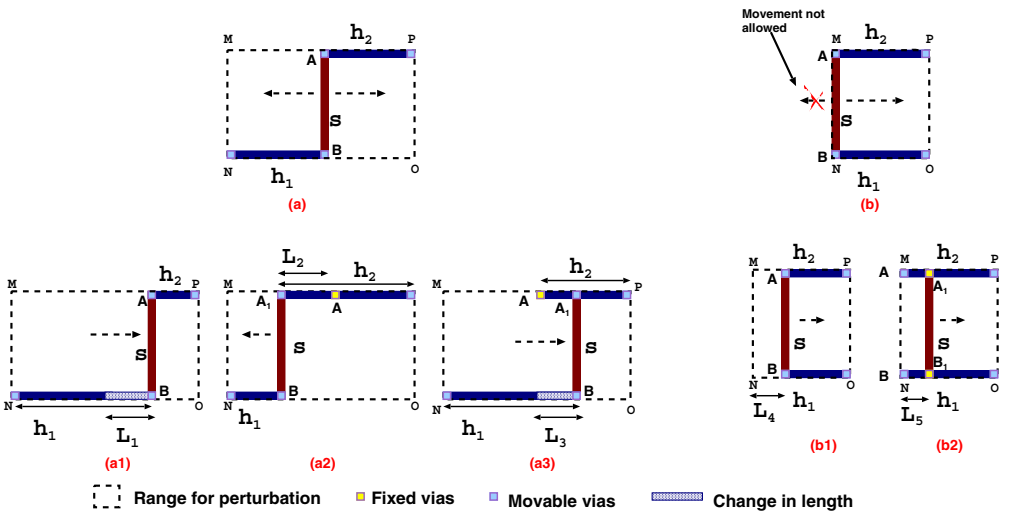

Fig. 5. Pattern (a) Type b, and (b) Type c of Fig. 4, and their respective feasible cases of perturbation within the defined perturbation range in the presence of movable and fixed vias

B_1 to connect s with h_1 and h_2 respectively. The lengths of both h_1 and h_2 remain unchanged. The concept of perturbation within a defined range described here can be applied to all the six types of patterns shown in Figure 4 with restricted change in the wirelength.

D. Layout Perturbation

Given the current pattern density map D_p, flare conforming target pattern density map D_p^t and the set of movable segments $S = \{s_j\}$ with each s_j having a perturbation range r_j, we formulate an ILP to minimize the flare of a given layout. The objective is to minimize the cumulative sum of the difference between D_p^t and the new pattern density D_p obtained by perturbation of wire segments, i.e, minimization of $\sum |D_p^t(i,j) - D_p(i,j)|$.

The movable wire segments have specific height and width in a cell. Therefore, moving a segment from one cell to another causes pattern area of the segment to be transferred from one cell to the other. This leads to approximation of all the density maps to area maps. Multiplying D_p^t with the total pattern area allowed by design rules in the corresponding cell, gives the area map A_p^t. Then, the target pattern area of a cell $A_i^{t'}$ is computed as its available area A_i^v pro-rated by the ratio of its A_i^t to the maximum of A_p^t over all grid cells.

The minimization of flare is next formulated as an ILP for each row of cells in the gridded layout. We have performed segment perturbation in two different ways. While the first does not have any constraint over the ordering of the wire segments within a row of grid cells, the second one retains the initial order of the wire segments during perturbation. These are illustrated in the Section IV-D1 and IV-D2. Let

- n_c : Number of cells in any row.
- G_R : Sequence of cells in any row from left to right, $(g_1, g_2, ..., g_{n_c})$
- n_s : Number of segments in any row.
- seg_i : Sequence of segments in i^{th} cell.
- seg_R : Sequence of segments $(s_1, s_2, ..., s_{n_s})$ in any row.
- A_j^s : Area of the j^{th} segment.
- A_i^v : Area available for allocation of the segments excluding the area of fixed segments in i^{th} cell.
- A_i^t : Pattern area for the i^{th} cell generated from D_p^t.
- A_{max}^t : Maximum of A_i^t over all grid cells.
- c_j^r : Subsequence of G_R such that c_j^r lies within the range r_j of the j^{th} segment.
- x_{ij} : 0-1 variable; 1 if segment j is assigned to i^{th} cell and 0 otherwise.
- A_i^a : Total area of the segments allocated to the i^{th} cell computed by Equation 2.
- $A_i^{t'}$: Target pattern area for the i^{th} cell computed by Equation 3.
- α : User defined parameter.

$$A_i^a = \sum_{j=1}^{n_s} x_{ij} A_j^s \ \mid \ \forall i, g_i \in G_R \tag{2}$$

$$A_i^{t'} = A_i^v \frac{A_i^t}{A_{max}^t} \ \mid \ \forall i, g_i \in G_R \tag{3}$$

The objective of minimizing the sum of differences of the target pattern area $A_i^{t'}$ and the new area A_i^a of i^{th} cell after the perturbation is formulated as below.

1) Unordered Perturbation of Wire Segments: Here we consider the case when the segments need not preserve their ordering while perturbation.

$$maximize : \sum_i A_i^a - \alpha(\sum_i |A_i^a - A_i^{t'}|) \tag{4}$$

subject to:

$$A_i^a \leq A_i^v \mid \forall i, g_i \in G_R \tag{5}$$

$$\sum_{i=1}^{n_c} x_{ij} = 1 \mid \forall j, s_j \in seg_i \tag{6}$$

The objective function in Equation 4 is essentially minimizing the difference between the total assigned area A_i^a and the target area $A_i^{t'}$ in each cell i. Equation 5 ensures that the area of segment assigned to a cell i never exceeds the available area A_i^v in it. The constraint 6 guarantees that each segment is assigned to exactly one cell.

This objective function with the modulus being non-linear, a standard technique is used to transform it into a linear one [7].

2) Constraints for Segment Ordering: Traditionally horizontal and vertical segments are on different layers. A conflict between two horizontal wire segments of same metal layer may occur if the initial ordering of the vertical wire segments connected to them are reversed by perturbation. This leads to design rule violation by two overlapping horizontal segments of different nets.

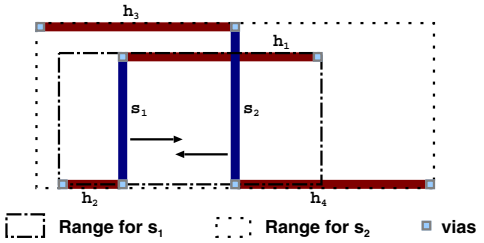

Fig. 6. Conflict between h_2 and h_4 occurs due to the movement of either in the direction shown by the corresponding arrow

Figure 6 depicts the possibility of conflict between two horizontal segment due to the change in the order of the vertical segments connected to them. In the Figure 6 any one or both of the vertical wire segments s_1 and s_2 can be perturbed towards the direction shown by the arrows. However, such perturbation can generate a conflict between horizontal segments h_2 and h_4. The lower ends of s_1 and s_2 connecting h_2 and h_4 respectively on the same routing track cause a conflict. In order to avoid such a conflict, s_2 cannot be placed anywhere in front of s_1 and vice-versa. So, we add another constraint to our ILP formulation to maintain the segment ordering, as given below.

$$x_{kp} + x_{lq} = 1, \tag{7}$$

- $\forall p, q$ s.t. $s_p \in G_R, s_q \in G_R$ and $p \leq q$
- $g_k \in c_p^r$
- $g_l \in (g_1 ... g_{k-1})$ and $g_l \in c_q^r$

Constraint 7 preserves the order between each pair of vertical wire segments by restricting the perturbation range for each segment.

TABLE I. SPECIFICATIONS OF CIRCUITS

Circuit	$W \times H$	$tr_h \times tr_v$	#Seg	$g_h \times g_v$	Range	
					Min	*Max*
ckt_A15	47 X 47	15 X 15	30	5 X 5	1	4
ckt_B15			33		1	4
ckt_C15			33		1	4
ckt_D15			34		1	4
ckt_E15			37		1	4
ckt_F15			36		1	4
ckt_A30	92 X 92	30 X 30	172	10 X 10	1	9
ckt_B30			146		1	9
ckt_C30			166		1	9
ckt_D30			141		1	9
ckt_E30			155		1	9
ckt_F30			146		1	9
ckt_A45	137 X 137	45 X 45	344	15 X 15	1	14
ckt_B45			338		1	14
ckt_C45			372		1	14
ckt_D45			337		1	14
ckt_E45			328		1	14
ckt_F45			339		1	14
ckt_G45			330		1	14
ckt_H45			318		1	14
ckt_A60	182 X 182	60 X 60	617	20 X 20	1	19
ckt_B60			600		1	19
ckt_C60			608		1	19
ckt_D60			579		1	19
ckt_E60			611		1	19

V. EXPERIMENTAL RESULTS

We have implemented our method using C on a system with Intel(R) Core(TM) i3-3217U CPU @ 1.80 GHz processor with 4GB memory. We used lp_solve package [7] for solving the ILP and MATLAB [8] for performing convolution during flare computation. We have performed our experiments on a set of randomly generated synthetic layouts described in Table I, focusing on perturbation in a layer with the reserved direction being vertical only. The input layouts are divided into equal sized cells such that each cell consist of three routing tracks. In Table I, the columns named Circuit, $W \times H$, $tr_h \times tr_v$, $\#Seg$ and $g_h \times g_v$ are the circuit name, width and height of the circuit, routing track resolution maintaining the design rule, number of movable vertical segments and cell resolution respectively. *Min* and *Max* define the minimum and maximum range possible in terms of the number of cells. The segments which increases the wirelength during perturbation are considered to be non-movable. Hence Wirelength remained same even after perturbation.

We have modeled our PSF as a Gaussian function with the peak at the center of the layout, and the standard deviation σ captures the effect of flare within 2σ distance around the center. An ILP is formulated for each row. User defined parameter α is set to be 0.5. The central area of the layout is more significant in terms of flare, thus perturbation starts from the middle row and proceeds towards the periphery. The pattern density of the input layout is modified based on the solution of the ILP satisfying the objective for reduction of flare. The values of flare computed from the initial and the new vacancy density maps are compared to report the reduction in the peak, mean and standard deviation of the flare map. Figure 7(a) and (b) show the initial and the final (post-ILP based perturbation) vacancy density maps and the corresponding flare maps for the circuit ckt_B60 respectively. The reduction in maximum flare in the final flare map is 18% for unordered formulation.

In Table II, the columns labeled Max, $StdDev.$ and $Mean$ show the maximum flare, standard deviation of flare and mean

TABLE II. COMPARISON OF FLARE LEVEL : INITIAL VS. OUR FINAL OUTPUT

Circuit	Initial			unordered					ordered				
	Max	Mean	Std Dev.	Max	Mean	Std Dev.	%Perturbed	Time(s)	Max	Mean	Std Dev.	%Perturb	Time(s)
ckt_A15	0.608	0.378	0.27205	0.563	0.353	0.25592	70.00	0.02	0.565	0.354	0.25947	56.67	0.01
ckt_B15	0.556	0.345	0.24708	0.503	0.317	0.22542	57.58	0.01	0.513	0.323	0.23150	48.48	0.01
ckt_C15	0.552	0.343	0.24659	0.525	0.329	0.23594	51.52	0.02	0.528	0.330	0.23726	39.39	0.02
ckt_D15	0.532	0.335	0.24178	0.501	0.316	0.22825	44.12	0.02	0.511	0.323	0.23176	26.47	0.02
ckt_E15	0.496	0.309	0.22054	0.459	0.291	0.20958	70.27	0.01	0.460	0.290	0.20624	43.24	0.03
ckt_F15	0.508	0.317	0.22993	0.475	0.297	0.22349	44.44	0.02	0.482	0.049	0.54946	27.78	0.02
ckt_A30	0.143	0.096	0.05269	0.121	0.091	0.04741	63.37	0.05	0.133	0.093	0.04865	43.60	1.78
ckt_B30	0.177	0.118	0.06535	0.163	0.112	0.05921	69.86	0.04	0.167	0.115	0.06107	44.52	1.52
ckt_C30	0.159	0.107	0.05691	0.146	0.101	0.05264	58.43	0.04	0.148	0.102	0.05330	30.12	1.28
ckt_D30	0.197	0.130	0.06956	0.163	0.122	0.06160	65.96	0.04	0.189	0.126	0.06727	43.26	0.83
ckt_E30	0.171	0.117	0.06138	0.152	0.111	0.05656	59.35	0.05	0.159	0.112	0.05730	48.39	1.15
ckt_F30	0.188	0.124	0.06570	0.165	0.119	0.06144	65.07	0.04	0.167	0.119	0.06120	49.32	0.72
ckt_A45	0.199	0.134	0.06034	0.173	0.129	0.05442	71.51	0.18	0.187	0.131	0.05790	38.66	35.83
ckt_B45	0.214	0.140	0.06468	0.179	0.133	0.05685	67.75	0.14	0.192	0.134	0.05994	54.44	117.75
ckt_C45	0.193	0.126	0.05836	0.154	0.119	0.05034	68.28	0.16	0.172	0.119	0.05301	45.70	132.74
ckt_D45	0.215	0.141	0.06559	0.185	0.133	0.05758	73.29	0.19	0.183	0.134	0.05819	49.85	87.99
ckt_E45	0.209	0.141	0.06341	0.184	0.136	0.05809	68.29	0.16	0.187	0.136	0.05892	47.26	52.46
ckt_F45	0.210	0.140	0.06414	0.186	0.133	0.05749	69.91	0.16	0.193	0.135	0.06060	44.25	98.07
ckt_G45	0.216	0.144	0.06597	0.180	0.135	0.05747	70.91	0.13	0.191	0.137	0.05977	46.36	48.28
ckt_H45	0.216	0.145	0.06589	0.197	0.139	0.05987	68.24	0.16	0.188	0.138	0.05936	55.35	218.00
ckt_A60	0.167	0.115	0.04657	0.142	0.110	0.04123	73.58	0.31	0.149	0.110	0.04258	52.84	1087.00
ckt_B60	0.176	0.120	0.04916	0.145	0.113	0.04258	73.33	0.36	0.152	0.114	0.04369	56.17	3042.86
ckt_C60	0.176	0.118	0.04907	0.144	0.111	0.04186	73.85	0.34	0.158	0.113	0.04462	50.16	3136.62
ckt_D60	0.185	0.124	0.05122	0.155	0.118	0.04491	74.78	0.35	0.166	0.120	0.04709	56.13	2617.30
ckt_E60	0.182	0.119	0.05036	0.147	0.112	0.04287	73.32	0.35	0.160	0.114	0.04534	52.70	1232.00
Geo Mean	0.242	0.159	0.08266	0.212	0.151	0.07466	-	-	0.221	0.152	0.07679	-	-
Normalized	1	1	1	0.874	0.90323	0.947	-	-	0.912	0.957	0.92904	-	-

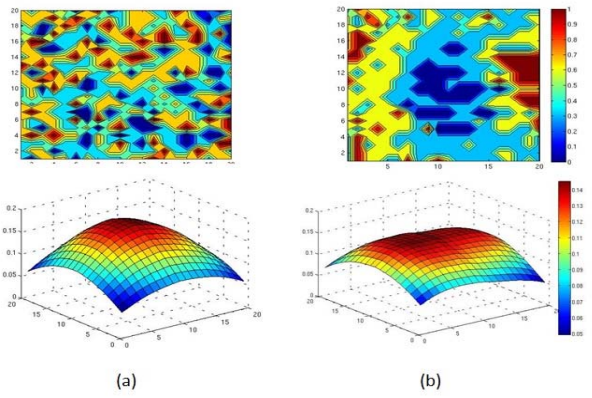

Fig. 7. (a) Initial vacancy density map (top) and flare map (bottom) of ckt_B60, and (b) final maps after ILP-based perturbation

flare. The percentage of the total number of segments which are perturbed and the CPU time in seconds appear under $\%Perturb$ and $Time$. Experimental results show a reduction of 12.6% and 8.8% in maximum flare, 5.3% and 4.3% in flare mean flare, and 9.7% and 7.1% in the standard deviation of flare for the cases of unordered and ordered formulations respectively. Flare reduction is lower in the ordered formulation than that for the unordered because in the ordered case the perturbation range for each wire segment is more restricted.

VI. CONCLUSION

This paper presents the first method on reduction of flare using wire segment perturbation in EUVL system without dummification, thus reducing the mask cost. The dummification after wire perturbation will lead to lesser dummies while reducing more flare. The impact of dummification, timing and cross-talk after perturbation will be studied in future.

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