ADC INTERFACING WITH PT 51 USING SPI

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Introduction:

In this experiment we are using the ADC – MCP 3008. The ADC can be given single ended or differential analog inputs and it produces 10 bit digital output. This 10 bit digital output is available on the D_{out} pin of the ADC serially. We are interfacing this with Pt 51 microcontroller. The microcontroller takes this 10 bit input and modifies data appropriately.

ADC interfacing with Pt51

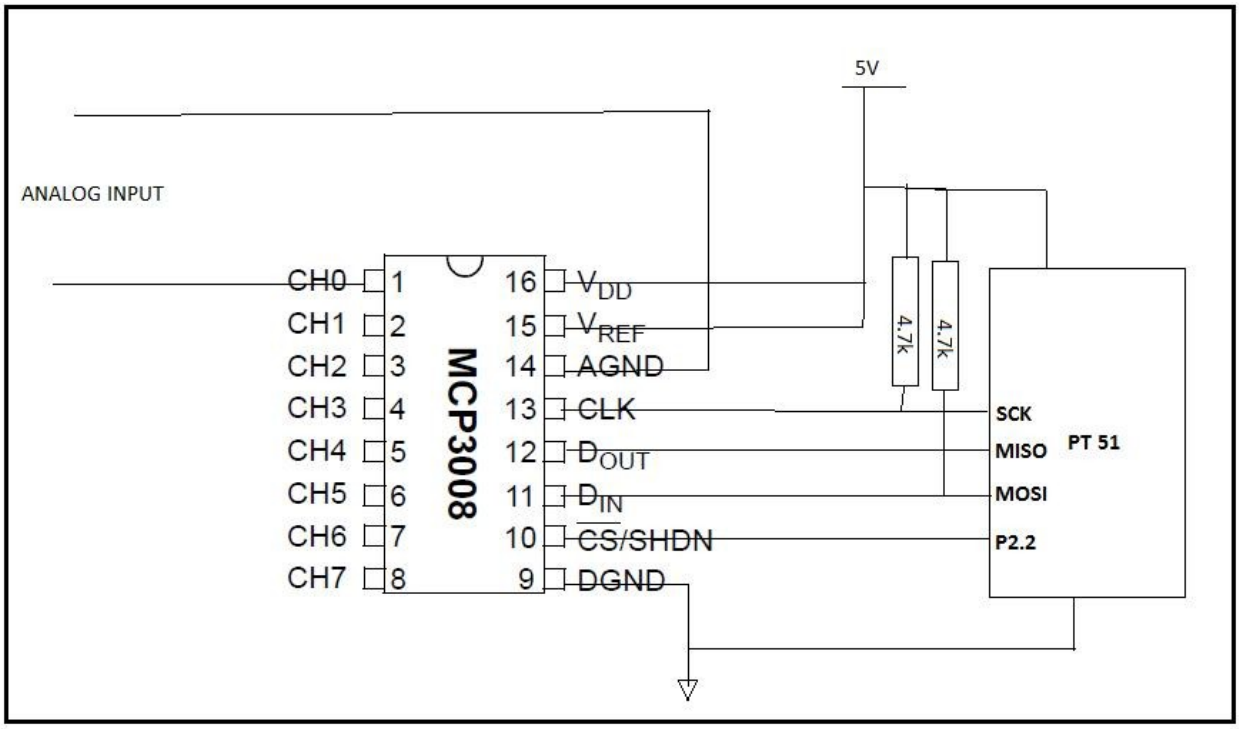

Figure 1: connection diagram

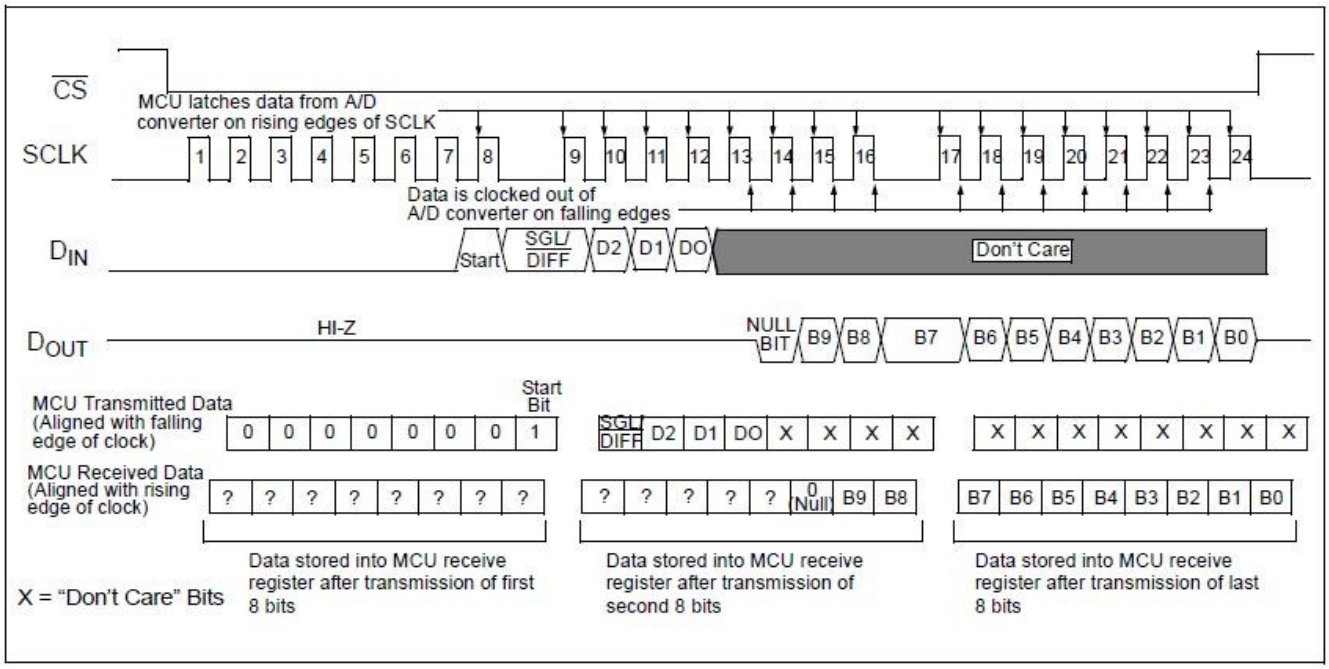

Figure 2 : Timing diagram

The SPI pins on the microcontroller are as follows:

Pin	**Function**	**Description**
P1.4	SS_{bar}	Chip Select
P1.5	MISO	Serial Input
P1.6	SCK	Serial Clock
P1.7	MOSI	Serial Output

The pins on the Pt-51 board marked “SPI” can be used for connecting wires to the ADC

Steps for ADC interfacing:

1. Configure the SPCON register as described below.

2. Enable SPI communication.

3. Make CS pin of ADC low to select it.
4. As shown in timing diagram send logic high to D_{in} of ADC to indicate start of conversion, followed by single/differential mode selection, followed by channel selection for ADC input.

5. Thus the corresponding digital data is obtained at D_{out} pin: null bit followed by 10 bits (MSB first). Refer MCP3008 datasheet for more details.

6. After the successful reception of 10 bit of data CS pin of ADC is made high.

7. The data bits transmission and reception from microcontroller should be done as per the alignment shown in timing diagram.

Steps to configure SPCON register:

1. Free the SS pin for a general-purpose

2. Select one of the Master clock rates (by choosing appropriate values of SPR0, SPR1, SPR2 we can get different baud rates. Select the appropriate baud rate)

3. Configure the SPI module as Master (in this case)

4. Selects serial clock polarity and phase(1,1) or (0,0)

5. Enable the SPI module (SPEN = 1)

SPCON Register

SPCON - Serial Peripheral Control Register (0C3H)

7	6	5	4	3	2	1	0
SPR2	**SPEN**	**SSDIS**	**MSTR**	**CPOL**	**CPHA**	**SPR1**	**SPR0**

Bit Number	Bit Mnemonic	Description
7	SPR2	**Serial Peripheral Rate 2** Bit with SPR1 and SPR0 define the clock rate.
6	SPEN	**Serial Peripheral Enable** Cleared to disable the SPI interface. Set to enable the SPI interface.
5	SSDIS	**$\overline{\text{SS}}$ Disable** Cleared to enable $\overline{\text{SS}}$ in both Master and Slave modes. Set to disable $\overline{\text{SS}}$ in both Master and Slave modes. In Slave mode, this bit has no effect if CPHA = "0".
5	MSTR	**Serial Peripheral Master** Cleared to configure the SPI as a Slave. Set to configure the SPI as a Master.
4	CPOL	**Clock Polarity** Cleared to have the SCK set to "0" in idle state. Set to have the SCK set to "1" in idle low.
3	CPHA	**Clock Phase** Cleared to have the data sampled when the SCK leaves the idle state (see CPOL). Set to have the data sampled when the SCK returns to idle state (see CPOL).
2 1	SPR1 SPR0	**SPR2 SPR1 SPR0 Serial Peripheral Rate** 0 0 0 Invalid 0 0 1 $F_{CLK\ PERIPH}/4$ 0 1 0 $F_{CLK\ PERIPH}/8$ 0 1 1 $F_{CLK\ PERIPH}/16$ 1 0 0 $F_{CLK\ PERIPH}/32$ 1 0 1 $F_{CLK\ PERIPH}/64$ 1 1 0 $F_{CLK\ PERIPH}/128$ 1 1 1 Invalid

Reset Value = 0001 0100b

IMPORTANT FORMULAE FOR VOLTAGE CONVERSION CALCULATION:

ADC:

$$LSB\ Size = \frac{V_{REF}}{1024}$$

$$Digital\ Output\ Code = \frac{1024 \times V_{IN}}{V_{REF}}$$

Where:

V_{IN} = analog input voltage

V_{REF} = analog input voltage