

Lesson Plan

Digital Logic

Credits: 4

Textbook: Digital Design: With an Introduction to the Verilog HDL, VHDL, and System Verilog, 6th Edition
M. Morris Mano & Michael D. Ciletti

Lecture Number	Topic
Lecture 1	Introduction to the course & Digital Systems
Lecture 2	Number System: Number Base Conversions <ul style="list-style-type: none">- Decimal to other number system conversion and vice versa- Binary to Octal- Binary to Hexadecimal
Lecture 3	<ul style="list-style-type: none">- Binary arithmetic(addition and subtraction)- Complements of Numbers (r and r-1complement)
Lecture 4	Subtraction using complement (1s&2s)
Lecture 5	Binary Codes
Lecture 6	Boolean Algebra & Logic Gates: Basic Definitions, Basic Theorems and Properties of Boolean Algebra
Lecture 7	Boolean functions, Simplification of Boolean functions using Boolean Algebra rules
Lecture 8	Introduction to Hardware Description Language (Gate-level modeling, Dataflow modeling, Behavioral modeling)
Lecture 9	Complement of Boolean Function, canonical and standard form, HDL Description of Boolean Functions
Lecture 10	Other Logic operations, Digital Logic gates, Integrated Circuits
Lecture 11	Gate Level Minimization Simplification of Boolean functions using Map method (Two and Three variable map methods), HDL Description of Simplified Boolean Functions
Lecture 12	Simplification of Boolean functions: 4 variable maps, Concept of 5 and 6 variable map, HDL Description of Simplified Boolean Functions
Lecture 13	Simplification of Boolean functions using K map with don't care conditions, HDL Description of Simplified Boolean Functions
Lecture 14	SOP & POS implementation using NAND & NOR gates, HDL Description of the circuit.
Lecture 15	Multilevel NAND, NOR circuits, Exclusive OR and Equivalence Functions, HDL Description of the circuit.
Lecture 16	Introduction to Combinational Logic- Combinational circuit analysis and design procedure, HDL Description of the circuit
Lecture 17	Binary Adder, HDL Models for Adder
Lecture 18	Binary Subtractor, HDL Models for Subtractor

Lecture 19	Code conversion and Analysis Procedure
Lecture 20	Binary Parallel adder, HDL Models for Binary Parallel Adder
Lecture 21	Decimal Adder, Magnitude Comparator, HDL Models of Magnitude Comparator
Lecture 22	Decoders, Combinational Logic design using Decoders, Encoders HDL Models for Combinational Circuits (Decoder, Encoder)
Lecture 23	Multiplexers, Combinational Logic design using Multiplexers
Lecture 24	HDL Models for Combinational Circuits using Multiplexer
Lecture 25	Introduction to Sequential Circuits, Storage Elements: Latches, HDL Description of Latch
Lecture 26	Storage Elements: Flip Flops RS flip-flop (Graphical Symbol, Logic Diagram, Function Table, Characteristics Table, Characteristics Equation, Excitation table) HDL Description of RS Flip Flop
Lecture 27	Storage Elements: Flip Flops JK flip-flop (Graphical Symbol, Logic Diagram, Function Table, Characteristics Table, Characteristics Equation, Excitation table) HDL Description of JK Flip Flop
Lecture 28	Storage Elements: Flip Flops D and T flip-flop (Graphical Symbol, Logic Diagram, Function Table, Characteristics Table, Characteristics Equation, Excitation table) HDL Description of Flip Flops
Lecture 29	Master-slave Flip Flop, Analysis of clocked Sequential Circuits
Lecture 30	Analysis of clocked Sequential Circuits contd.
Lecture 31	State Reduction and Assignment
Lecture 32	Design Procedure of clocked sequential circuit
Lecture 33	Register, Shift Registers, HDL Models for Shift Register
Lecture 34	Design of Ripple Counters with timing sequences
Lecture 35	Design of Synchronous counters,
Lecture 36	Design of Synchronous counters contd.
Lecture 37	Design of Synchronous counters contd.
Lecture 38	HDL Models for Counters
Lecture 39	Memory : Random Access Memory, Read Only Memory, Programmable Logic Array, Programmable Array Logic, HDL Description for Read and write operations of memory
Lecture 40	Introduction to Register Transfer Level(RTL)