Debasish Das

5069 Xavier Common
Fremont, CA 94555
Email: debasish.das83@gmail.com
Phone: (408) 313-2465
Portfolio LinkedIn

OBJECTIVE

Technical Lead position focused on design and implementation of large scale data pipelines and machine learning algorithms.

EDUCATION

Doctoral in Computer Engineering GPA : 3.9/4.0
Department of Electrical Engineering and Computer Science,
Robert R McCormick School of Engineering and Applied Sciences,
Northwestern University, Evanston, USA

Bachelor of Technology (B.Tech, Hons, 2004) GPA : 8.3/10.0
Department of Computer Science and Engineering
India Institute of Technology, Kharagpur, India

TECHNICAL SKILLS

- Languages: Scala, Java, C/C++, Javascript, Python, Tcl, Visual C++, Verilog
- Skills: Spark, Lucene, Solr, Cassandra, HBase, Akka, YARN, HDFS, Distributed Systems, Machine Learning, Convex Optimization, Linear Programming, Multithreading, Algorithms, Data Structures, Automatic Differentiation
- Tools: gdb, lex, yacc, gprof, CPLEX, AMPL, TLA+, Mentor Graphics EDA Suite, Synopsys DC/ICC

OPEN SOURCE

- Data Access Object for Spark, Lucene and Solr integration to support hybrid row/column storage and search for machine learning flows
- Framework for building Batch, Streaming and API workflows using Spark and Akka compute
- Contributed recommendAll feature to Spark MLlib
- Constrained Matrix Factorization for recommendation and topic modeling
  Spark Summit 2014 Presentation
- Row based similarity computation and Twitter DimSum comparisons
  Spark Meetup 2015 Presentation
- Quadratic and Nonlinear Programming solvers using ADMM
- Conic Solver for JVM and Spark integration

EXPERIENCE

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Distinguished Engineer / Software Architect   May 2013 - Present
Verizon, Palo Alto, CA, USA
Advisor: Ashok Srivastava, Professor Stephen Boyd

- Advertising: Verizon Audience Insight for building Audience using Temporal, Location, Clickstream and CRM attributes from Verizon Wireless datasets and serve ads on Oath properties (yearly revenue 25 Million)
- Marketing: Near-RealTime Lookalike Modeling, Discriminant Analysis and Demand Forecasting for Audience
  Spark Summit East 2017 Presentation
  Spark Summit East 2016 Presentation

- Platform-as-a-Service: Verizon Insight deployment for international carriers powered by trapezium (yearly revenue 10 Million)
- IoT Security: Streaming DDoS Detection on Verizon Wireline datasets using statistical, autoregressive and k-NN models
  Hadoop Summit Tokyo 2016 Presentation
- Architecture validation for OLAP store using Solr, Druid and internally developed LuceneDAO
- Leading collaboration across Platform, Data Engineering and Data Science teams to hit timely release schedules
- Provided technical guidance and coaching to developers, and conducted design discussion, code review and data validation.

Staff Research and Design Engineer   April 2012 - Present
Synopsys Inc, Mountain View, CA, USA
Advisor: Will Naylor
- Generating timing models from post-routed sign-off timing data using physical models and convex machine learning techniques (nonlinear regression). For solution QoR and runtime, compared effectiveness of Batch/Stochastic Gradient Descent, Conjugate Direction, Conjugate Gradient and L-BFGS-B solvers.
- Benchmarked internal network simplex solvers with cost scaling push-relabel algorithm and IBM CPLEX network optimizer. Network flow solvers are used in density optimization for top level fragmented floorplans.

Member of Consulting Staff   May 2011 - Present
Magma Design Automation, San Jose, CA, USA (Acquired by Synopsys Inc)
Manager: Saurabh Adya
- Developed algorithms to solve quadratic programs with nonlinear objectives derived from performance and legality constraints of VLSI circuit placement in Talus Vortex and Talus FX platform.
- Developed timing objective driven placement algorithms for quadratic programming based placement framework.
- Used multithreading and streaming instructions to generate efficient implementation of the proposed optimization algorithms.

Place and Route Development Engineer   September 2009 - May 2011
Mentor Graphics, San Jose, CA, USA
Manager: Arash Hassibi and Phiroze Parakh
- Developed an automatic differentiation engine (Direct Timing) for handling timing constraints in an analytical timing framework. This engine is used to generate derivatives of timing QoR metrices (TNS and WNS) with respect to placement coordinates.
- Developed the vectorized and scalable multithreaded version(3X faster on 1 thread and 6X faster on 4 threads than production Timer) of Direct Timing engine.
- Developed analytical placement algorithms that use Direct Timing to generate descent direction and guide analytical placer to produce better timing QoR(TNS and WNS) without affecting wirelength and routability metrics.
- Developed Augmented Lagrangian based algorithms using core Quasi Newton Solvers (L-BFGS/L-BFGS-B) to solve large scale nonlinear/linear constrained optimization problems (tested upto 100M nodes and edges) involving wirelength, spread and direct timing modules.

Research Assistant   Spring 2005 - August 2009
EECS Department, Northwestern University, Evanston, IL, USA

Advisor: Professor Hai Zhou

- Developed algorithms and charge sharing based models to improve efficiency and accuracy of iterative Static timing analysis with crosstalk effects for early stages of design cycle. Industry collaborators were Strategic CAD Lab, Intel and Faraday Technology.
- Developed a sub-gradient optimizer for general gate sizing problem. Assuming the convexity on gate delays, developed an efficient method of feasible direction based solver to improve the efficiency of general purpose sub-gradient optimizer (which is the state-of-the art algorithm for sizing used in industry). This project is supported in parts by a NSF grant and a grant from Intel.
- Developed an efficient incremental algorithm for minimum period retiming in general delay models for NSF supported project. Our algorithm achieved average performance and memory improvements of 100X and 40X over previously proposed algorithm.

Research Assistant   Fall 2004 - Winter 2005
EECS Department, Northwestern University, Evanston, IL, USA
Advisor: Professor Seda Memik

- Developed an algorithm to save leakage power in FPGAs using multiplexer shutdown.
- Developed a tool based on VPR for the analysis of routing patterns in FPGAs.

Graduate Summer Intern   Fall 2007 - Winter 2008
Magma Design Automation, San Jose, CA, USA
Advisor: Dr. William Scott

- Developed a current based model to improve efficiency and accuracy of crosstalk induced delta delay computation for coupling analysis in late design stages. Model is generated from delay and slew tables rather than ECSM/CCSM data.
- Reviewed state-of-the-art coupling analysis algorithms and found their ineffectiveness with extreme interconnect scaling for present and future process nodes.
- Developed an algorithm based on the convexity of aggressor alignment curve to compute spice accurate crosstalk delta delay improving the ineffectiveness of present analysis algorithms.

Graduate Summer Intern   Summer 2007
Circuit Simulation Group, Intel Corporation, Santa Clara, CA, USA
Manager: Dr. Eric Grimme

- Improved the complexity of general purpose transistor sizing by removing the constraints using lagrange multipliers from cell based sizer.
- Developed a hybrid algorithm to merge sub-gradient optimization techniques used in standard cell based sizer with nonlinear optimization techniques used for transistor sizing.

Graduate Summer Intern   Summer 2006
Strategic CAD Lab, Intel Corporation, Hillsboro, OR, USA
Manager: Dr. Noel Menezes
Advisor: Kip Killpack and Dr. Chandramouli Kashyap

- Developed an iterative algorithm for pessimism reduction in static timing analysis in presence of crosstalk using logic and timing filtering.
- Derived a sensitivity based metric to select important aggressors for logic constraints analysis.

Graduate Summer Intern   Summer 2005
Calypto Design System Inc, San Jose, CA, USA

Manager: Dr. Sumit Roy
Advisor: Rajat Subhra Mukerjee and Abhishek Ranjan

- Enhancements to SLEC Optimization engine like propagating constants across different types, optimization of scan-latch designs and strength reductions.
- Developed an efficient timing macromodeling algorithm for word level static timing analysis. For timing analysis of system level designs, fast generation of accurate timing macromodel for system level blocks are essential.

ACHIEVEMENTS

- Verizon Spotlight Award for design and implementation of lambda architecture for streaming anomaly detection flows using Spark, Spark Streaming, Hive and Cassandra.
- Place and Route Division, Mentor Graphics Excellence Award for architecting the multithreaded direct timing engine to drive timing driven placement.
- Place and Route Group Excellence Award for developing the timing driven placement engine TESLA and replace the old offering with the new engine.
- Nominated for Intel Foundation PhD Fellowship from Robert R McCormick School of Engineering and Applied Sciences, Northwestern University for year 2007.
- Awarded Walter P Murphy Fellowship by the Department of Electrical Engineering and Computer Science, Robert R McCormick School of Engineering and Applied Sciences, Northwestern University for 2004-2005.

IMMIGRATION STATUS   Green Card

REFERRED PUBLICATIONS

- Somsubhra Mondal, Debasish Das and Seda Memik. Hierarchical LUT Structures for Leakage Power Reduction, Poster Paper, Proc. International Symposium on FPGAs (FPGA), Monterey, CA, 2005.
- Debasish Das, Ahmed Shebaita, Hai Zhou, Yehea Ismail and Kip Killpack. FA-STAC: A Framework for Fast and Accurate Static Timing Analysis with Coupling, IEEE International Conference on Computer Design (ICCD), San Jose, CA, 2006.
- Debasish Das, Ahmed Shebaita, Yehea Ismail, Hai Zhou and Kip Killpack. Nostra-XTalk: A Predictive Framework for Accurate Static Timing Analysis in UDSM VLSI Circuits, ACM Great Lakes Symposium on VLSI (GLSVLSI), Stresa, Italy, 2007.
- Jia Wang, Debasish Das and Hai Zhou. Gate Sizing by Lagrangian Relaxation Revisited, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), San Jose, CA, 2007
- Debasish Das, Kip Killpack, Chandramouli Kashyap, Abhijit Jas and Hai Zhou. Pessimism Reduction in Coupling Aware Static Timing Analysis Using Timing and Logic Filtering, IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Seoul, Korea, 2008. (Best Paper Award Nominee : 10/350)
- Debasish Das, William Scott, Shahin Nazarian and Hai Zhou. An efficient Current Based Logic Cell Model for Crosstalk Delay Analysis, Accepted to International Symposium on Quality Electronic Design (ISQED), San Jose, CA, 2009.
- Debasish Das, Jia Wang and Hai Zhou. iRetILP: An efficient incremental algorithm for min-period retiming under general delay model, Accepted to IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Hsinchu, Taiwan, 2010.

- Jia Wang, Debasish Das, and Hai Zhou. Gate Sizing by Lagrangian Relaxation Revisited. Accepted to IEEE Transactions on Computer-Aided Design (TCAD).
- Debasish Das, Ahmed Shebaita, Hai Zhou, Yehea Ismail and Kip Killpack. FA-STAC: An Algorithmic Framework for Fast and Accurate Coupling Aware Static Timing Analysis. Accepted to IEEE Transactions on VLSI (TVLSI).
- Debasish Das, Kip Killpack, Chandramouli Kashyap, Abhijit Jas and Hai Zhou, Pessimism Reduction in Coupling Aware Static Timing Analysis Using Timing and Logic Filtering. Accepted to IEEE Transactions on Computer-Aided Design (TCAD).
- Ahmed Shebaita, Debasish Das, Dusan Petranovic and Yehea Ismail, A Novel Moment Based Framework For Accurate and Efficient Static Timing Analysis. Accepted to IEEE Transactions on Computer-Aided Design (TCAD).

NONREFERRED PUBLICATIONS

- Debasish Das, Jia Wang and Hai Zhou. iRetILP: An efficient incremental algorithm for min- retiming under general delay model, Accepted to ACM International Workshop on Timing Issues (TAU), Austin, TX, 2009.
- Debasish Das, William Scott, Shahin Nazarian and Hai Zhou. An Efficient Current Based Logic Cell Model for Crosstalk Delay Analysis,ECM workshop, IEEE/ACM International Conference on Computer Aided Design, San Jose, CA, 2008.
- Abhijit Jas, Kip Killpack, Chandramouli Kashyap, Debasish Das and Hai Zhou. Using Boolean Satisfiability to Eliminate False Aggressor Combinations in Timing Analysis, International Test Synthesis Workshop, San Antonio, Texas, USA, 2007.
- Debasish Das. Symbolic Solver for live variable analysis of high level design languages. Accepted to IEEE Computer Society Annual Symposium on VLSI, Karlsruhe, Germany, 2006.
- Debasish Das, Abhishek Ranjan, Sumit Roy and Venky Ramachandran. Efficient Timing Macromodeling for Word Level Static Timing Analysis, Internal Report, Calypto Design Systems Inc.

SCORES

- GRE: Quantative:800/800 Verbal:550/800 Analytical:4.5/6.0
- TOEFL: 270/300, TSE: 45/60

RELEVANT COURSES

Graduate Courses
Computer Architecture, VLSI System Design, Introduction to VLSI CAD, Design and Analysis of High Speed ICs, Formal Techniques in Design and Verification of Digital Systems, Design and Analysis of Algorithms, Advanced Algorithms, Seminar on Computer Security and Information Assurance, Random Processes in Communications and Control I, Advanced Computer Architecture II, Numerical Methods for Engineers, Mathematical Programming

Undergraduate Courses
Programming and Data Structure, Discrete Structures, Switching Circuits and Logic Design, Design and Analysis of Algorithms, Computer Organization and Architecture, Formal Language and Automata Theory, Operating Systems, Computer Networks, Microprocessors and Microcontrollers, Software Engineering, Electronic Design Automation, Artificial Intelligence, Compiler Construction, VLSI System Design, Embedded Systems, Applied Graph Theory, Low power circuits and systems, File

Organization and Database Systems, Basic Electronics, Electrical Technology, Electromagnetic Engineering, Semiconductor Devices, Probability and Statistics, Signals and Networks, Linear Algebra.

ADDITIONAL ACTIVITIES

- Advisory Council member of IBM Spark Technology Center
- Reviewer for SIAM Data Mining, ICDM, TCAD, TVLSI, DAC, ICCAD, ISPD, ISQED, TAU and VLSI India
- Teaching Assistant for ECE203 (Introduction to Computer Engineering) Fall, Spring 2005, ECE231 (Advanced Programming for Computer Engineers) Winter 2006, ECE357 (Introduction to VLSI CAD) Fall 2006, EECS366 (Design and Analysis of Algorithms) Winter 2006.

REFERENCES

- Ashok Srivastava, SVP, Intuit Systems, Mountain View, USA

- Professor Stephen Boyd, Department of EE, Stanford University, USA

- Dr. Premal Buch, CEO, Robin Systems, San Jose, USA

- Dr. Phiroze Parakh, MTS, Google, Mountain View, USA

- Dr. Arash Hassibi, CEO and Founder, Joined App, Palo Alto, USA

- Dr. Sumit Roy, Group Director, Synopsys Inc, Mountain View, USA

- Professor Hai Zhou, Department of EECS, Northwestern University, USA

- Professor Yehea Ismail, Department of EECS, Northwestern University, USA

- Dr. Noel Menezes, Manager, Strategic CAD Lab, Intel Corporation, USA

- Dr. Eric Grimme, Manager, Circuit Simulation Group, Intel Corporation, USA

- Professor Ajit Pal, Department of CSE, IIT Kharagpur, India