The trend of 2D transistors toward integrated circuits: Scaling down and new mechanisms

Yang Shen[1, †], *Zuoyuan Dong*[2, †], *Yabin Sun*[2, †], *Hao Guo*[3, †], *Fan Wu*[1], *Xianglong Li*[2], *Jun Tang*[3], *Jun Liu*[3], *Xing Wu*[2*], *He Tian*[1*], *Tian-Ling Ren*[1*]

[1]Institute of Microelectronics and Beijing National Research Center for Information Science and Technology (BNRist), Tsinghua University, Beijing 100084, China

[2]Shanghai Key Laboratory of Multidimensional Information Processing, School of Communication and Electronic Engineering, East China Normal University, Shanghai 200241, China

[3]Shanxi Province Key Laboratory of Quantum Sensing and Precision Measurement, School of Instrument and Electronics, North University of China, Taiyuan 030051, Shanxi province, China

*E-mail: RenTL@tsinghua.edu.cn, tianhe88@tsinghua.edu.cn, xwu@cee.ecnu.edu.cn

[†]These authors contributed equally to this work

Keywords: 2D semiconductor, device engineering, scaling down, new mechanisms, physical models, very large-scale integration (VLSI)

Abstract:

Two-dimensional (2D) transition metal chalcogenide (TMDC) materials, such as MoS_2, have recently attracted considerable research interest in the context of their use in ultra-scaled devices owing to their excellent electronic properties. Microprocessors and neural network circuits based on MoS_2 have been developed at a large scale but still do not have an advantage over silicon in terms of their integrated density. In this study, we review the current structures, contact engineering, and doping methods for 2D TMDC materials for the scaling-down process and performance optimization. Devices are introduced according to a new mechanism to provide the comprehensive prospects for the use of MoS_2 beyond the traditional complementary–metal–oxide semiconductor (CMOS) in order to summarize obstacles to the goal of developing high-density and low-power integrated circuits (ICs). Finally, we briefly analyze prospects for the use of MoS_2 in large-scale ICs from the perspectives of the material, system performance, and application to non-logic functionalities such as sensor circuits and analogous circuits. The latter issue is along the direction of "more than Moore" research.

1. Introduction

Since the invention of the first transistor at Bell Labs in 1947 [1], human society has advanced from the age of the electron tube to that of the transistor. The IC was subsequently developed in 1958~1959 [2], and the semiconductor and IC industries have since progressed at a dizzying pace. Driven by the well-known Moore's law [3-4], the size of features of metal oxide–semiconductor–field-effect transistors (MOSFETs) continues to decrease. Such critical dimensions as the gate length L_g have decreased by hundreds of times, from the order of micrometers to nanometers at present, such that currently used transistors occupy a much smaller area and have a considerably higher speed. More than five billion transistors have been integrated into current 5 nm processing technology. As the silicon channel becomes

ultra-thin, the scattering becomes severe and leads to a significant reduction in mobility. Two-dimensional (2D) materials have attracted extensive research interest due to their mobility and sustainability, even with atomic-level thickness.

2D materials are more feasible than 1D materials for manufacturing complex structures [5-6]. Graphene is one of the most widely studied 2D materials because of its high electron mobility [7] and rich physical properties [5, 8-10]. However, the semi-metal properties of graphene constrain its application to novel devices [11] because the bandgap is an essential property for FET [12-13]. 2D transition metal chalcogenide (TMDC) materials have emerged as a core topic of interest in the semiconductor community, and have a wide range of properties, ranging from those of metals (NbS_2, TaS_2) [14-15] and semiconductors (MoS_2, WSe_2) [5, 16] to superconductors ($NbSe_2$, $TaSe_2$) [17-19]. TMDCs are 2D layered materials with the chemical formula MX_2, where M is a transition metal, such as Mo, W, and Pt, and X is a chalcogen, such S and Se. 2D TMDC materials have emerged as promising candidates for next-generation semiconductors in recent years. They usually have a sizable bandgap, are ultra-thin, and have other excellent electronic properties. MoS_2 is one of the most attractive 2D materials in this regard. Many common 2D TMDCs have strong in-plane covalent bonds and weak van der Waals interactions between neighboring layers, leading to easy mechanical exfoliation. Single-layer MoS_2 with a direct bandgap can be introduced as a critical material to optoelectronic devices to provide multiple functionalities. Furthermore, the tunability of the bandgap based on strain and the dielectric environment, and by tailoring the number of layers offers more opportunities for its use in various electronic devices. Moreover, 2D materials play an important role in flexible electronics and ultra-sensitive sensors [20-21]. Considering their advantages of biocompatibility, a high surface-to-volume ratio, and robust covalent bonding within a layered plane of the material, many studies have used 2D materials as biosensors and flexible materials.

In this review, we discuss 2D semiconductors from the perspective of device engineering in light of new mechanisms for very large-scale integration (VLSI), as shown in **Fig. 1**. We first summarize currently available ultra-scaled 2D transistors and highlight the importance of device engineering, including through doping and contact. We then introduce the development of 2D transistors based on new physical mechanisms that offer improvements and opportunities for their use in 2D VLSI. Millstone studies in 2D semiconductor-based ICs are subsequently summarized. Finally, outstanding challenges to VLSI are discussed.

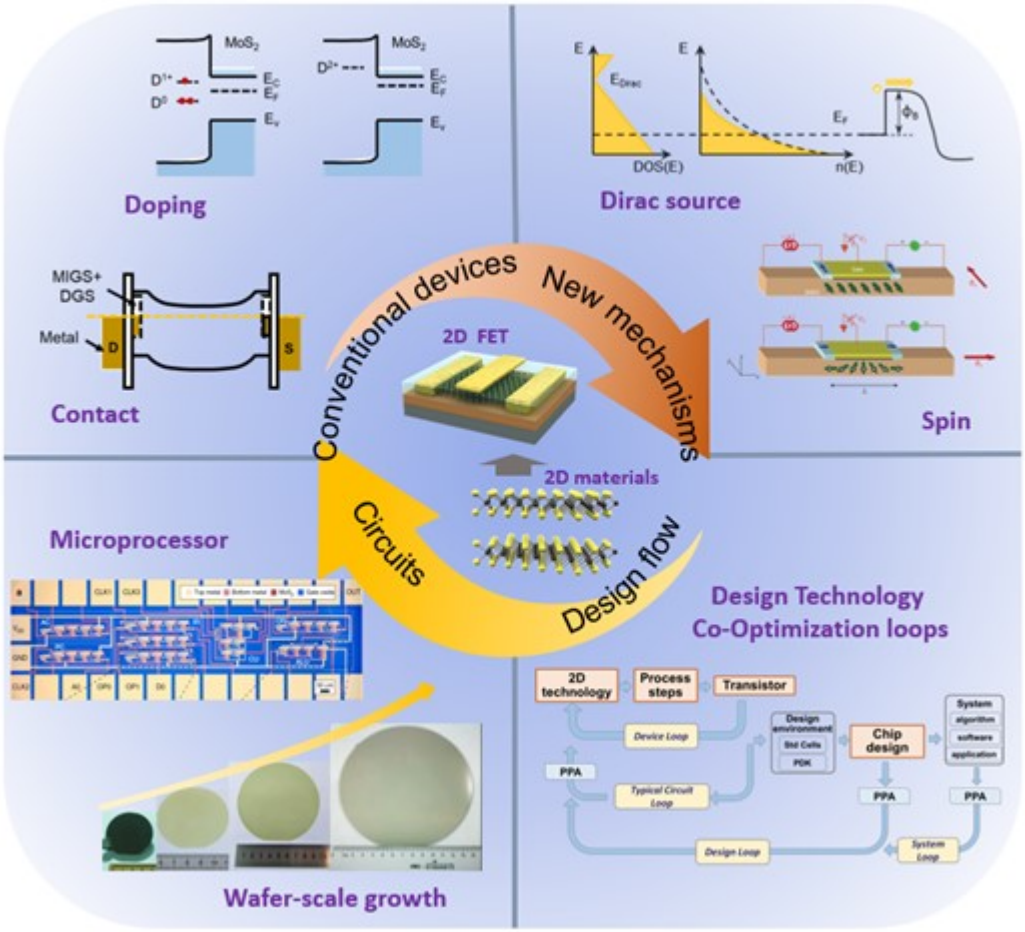


Fig. 1 The main parts of this review on 2D transistors for VLSI, including device engineering, new mechanisms, 2D circuits, and design flow. Adapted with permission [5]. Copyright 2011, Springer Nature. Adapted with permission [22]. Copyright 2009, American Association for the Advancement of Science. Adapted with permission [23]. Copyright 2017, Springer Nature. Adapted with permission [24]. Copyright 2014, American Association for the Advancement of Science. Adapted with permission [25]. Copyright 2017, American Chemical Society. Adapted with permission [26]. Copyright 2020, American Chemical Society. Adapted with permission [27]. Copyright 2019, Wiley-VCH.

2. Material and Device Engineering Toward VLSI

Although 2D materials have impressive electronic properties, some challenges to their use persist from the perspective of device engineering, which is essential for 2D VLSI. Although the intrinsic mobility of TMDCs is expected to be lower than that of bulk silicon, thus constraining the ON current (I_{ON}) [28], the degradation in mobility in ultra-thin silicon is more severe due to the state of the surface trap and dangling bonds. TMDCs have a higher intrinsic mobility than Si at a similar scale. However, short channel effects (SCEs) also emerge in ultra-scaled 2D semiconductor transistors. Uniform, selective, and effective doping techniques are required to tune the device characteristics and enable CMOS circuits. Moreover, metallic contact in 2D materials tends to be resistive. The Schottky barrier is difficult to control owing to gap states induced by defects and the metal. We introduce advanced structures of small 2D transistors here. Recent work on doping and contact is also introduced, following which we briefly generalize the progress in research on 2D ICs.

2.1. Scaling Down Toward Ultra-scaled Size

Since Gordon Moore proposed Moore's law in the 1960s, silicon has been used as the mainstream material to maintain the doubling of the integrated density of logic chips every 18 months or so. This process has led to significant improvements in performance to meet the demands of increasingly complex calculation tasks. More than 10 billion transistors can be integrated into one chip when the process node is scaled down to 5 nm in modern microprocessor chips. This can be mostly attributed to continually improving fabrication processes and advanced device structures. However, as the process node approaches the physical limit of silicon, especially below 5 nm, serious SCEs degrade device performance and the large amount of leaked current increases static power consumption, and can even lead to logic errors. In the past, silicon-based devices have been continually scaled down to ensure high density and good performance while SCEs have become increasingly severe, making it difficult to reduce the rising leakage current. Such structures as the FinFET [29] and gate-all-around FET (GAAFET) [30-31] have been proposed to improve scalability and robustness against SCEs. The laterally stacked GAA structure is expected to enable silicon ICs to even approach the "0.7" nm node by using 12 nm physical gates [32]. Nevertheless, even state-of-the-art silicon-based devices have a limit beyond which such enhancements cannot offset SCEs.

The natural scaling length is $\lambda = \sqrt{T_{ox}T_s\varepsilon_s/\varepsilon_{ox}}$, where T_{ox} and ε_{ox} are the thickness and dielectric constant of the gate insulator, respectively, and T_s and ε_s are those of the channel. It can be inferred that atomic-level thickness and a low dielectric constant (~4 for monolayer MoS_2) can enhance electrostatic controllability, and a sizable bandgap (~2 eV for monolayer MoS_2) ensures low leakage current and a large on/off ratio. More importantly, the reduced degradation in mobility in ultra-thin 2D semiconductors compared with that in silicon highlights the prominent advantage of MoS_2. Further improvements in mobility can be realized by hexagonal boron nitride (h-BN) [33] and Al_2O_3 encapsulation [34] owing to suppressed scattering. These features make 2D MoS_2 a promising candidate for use in

advanced ultra-scaled logic circuits because it can promote the development of "more of Moore." When 3D structures or integration are not considered, the lateral scaling in size determines the final integrated density. For a planar top-gate or back-gate MoS_2 transistor, size scaling can be summarized into two parts: scaling L_g and the channel length (L_{CH}). In 2016, Desai et al. used a single-wall carbon nanotube (SWCNT) as gate to control the bilayer MoS_2 by utilizing the electronic properties of 2D TMDC and the small diameter of the SWCNT [35] (**Fig. 2c**). A transistor with a sub-1 nm gate length has recently been reported with a single layer of graphene that is ~0.34 nm thick (**Fig. 2g**) [36]. This can be regarded as the shortest L_g among the available mainstream materials for the gate, and was obtained by using advanced nanomaterials with a scaled size as the gate. The scaling of L_{CH} is mostly carried out by special processing methods. In 2017, Xie et al. used a lithographic free technique to form a 3.8 nm nanogap in graphene as the channel region in MoS_2 [37]. MoS_2 transistors at the ultimate scale also demonstrate non-negligible drain-induced barrier-lowering (DIBL) [35] and a degradation in the sub-threshold swing (SS) [37-38]. This can be attributed to the lack of control over the planar structure in the form of a top gate or a back gate, as shown in **Figs. 2a**-**b**. A small SS value enables a low operation voltage and a small amount of sub-threshold leakage current, and a poor DIBL degrades the voltage gain of the device and impacts the performance of the circuit. **Fig. 2d** summarizes schemes of single- and double-gate structures that have been reported for 2D materials.

For the above reasons, advanced device structures proposed in silicon-based technology need to be introduced to MoS_2 devices. Since FinFET was first reported in 1998 and adopted in the Intel 22 nm Ivy Bridge processor, it has come to replace conventional planar transistors and become the basic component in mainstream IC manufacturing technology. Advanced 5 nm FinFET technology has been manufactured at a high volume. As predicted in the 2021 International Roadmap for Devices and Systems (IRDS), the GAA transistor will replace FinFET in the 3 nm technology node and will continue to be used in future 1 nm nodes.

Alternatives have been proposed to further enhance the ability of gate control of silicon-based transistors in CMOS technology, and the one of most promising ones is the transistor with a double gate (DGFET), which was proposed by Sekigawa and Hayashi in 1984. 2D-based FinFET [39] and GAAFET [40-42] have also been recently reported for 2D semiconductors, and their atomic-level channel thickness makes them analogous to the 2D DGFET, as shown in **Figs. 2e-f**. Tang et al. assembled an all-2D-based GAA structure with a monolayer MoS_2 as the channel, multilayer graphene as the gate, and h-BN as the dielectric [43]. An ultra-low value of I_{ON} of 100 fA, an I_{ON}/I_{OFF} ratio of up to 10^{10}, and an SS of 100 mV dec^{-1} were achieved owing to the effective double-gate modulation and high-quality contact of graphene. The critical superiority of MoS_2 over bulk silicon lies in the fact that it does not suffer a degradation in mobility in an ultra-thin sub-1 nm layer. A number of theoretical studies have predicted the limit of performance of the 2D DGFET at a sub-3 nm gate length [44-46]. Density function theory and simulations of the non-equilibrium Green's function (DFT-NEGF) have shown that the 2D DGFET is expected to fail to satisfy the low-power application requirements of the ITRS at a 3 nm gate length [46].

3D stacking is a candidate technique for the future beyond the GAA architecture in which transistors are stacked along the vertical direction [47]. A typical case is the complementary field-effect transistor (CFET), in which an n-FET is stacked on a p-FET. IMEC proposed the process for the world's first monolithic CFET device in 2018 [48] and demonstrated it in cell array form appropriate for mass fabrication in 2020 [49]. These architectures can also be applied to 2D semiconductors to enhance performance. In 2020, Huang et al. fabricated a stacked GAAFET based on a bilayer and a monolayer MoS_2 channel with a leakage current of only 6.5% on an Si-stacked nanosheet GAAFET [41, 50]. A stacked GAA MoS_2 transistor with two isolated chemical vapor deposition (CVD)-grown monolayer MoS_2 nanosheets was developed, with a high I_{on} of above 400 μA $μm^{-1}$ at V_{DS}=1 V [51]. The bottom gate (back gate), inner gate, and top gate surrounding the two-stacked MoS_2

nanosheets are deposited or transferred (as the graphene gate) as the control gate for stacked 2D GAA structures, as shown in **Fig. 2h**. These demonstrations exhibit strong drive capability and a largely suppressed off current, because of which higher-level stacking is expected. The CFET is another means of stacking to increase density. A 2D complementary FET with a WSe_2 p-type FET stacked on an MoS_2 n-type FET was fabricated, with footprint half reduced [51] (**Fig. 2i**). A through-layer via (TLV) is generally used to achieve 3D transistor-level stacking in stacked structures [52]. The space between transistors can reach the scale of local inter-connection to greatly improve the efficiency of the transmission lines while reducing delays and power consumption. The challenge for the future is to realize ultra-scaled L_g and L_{CH} in stacking structures in 2D semiconductors in high-density circuits such that the transistor footprint is minimized and performance is optimized.

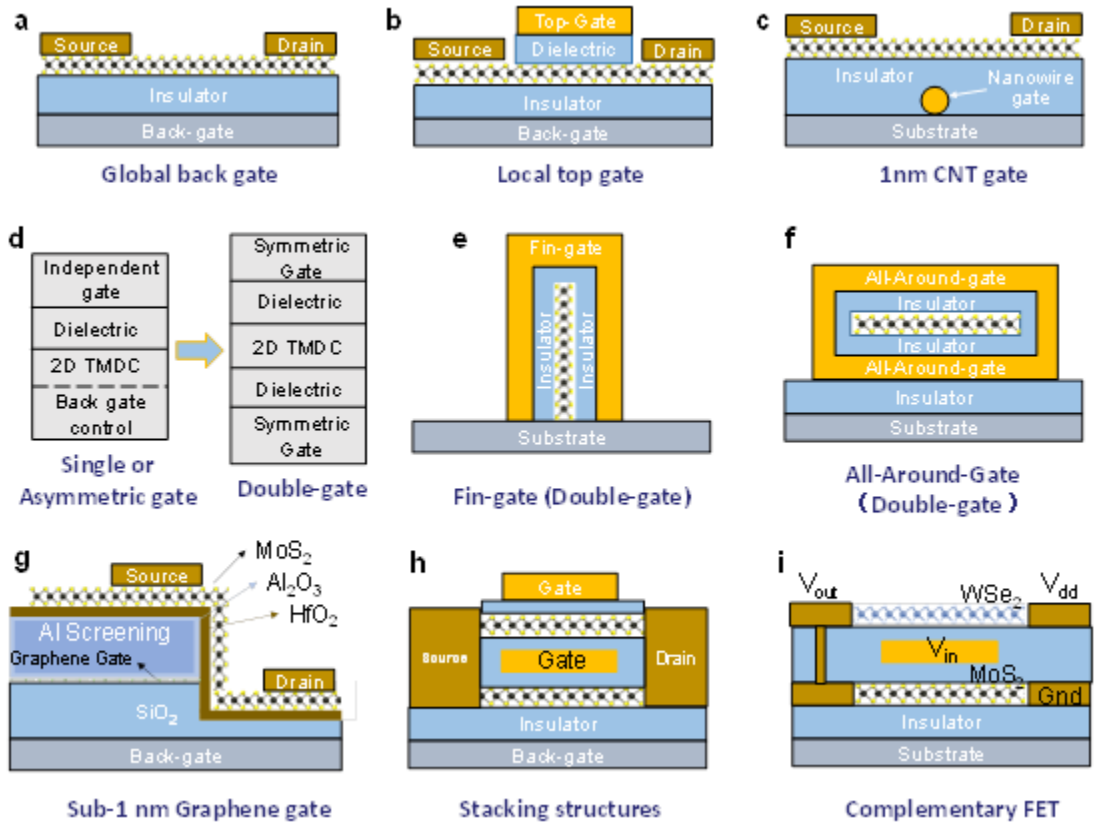


Fig. 2 Typical demonstrations of 2D FET. (a) Global back-gate MoS_2 FET. (b) Local top-gate MoS_2 FET. (c) Buried CNT gate with a diameter of 1 nm [35]. (d) Schematic view to summarize single or asymmetric gate and the DG structure. (e) and (f) MoS_2-based Fin-FET and GAA-FET. (g) Sidewall graphene gate with a sub-1 nm thickness. (h) Two-level stacking nanosheet MoS_2 GAAFET. (i) CFET comprising p-type WSe_2 FET and n-type MoS_2 FET.

2.2. 2D Material Doping

Intrinsic MoS_2 usually exhibits n-type conductance behavior. In some situations, it is necessary to modify the electronic properties of the semiconductor. In bulk silicon material, doping is usually realized by implanted substitutional impurities, which is not suitable for 2D materials. The challenge of doping 2D materials is realizing uniform doping without damaging the lattice. The p-type doping method is important for MoS_2 to realize multiple applications, such as CMOS logic devices using one type of semiconductor without integrating other 2D TMDC materials. Moreover, suitable and selective degenerate doping can decrease the contact resistance, further enhancing drive capability [53]. Finding an effective and controllable way to dope 2D TMDCs is important for controlling the threshold voltage of the channel, enable CMOS, and improve the robustness of the circuit.

2.2.1. Substitutional Doping

Substitutional doping is a typical doping method intensively reported in recent years. Mostly, substitutional doping uses metal atoms. P-type doping is reported to be implemented by introducing p-type dopants, such as Nb substitutional doping [54] or plasma doping [55]. The process can be typically described by CVD growth incorporated with doping atoms. In **Fig. 3a-b**, the schematic processes of substitutional doping in CVD growth are exhibited, including Ni and Re doping in MoS_2, as well as V doping in WSe_2. In the atomic plane of 2D

materials, substitutional doping is thought to be defective, not selective, and challenged by reliability and reproducibility. Plasma doping is reported to enable selective doping but can damage the lattice of 2D materials (**Fig. 3c**).

2.2.2. Interface Charge Transfer Doping

Another effective doping method is charge transfer (CT) from the interface or close to the interface (**Fig. 3d)**. Related reports have examined various 2D materials doped by metal oxides, such as MoO_3 [56-57], TiO_x, and NiO_x [58]. The detailed transfer process is illustrated in **Fig. 3e**. The band alignment between CT layer and 2D semiconductors, and trapping states at the interface, can determine the effects of doping and device performance. This process involves two kinds of situations. First, the charge can be induced by interfacial trap states or border trap states near the interface located in the bandgap of 2D semiconductors. However, the trap states and defects normally cause the material properties to deteriorate, e.g., SS and mobility can be degraded. This may result in a low I_{on} and a low on/off ratio. Second, the carriers transferred from the states are not located in the bandgap states, either in the conduction band or in the valence band (donating electrons or holes), and have no influence on the properties of transport of 2D semiconductors. Early in 2013, Fang et al. reported CT between potassium and WSe_2/MoS_2 to realize degenerate n-doping in the TMDC channel [59]. The n-type doping of MoS_2 by AlO_x [60], its n-type doping by benzyl viologen (BV) [61], p- or n-type doping of WSe_2 by electric double layers [62], p-type doping of WSe_2 by MoO_3 [56], and n-type doping of MoS_2 by amorphous titanium suboxide (ATO) [53] are similar. The capsulation not only has doping effects, but can also induce an enhancement in mobility [53]. The SS and mobility revert to their original values through annealing in ambient N_2 when doping is not applied [60]. The material-selective doping of 2D TMDC by

Al_xO_y has also been demonstrated [63]. However, selective CT doping over a stable region in 2D TMDCs is still lacking.

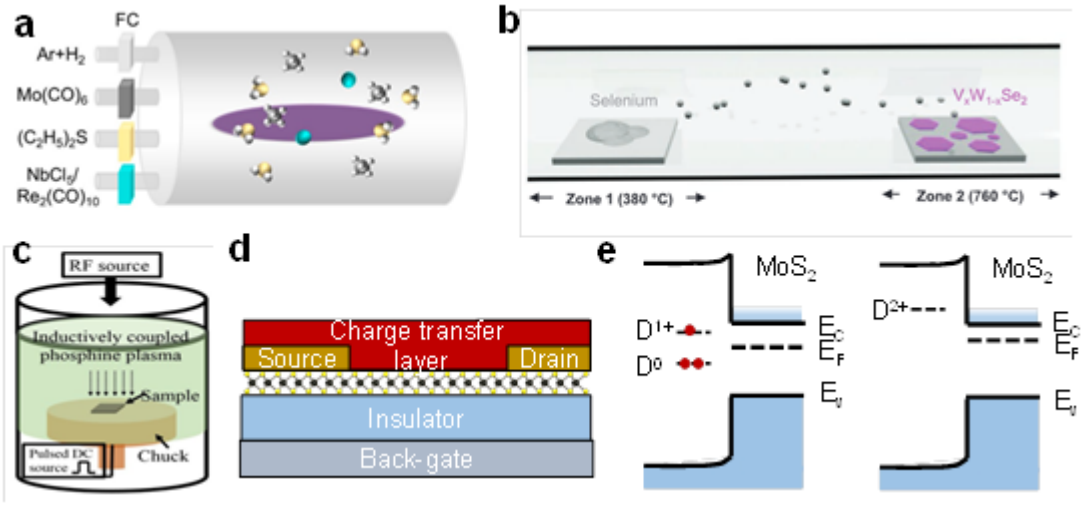


Fig. 3 Typical doping methods for 2D TMDCs. Substitutional doping including (a) Ni and Re doping in MoS_2 via metal organic CVD (MOCVD). Adapted with permission[64]. Copyright 2020, American Chemical Society. (b**)** V doping in WSe_2 via CVD. Adapted with permission[65]. Copyright 2020, Wiley-VCH. (c) P-type doping in MoS_2 via plasma immersion ion implantation. Adapted with permission[55]. Copyright 2016, American Chemical Society. (d) Schematic view of back-gate 2D FET capped with CT layer. (e) Typical band diagram showing the trapping and doping states at AlO_x/MoS_2 interface, where AlO_x is CT layer and D^0, D^{1+}, D^{2+} represents defect with 0, 1, 2 positive charge. The MoS_2 is n-doped after CT from AlO_x[60].

2.3. Contact Engineering

Contact resistance (R_C) is a critical issue in semiconductor technology, and makes it difficult for the device to exhibit intrinsic material properties. A high R_C normally results from a non-negligible height of the Schottky barrier (SB) that can fundamentally impact the

efficiency of charge transport and device performance, typically in the range of 100–400 meV at the metal/MoS_2 interface [66-67]. The SB is often formed between the metal and the semiconductor, and is thought to originate from the energy difference between the work function of the metal and the electron affinity of the semiconductor. However, in some devices based on 2D TMDCs, the SB depends weakly on the work function of the metal [68-72]. It is necessary to tune the height of the SB to reduce R_C, but Fermi-level tunability is often constrained by Fermi-level pinning (FLP). The contact generally suffers from FLP owing to the metal-induced gap states (MIGS) [73] and defect gap states (DGS) [74-75]. MIGS are actually Bloch states in the semiconductor under the influence of the extended wavefunction from the metal [76] while DGS in MoS_2 mostly result from structural defects, such as S vacancies (Sv) and Mo vacancies. The former are dominant owing to the lower formation energy of Sv compared with those of other structural defects [72, 75]. Both hinder contact from approaching the Schottky–Mott limit. A large bandgap of TMDCs makes it challenging to control the height of the SB [77]. Typically, Nb–MoS_2 contact with unsaturated MIGS at the interface induces a strong Schottky junction behavior, as shown in **Fig. 4a**, that significantly impacts device performance. Contact engineering in 2D semiconductors is a major technological issue for these reasons.

The MIGS are formed at the interface when the metal is in direct contact with the semiconductor. One strategy to weaken this interaction is to insert a block layer, such as h-BN [77], to form van der Waals contact. However, this may lead to an enhanced tunneling barrier for Au–MoS_2 van der Waals contact [78]. In case of graphene van der Waals contact, the reduced R_C can be attributed to the clean and defectless surface [79]. Detailed discussions can be found in Refs. [78, 80]. Suitable semi-metal contact can fully saturate the MIGS. Shen et al. used semi-metal bismuth (Bi) contact for 2D MoS_2 materials to achieve ohmic contact with a value of R_C of 123 Ω μm at a carrier density of 1.5×10^{13} cm^{-2}, which is the lowest reported value to date [73] (**Fig. 4b**). The absence of SB was verified by measurements and

attributed to the saturation of MIGS, which was induced by aligning the conduction band of the semiconductor with the Fermi level of Bi and nearly free DOS at the Fermi level of the semi-metal [73]. Bi contact was also shown in an experiment to have significant thermal instability [81]. A melting point of 271.5 ℃ indicates poor compatibility of the back-end-of-line (BEOL) for Bi, whereas Sb (melting point of 630.6 ℃) is more thermally stable, and can achieve a value of R_C as low as 0.66 kΩ μm [81]. Intel has also compared Au, Bi, and Sb in terms of contact with the MoS_2 film, where Sb (Rc = 146 Ω μm) yielded the best results in a BEOL environment [82]. The In/Au alloy can reduce the value of R_C with respect to MoS_2 to 0.19 kΩ μm while improving thermal stability [83].

A number of treatments have been proposed to reduce the Sv to avoid the impacts of DGS, in light of the problem of non-uniformity [84-86]. Forming vdW contact by transferring pre-deposited metal electrodes is an effective strategy for preventing damage-induced gap states and chemical disorders that are generated in the process, such as physical vapor deposition. Liu et al. avoided direct chemical bonding by laminating atomic-level thin films on top of MoS_2 and nearly achieved the Schottky–Mott limit for suppressed FLP [87]. vdW bottom contact has also been recently applied to WSe_2 to enable FL de-pinning [88]. By taking advantage of the de-pinning effect, Wang et al. achieved values of R_C of 800±200 Ω μm and 3000±300 Ω μm for few-layered and monolayer MoS_2, respectively, through vdW contact with In/Au [80]. A chemical method based on oxygen-incorporated CVD has also been shown to suppress DGS and yield improvements in R_C [66] (**Fig. 4c**). DFT calculations were used to show that oxygen at the Sv sites could passivate the Sv-induced donor energy levels [66] to reduce DGS.

Expect for eliminating undesirable SB by supressing the gap states and chemical disorder, introducing other conduction mechanisms can also comprise the lost conductance [89]. Increasing the tunneling current to negate the thermionic emission current is a feasible

way to reduce interfacial resistance in silicon. The tunneling current typically depends on the width of the Schottky barrier while thermionic emission current depends on its height. Therefore, heavily doping the 2D semiconductor can increase the probability of tunneling and provide excess current [90], but 2D materials still face technological challenges. A tunneling layer, such as h-BN, was inserted between TMDC and the metal to suppress the FLP, following which gate tunable p-n and n-p diode behaviors through the channel were demonstrated (**Fig. 4d**) [91].

1D edge contact has been recently reported to be free of the multiple origins of the FLP, and can thus enable nearly ideal contact in 2D TMDCs. Top contact has usually been adopted in the past for ease of fabrication, with the metal electrode located on top of the channel and leading to large values of R_C. Early in 2013, Wang et al. encapsulated graphene with h-BN and effected Cr/Pd/Au contact along the exposed edge to achieve an ultra-low R_C of 100 Ω μm and ballistic transport over 15 μm at low temperature [92]. This can be ascribed to a shorter bonding distance with a larger orbital overlap than surface contact compared with that in case of traditional 2D surface contact. Similar constructions have been applied to MoS_2 to form edge contact and then tune the polarity (p or n type) by changing the work function of the metal to obtain a suppressed FLP [93-94]. A small area of contact of the 1D edge can reduce the density of states and weaken the FLP [93, 95]. However, the use of edge contact on MoS_2 makes it difficult to attain the anticipated reduction in R_C due to the current-crowding effect caused by the long transfer length [93, 96].

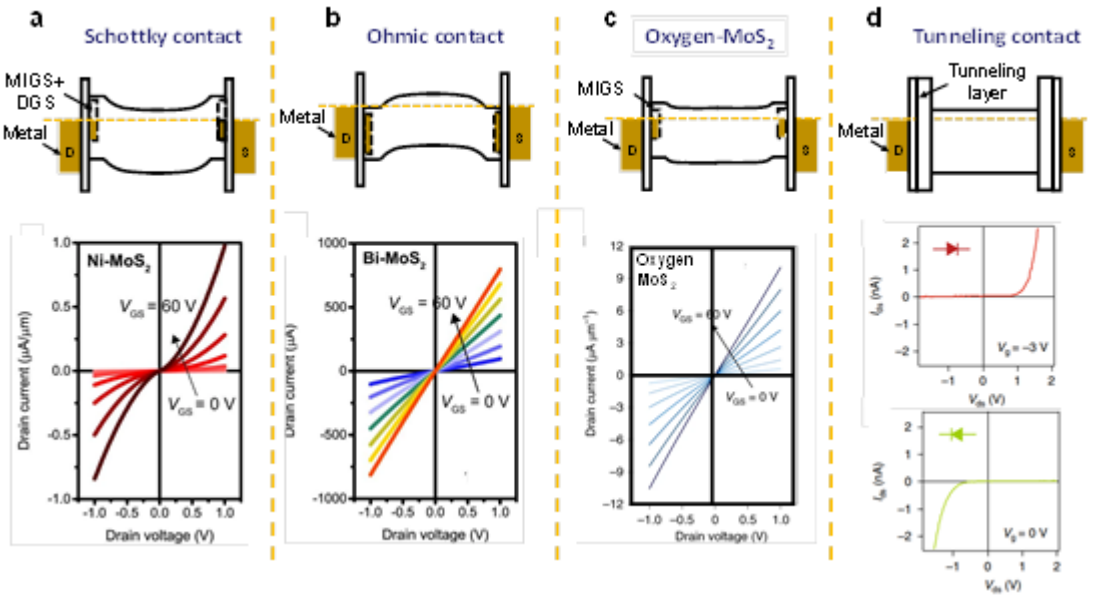


Fig. 4 Band diagrams and output characteristics showing contact behavior for recently reported typical contact engineering demonstrations. (a) The Schottky behavior in case of Ni–MoS_2 contact under the influence of MIGS and DGS, causing severe Fermi-level pinning (FLP). Adapted with permission [73]. Copyright 2021, Springer Nature. (b) Ohmic contact realized by Bi. Adapted with permission [73]. Copyright 2021, Springer Nature. (c) MoS_2 with incorporated oxygen can reduce the DGS at the interface, but with a certain amount of MIGS. Adapted with permission [66]. Copyright 2021, Springer Nature. (d) Tunneling layer-induced gate-tunable diode behavior in case of metal–TMDC contact. Adapted with permission [91]. Copyright 2017, Springer Nature.

3. New Mechanism Beyond CMOS

Fig. 5 shows a diagram of novel devices based on typical 2D materials. The power consumption of modern ICs has an approximate formula of ~V_{DD}^3, where V_{DD} is the supply voltage. A low SS is needed for power scaling. In conventional FETs, the intrinsic limitation on the thermal emission of the carrier keeps the SS above 60 mv dec^{-1}. As the scaling down continues, the performance of the transistor gradually worsens, and a smaller SS is needed to

steadily complete the function of the circuit and meet the demand for low power consumption. Scaling the supply voltage to reduce power consumption requires that the transistor violate the thermionic limit. Continual discoveries and research on novel physical mechanisms can propel 2D materials toward high-performance (HP) and high-density (HD) VLSI applications. Numerous devices beyond CMOS technology have been proposed and investigated, and the tunneling transistor [97-101], ferroelectric transistor [101-107] and nano-electromechanical relay [108-109] are typical among them. For example, a tunneling transistor with a carbon nanotube as channel material yields a value of SS below 40 mv dec^{-1} [97]. In recent years, the Dirac source transistor and filament transistor have emerged as candidates with excellent properties. The goal of these new devices is to improve energy efficiency, density, speed, and functionality. They have led to the development of novel technologies by introducing new physical mechanisms to help improve transistor performance and extend semiconductors to next-generation nodes. However, they all have their respective limitations and face technical problems that need to be solved. For example, the limited on-current hinders the drive capability of the tunneling FET (TFET), and FeFET suffers from a large hysteresis and issues with long-term stability. The spin transistor can enable fast and energy-efficient data processes. This section summarizes the basic working principles of these types of transistors and current drawbacks in 2D VLSI.

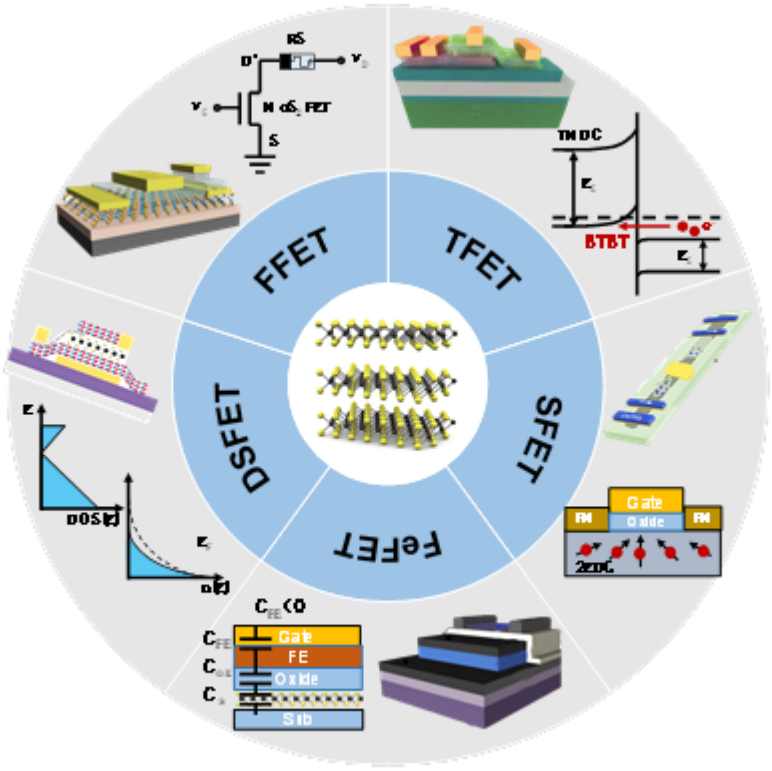


Fig. 5 A diagram summarizing six typical novel devices that offer promise for the use of 2D materials. FeFET: ferroelectric FET. Adapted with permission [106]. Copyright 2021, American Chemical Society. TFET: tunneling FET. Adapted with permission [110]. Copyright 2019, IEEE. DSFET: Dirac source FET. Adapted with permission [40]. Copyright 2021, American Chemical Society. SFET: spin FET. Adapted with permission [111]. Copyright 2017, Springer Nature. FFET: filament FET. Adapted with permission [111]. Copyright 2020, Springer Nature. The insets represent the respective mechanisms introduced to typical 2D transistors.

3.1. 2D Tunneling FET

The TFET is a new device concept that is expected to reduce the operating voltage. In the conventional FET, the values of I_{DS} changes exponentially with V_{GS} based on the thermionic

injection current over the gate-controllable barrier. The conduction of the TFET is governed by the band-to-band tunneling (BTBT) process, which can achieve a sub-thermal SS below the limit of ln(10)kT/q (~60 mV dec^{-1} at 300 K) [99]. The basic mechanism is one where the energy distribution of the carrier at the source is filtered by the energetic window between the valence band maximum of the channel and the conduction band minimum of the source, where the tunneling event is allowed to occur [112]. This mechanism has been used to attain sub-60 mV dec^{-1} for CNT [97] and Si [98], but the low values of I_{ON} and SS make it difficult to sustain this over a sufficiently long span of I_{DS}. 2D vdW heterojunctions (HJs) have recently been regarded as promising candidates for high-performance TFETs owing to their ultra-short tunneling distance and atomically sharp surface [113] as well as a strong gate controllability [114] enabled by van der Waals bonding.

In conventional demonstrations, I_{ON} is constrained by the probability of tunneling . The probability of transmission is given by the Wentzel–Kramer–Brillouin (WKB) approximation:

$$T_{WKB} \approx \exp\left(-\frac{4\lambda\sqrt{2m^{*}E_g^3}}{3e\hbar\left(E_g+\Delta\phi\right)}\right) \#(1)$$

where $\triangle\phi$ is the energetic window, λ is the screening tunneling length, m* is the effective mass of the carrier, and E_g is the bandgap. It can be inferred that a small λ and a narrow bandgap ensure a large I_{ON}.

2D TFETs have been intensively investigated by taking advantage of 2D materials, and include the WSe_2–MoS_2 TFET [112, 114], black phosphorus (BP) TFET [115], BP–MoS_2 [116], and Ge–MoS_2 [113]. The performance of the BTBT has been verified at room temperature in many demonstrations, but few of the relevant studies have been reported to

violate the minimum sub-threshold slope limit. The underlying reasons can be ascribed to the difficulty of forming a suitable dielectric on 2D materials and interfacial contamination between layers [112, 117]. In a 2D HJ TFET, the low SS can also be ensured by BTBT. Taking 2D HJ TFET adoping p-type degenerated $SnSe_2$ as source and WSe_2 as channel for example, thermal emission conduction dominates when negative gate voltage is applied (**Fig. 6a**). In the regime applying little positive gate voltge, the current can be greatly suppressed due to zero tunneling window and high potential barrier hard to overcome for electrons and holes (**Fig. 6b**). Further increasing the gate voltage, WSe_2 is n-type degenerated and its conduction band overlap with the valence band of $SnSe_2$, then BTBT pathway is formed with available DOS in WSe_2, resulting abruptly increased current (**Fig. 6c**).

The switching performance of the 2D TFET is closely related to the quality of the interface and the dielectric on the 2D material. In 2015, Sarkar et al. introduced a liquid ion gate to the Ge–MoS_2 TFET for the first demonstration with sub-thermionic SS over four decades at a supply voltage of 0.1 V [113], with a value of I_{60}/I_{OFF} of ~7×10^3 (I_{60} is the I_{DS} current at an SS of 60 mV dec^{-1}). It was thought that the interfacial layer formed by the oxidation of germanium can limit the probability of tunneling, indicating room for improvement. The BTBT was subsequently verified in 2D–2D HJ TFETs, but without overcoming the SS limit [118-119]. In 2017, a 2D–2D HJ TFET with a sub-thermionic SS of 37 mV dec^{-1} was exhibited with n-type behavior for the first time. It consisted of a p-type layer of $SnSe_2$ and an n-type layer of WSe_2 [120]. A p-type $SnSe_2$–WSe_2 HJ TFET with an SS of 35 mV dec^{-1} was further realized [121]. A p-type WSe_2–MoS_2 HJ TFET with ion gel as the top dielectric also achieved a minimum SS of 36 mV dec^{-1} and an on/off ratio of 10^6 [112]. 2D HJ TFETs still suffer from interface problems. In 2020, a natural HJ BP with layers of varying thicknesses, to avoid interfacial problems among materials, was demonstrated, and achieved a sub-30 mV dec^{-1} both for p- and n-type semiconductors as well as improved performance [115]. However, poor air stability still limits the application of BP. By

transferring 2D materials assisted by polycarbonate (PC) and polydimethylsiloxane (PDMS) on to a defect-free poly methyl methacrylate (PMMA) substrate, Duong et al. achieved an average value of 46 mV dec^{-1} over four decades and a high on/off ratio of ~10^8 with a graphene–hBN–$MoTe_2$ vdW heterostructure (**Figs. 6d–f**) [117]. To meet the demand of state-of-the-art MOSFETs, 2D TFETs still face the challenge of realizing a stable and steep SS over a sufficient number of decades as well as a large drive current.

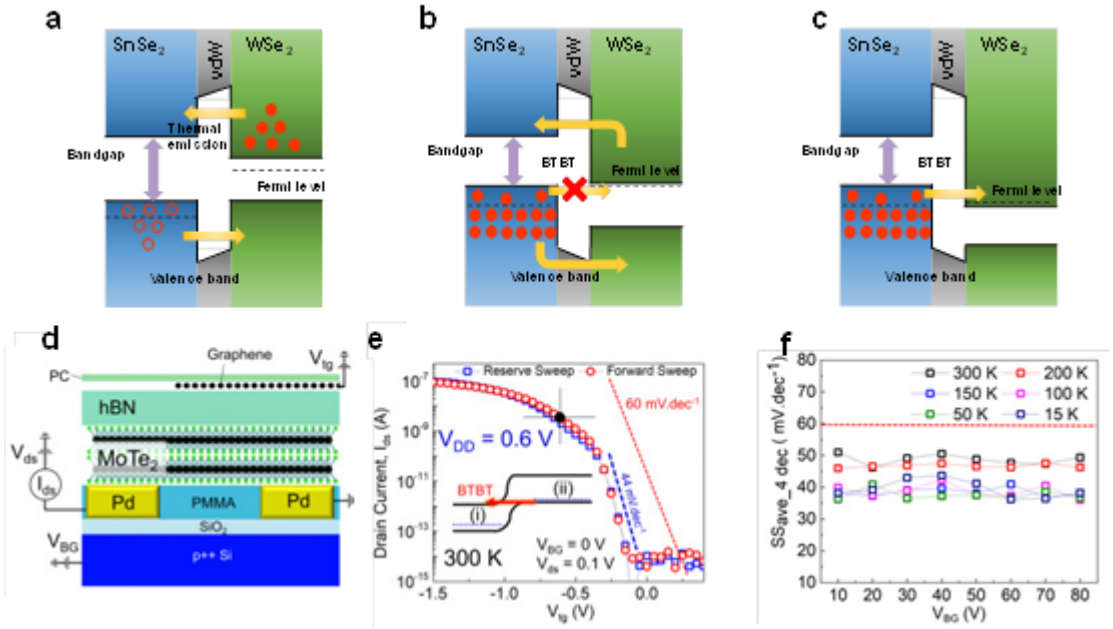


Fig. 6 2D HJ Tunneling transistor (TFET). (a) Band diagram of $SnSe_2$-WSe_2 HJ applying negative gate voltage. (b) Band diagram of $SnSe_2$-WSe_2 HJ TFET at off state applying small positive gate voltage. (c) Band diagram of $SnSe_2$-WSe_2 HJ TFET at on state applying large positive gate voltage. (d) Schematic diagram of graphene-hBN-$MoTe_2$ HJ TFET. Adapted with permission[117]. Copyright 2021, Elsevier. (e) Transfer curves of graphene-hBN-$MoTe_2$ HJ TFET showing sub-thermionic switching. Adapted with permission[117]. Copyright 2021, Elsevier. (f) Average SS over 4 decades

versus V_{BG} of graphene-hBN-$MoTe_2$ HJ TFET at different temperatures. Adapted with permission[117]. Copyright 2021, Elsevier.

3.2. 2D Ferroelectric FET

The SS value refers to the inverse of the change in the drain current (log) that can be obtained for a unit change in the gate voltage. It is a key factor for evaluating the performance of FETs, and is expressed as:

$$\mathrm{SS} = \frac{\partial V_{gs}}{\partial I_g I_{ds}} = \frac{\partial V_{gs}}{\partial \varphi_s}\frac{\partial \varphi_s}{\partial I_g I_{ds}} \#(2)$$

The first term, $\frac{\partial V_{gs}}{\partial \varphi_s}$, is equal to $1 + \frac{C_s}{C_{ins}}$. The second term, $\frac{\partial \varphi_s}{\partial lg I_{ds}}$, can be simplified as $\frac{ln10 \cdot k_B T}{q}$ in the conventional FET structure based on the Boltzmann distribution. At room temperature, the value of the second term was approximately 60 mV dec^{-1}, Equation (1) can be simplified as:

$$SS = \frac{ln10 \cdot k_B T}{q}\left(1 + \frac{C_s}{C_{ins}}\right) \#(3)$$

In the conventional FET structure, both C_s and C_{ins} have positive values. Although some studies have examined engineering C_s and C_{ins}, the SS value remains limited to 60 mV dec^{-1} and cannot be reduced through the scaling down of the CMOS. As a result, the supply voltage (V_{DS}) needed to realize the on-state current cannot be lowered and this leads to severe power consumption problems.

A ferroelectric dielectric has a typical P–E (polarization versus electric field) characteristic. The slope of P versus E, which can be regarded as those of Q (charge) versus V (voltage), is negative around the origin. Thus, the effect of negative capacitance (NC) can be obtained in the ferroelectric insulator [122]. Moreover, higher values of both I_{ON} and low

I_{OFF} can be realized through the use of the NC ferroelectric dielectric in the transistor compared with that in tunneling-based transistors.

A simple gate-ferroelectric dielectric-channel (GFC) stack was first demonstrated to realize sub-60 mV dec^{-1}. If the gate voltage of ferroelectric-based polarization switching corresponds to the region of the sub-threshold of the drain current, the idealized sub-60 mV dec^{-1} at room temperature can be obtained. However, the interface between the ferroelectric as dielectric and the channel is not compatible. This leads to undesirable device performance. A conventional insulator layer with a relatively large positive capacitor was deposited between the ferroelectric dielectric and the channel. The additional capacitor stabilized the ferroelectric in the state of zero polarization [123]. A silicon-based N-FET with a sub-60 mV dec^{-1} was reported by using this gate-ferroelectric dielectric-insulator channel (GFIC) stack structure. The P(VDF-TrFe) polymer acted as the ferroelectric layer. Compared with bulk materials, exfoliated and layered 2D semiconductor materials can achieve ultra-flattened surfaces with fewer dangling bonds, which is a better platform for realizing high-performance negative-capacitance FETs (NCFETs). The first 2D NCFET was also realized by using the P(VDF-TrFe) ferroelectric polymer layer, with MoS_2 as the channel material [123]. But the fabricated device seemed unstable, and lacked dual-sweep I_{DS}–V_{GS} characteristics. 2D NCFETs with stable sub-60 mV dec^{-1} values, a high on/off current ratio, and a smaller I_{DS}–V_{GS} hysteresis were reported by designing C_{FE}–C_{DE} matching [124-126]. Different 2D semiconductors have been demonstrated as channel materials in NCFETs, including p-type WSe_2 (**Figs. 7a–c**) [127], n-type WSe_2 [128], p-type BP [129], and n-type MoS_2 [130]. Basic logic circuit functions, such as inverters, can be experimentally realized in 2D NCFETs as well (**Fig. 7d**) [130]. The low power consumption [130] and short-channel robustness [131] of NCFETs have also been experimentally proven. Some 2D dielectric materials, such as $CuInP_2S_6$, have demonstrated ferroelectric characteristics [132]. $CuInP_2S_6$ has switchable polarization characteristics even down to 4 nm. 2D flexible NCFETs have been realized by

using MoS_2 as the channel, h-BN as the dielectric, and $CuInP_2S_6$ as the ferroelectric [133]. Graphene has also been used to replace the gate metal to realize 2D NCFETs. Some studies have also discussed the feasibility of NCFETs [123, 134].

Apart from the effect of negative capacitance, the hysteretical I_{DS}–V_{GS} characteristics in FeFETs draw attention to their use as memory or artificial devices [135]. Graphene FeFETs as memory devices with PVDF ferroelectric gating were demonstrated early in 2010 [136]. Ferroelectric polarization was realized by symmetrical voltage sweeps. A suitable negative write voltage ($-V_w$) was applied as V_{GS} and the dipole polarization of the ferroelectric was set to Pr to attain the high-resistance state "1." By contrast, a suitable positive write voltage ($+V_w$) applied as V_{GS} can realize the low-resistance state "0." The limited on-off current ratio of zero-bandgap graphene constrains the memory-related performance. With the development of TMDC FETs, TMDC FeFETs were subsequently demonstrated. The polarization process is highly similar to that of an artificial synapse, because of which basic synaptic behavior can be achieved (**Figs. 7e–f**) [137].

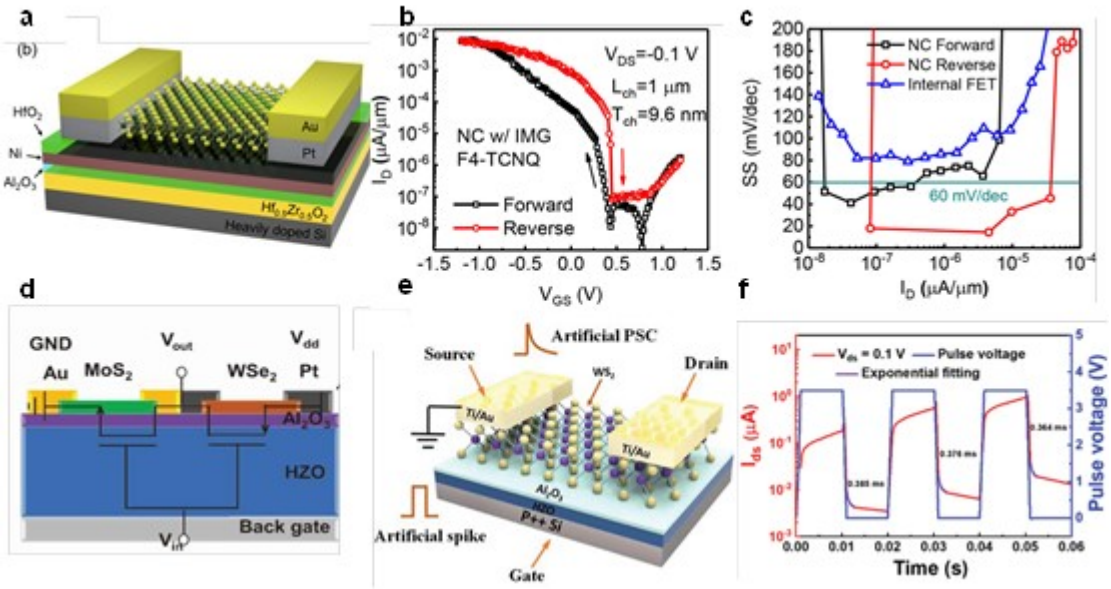


Fig. 7 2D Ferroelectric FETs (FeFETs). (a) Schematic diagram of a p-type WSe_2 FeFET. Adapted with permission [127]. Copyright 2018, American Chemical Society. (b) Dual-sweep transfer curves of the p-type WSe_2 FeFET. Adapted with permission [127]. Copyright 2018, American Chemical Society. (c) SS versus I_{DS} of the p-type WSe_2 FeFET in forward sweep and reverse sweep compared with those in the conventional FET (internal FET). Adapted with permission [127]. Copyright 2018, American Chemical Society. (d) MoS_2 and WSe_2 NCFETs-based inverter structure. Adapted with permission [130]. Copyright 2020, Wiley-VCH. (e) Schematic diagram of 2D HZO/WS_2 synaptic transistor. Adapted with permission [137]. Copyright 2020, Wiley-VCH. (f) Dynamic response showing weight update of the 2D HZO/WS_2 synaptic transistor. Adapted with permission [137]. Copyright 2020, Wiley-VCH.

3.3. 2D Dirac Source FET

The metal source terminal usually has a Boltzmann thermal distribution with an energy tail above the potential barrier in the channel. Except for harnessing tunneling mechanisms with a filtered density of states (DOS), this thermal tail can be suppressed at the source by using Dirac materials with a linear DOS. The thermal injection current enables a more adequate drive capability compared with conventional MOSFETs while ensuring low hysteresis.

Dirac source FET (DSFET) is promising for use as a novel technology. Graphene is usually applied in light of the special DOS distribution of the source materials. In 2018, a graphene source was reported to have yielded excellent switching properties in a p-type carbon-nanotube (CNT) FET with the CNT as channel, with the measured SS overcoming the 60 mV dec^{-1} limit (**Figs. 8a** and **b**) [138]. Its performance was more promising than that of the TFET and NCFET when a significant increase in I_{60} was observed, which implied a high I_{ON} and a low average SS (**Fig. 8c**). Compared with Intel's 14 nm MOSFET, a significantly

improved switching process and comparable I_{ON} were obtained (**Fig. 8d**). A subthermionic SS has also been reported for 2D materials in MoS_2 DSFETs, and the GAA structure can improve performance [40]. The temperature measurements also showed a similar trend to that of MOSFETs, i.e., the SS linearly increased with the temperature. Although few demonstrations have been reported, the promising performance makes them appealing for use in other 2D semiconductors in the future.

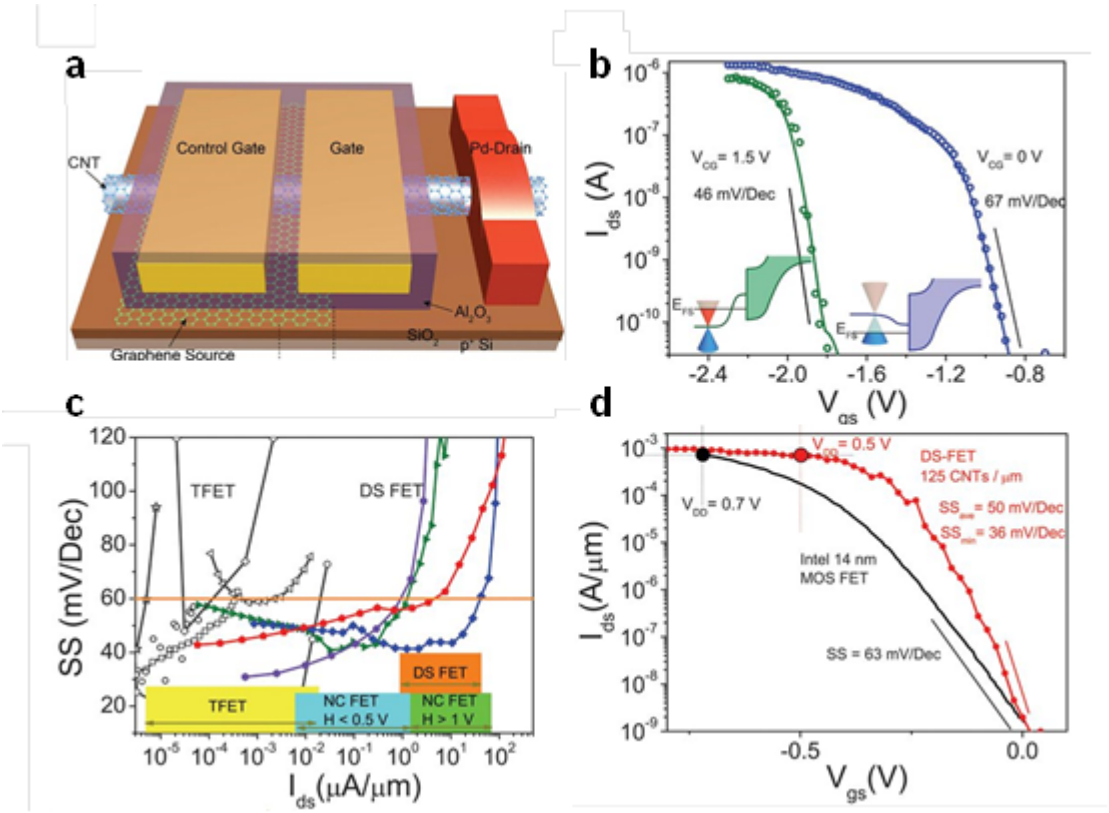


Fig. 8 Graphene/CNT Dirac source FET (DSFET) demonstration compared with other types of transistor. (a) Schematic diagram. Adapted with permission [138]. Copyright 2018, American Association for the Advancement of Science. (b) Transfer curves at V_{CG}=1.5 V and V_{CG}=0 V, V_{CG} is the voltage applied to control gate. Adapted with permission [138]. Copyright 2018, American Association for the Advancement of Science. (c) SS versus I_{DS} compared with those of NCFET and TFET, with a higher I_{60} of the DSFET. Adapted with permission [138]. Copyright 2018, American

Association for the Advancement of Science. (d) Transfer curve of CNT DSFET compared with that of 14 nm Si MOSFET, with a sharper switching of the DSFET. Adapted with permission [138]. Copyright 2018, American Association for the Advancement of Science.

3.4. 2D Filament-based FET (FFET)

Resistive random-access memory (ReRAM) is usually a two-terminal device with a resistive switching layer sandwiched between electrodes. Its simple structure and compatibility with CMOS have led to considerable research on it as a memory unit. Large-scale computing and neutral network circuits have been demonstrated based on it as well [139]. The rupture and formation of the filament in an ReRAM device usually occur abruptly, with a sizable ratio of the on/off current and fast switching [140]. In the FFET, steep current switching is enabled by abrupt filament formation and rupture in the set and reset processes of the ReRAM device, as shown in **Figs. 9a** and **b**. In 2018, Tian et al. proposed an MoS_2 FFET with a graphene–AlO_x–Al ReRAM connected to the drain terminal, and achieved an SS of 4.6 mV dec^{-1}. The forward and reverse sweeping of the gate voltage was at V_{DS}, and led to severe hysteresis as shown in **Fig. 9c** [141]. When a suitable negative or positive voltage was applied to V_{DS}, high resistance "1" and low resistance "0" in the ReRAM device were realized. Further forward/backward sweeping at V_{GS} triggered filament formation/dissolution from the original states to realize ultra-steep slope switching. A similar working mode was adopted in Ref. [142], in which an Ag–HfO_x–MoS_2 ReRAM was used to obtain an I_{DS}–V_{DS} curve with small hysteresis of ~162 mV, as shown in **Fig. 9d**. A hysteresis of ~1 V was also observed at the same V_{DS} [143]. Uniformity and durability are common issues in the ReRAM [140, 144]. The uncertain filament formation/dissolution determines the hysteresis of the FFET as a consequence. Obtaining a stable and uniform switching process is a critical challenge for the FFET.

Resistive switching was very recently introduced to the gate dielectric, with an Ag–PO_x–BP ReRAM integrated on a top-gate MoS_2 FET [145]. A low operating voltage of conducting-bridge random-access memory (CBRAM) was used to obtain sub-1 mV dec^{-1}. The high drive voltage and low I_{ON} still limited its application, and a strong hysteresis was observed [145]. The nearly ideal steep switching in FFETs is appealing but needs to be optimized to achieve the goals of no hysteresis and a high ON.

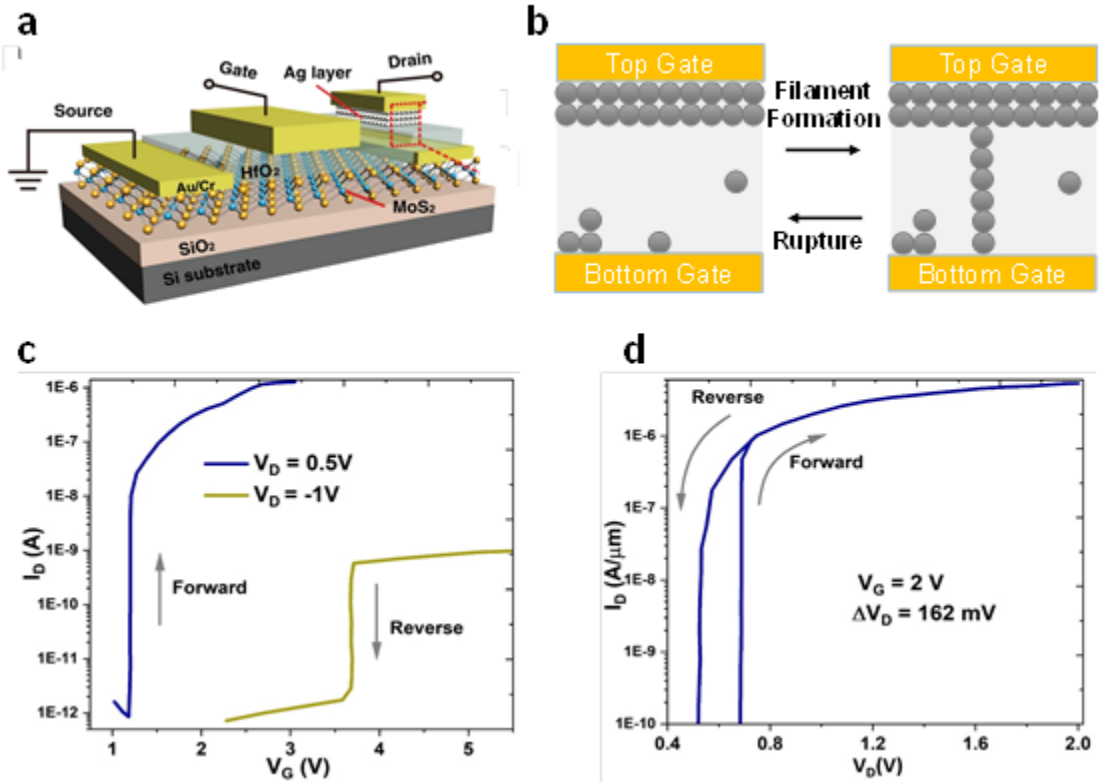


Fig. 9 2D MoS_2 Filament transistor (FFET). (a) Schematic diagram. Adapted with permission [143]. Copyright 2020, Springer Nature. (b) Schematic view of abrupt switching in an RRAM device with filament formation/rupture after applying a set/reset stimulus. (c) Transfer curves in forward and reverse sweep at V_{DS} = 0.5 V and V_{DS} = -1 V. The data are from Ref. [142]. (d) Output curves in forward and reverse sweep at V_{GS} = 2 V. The data are from Ref. [143].

3.5. 2D Spin FET

Since the spin FET was proposed by Datta and Das in 1990 [146], spin devices have been extensively studied due to their potential for faster, more energy-efficient, and non-volatile data storage. 2D materials have been widely studied due to their characteristics of electron transport, structure of the energy band, and other unusual physical phenomena because charge transport is confined to a plane. Spin transistors are also being scaled down and becoming more diverse due to significant advances in the synthesis of 2D materials.

3.5.1. MoS_2 (MX_2) spin transistor

Compared with graphene, TMDCs have a higher spin–orbit coupling (SOC). Such high SOC TMDCs have attracted considerable attention because of their spin dynamics and transport properties. Non-magnetic spin FET and the spin Hall-effect transistor can be fabricated by using TMDCs.

2D non-magnetic spin FETs usually contain six parts: substrate, 2D materials conductive channel, magnetic drain electrodes, magnetic source electrodes, grid electrodes and other materials contacted with the 2D materials conductive channel. When the spin FET operates in the direction of magnetization along the y axis, the magnetic electrodes create binary magnetization (M_y) along the y axis. By applying a external magnetic field along the y axis (B_y) parallel or antiparallel to the directions of electrode magnetizations, spin-dependent voltages can be detected by the detector.

Figs. 10a–c show the traditional structure and properties of non-magnetic spin FETs made of MoS_2. As shown in **Fig. 10a**, the ferromagnetic (FM) drain and source electrodes provide spin-polarized electrons, gate voltage is used for spin–orbit coupling to provide a precession in spin, and MoS_2 provides a suitable environment for sufficient spin–orbit coupling. **Fig. 10b** shows a color scanning electron microscope image of this device. It is

clear that the entire device can be designed to be shorter than 5 μm and thinner than 30 nm. As shown in **Fig. 10c**, this device shows a transistor-like on/off spin signal modulation at room temperature for both magnetization-based alignments [147].

Moreover, a highly quantized conductance can be observed in the non-magnetic spin FET made from MoS_2. Recent research has revealed that the electron spin lifetime of the monolayer MoS_2 can exceed 3 ns at 5 K (two to three orders of magnitude longer than typical exciton recombination times) [148]. The on/off ratio of this device can be as high as 10^8 [149].

The spin Hall-effect transistor is mainly composed of 1T'–MX_2 with M = (W, Mo) and X = (Te, Se, S). **Figs. 10d–f** show a van der Waals heterostructure-based topological field-effect transistor (vdW-TFET) made of a monolayer of TMDC [150]. When various gate voltages are applied, a topological phase transition can be observed in the vdW-TFET (made of 1T'–MX_2). An all-electrical control of the on/off spin conductance can be achieved by applying different gate voltages. In other words, vdW-TFET works by switching the presence/absence of topologically protected conduction channels. It has a minimum horizontal size of ~20 nm. In the context of response time, the electric field-induced topological phase transition can occur very rapidly, at an the timescale of an electronic response [150]. Therefore, the vdW-TFET has significant implications for high-density integration on a chip.

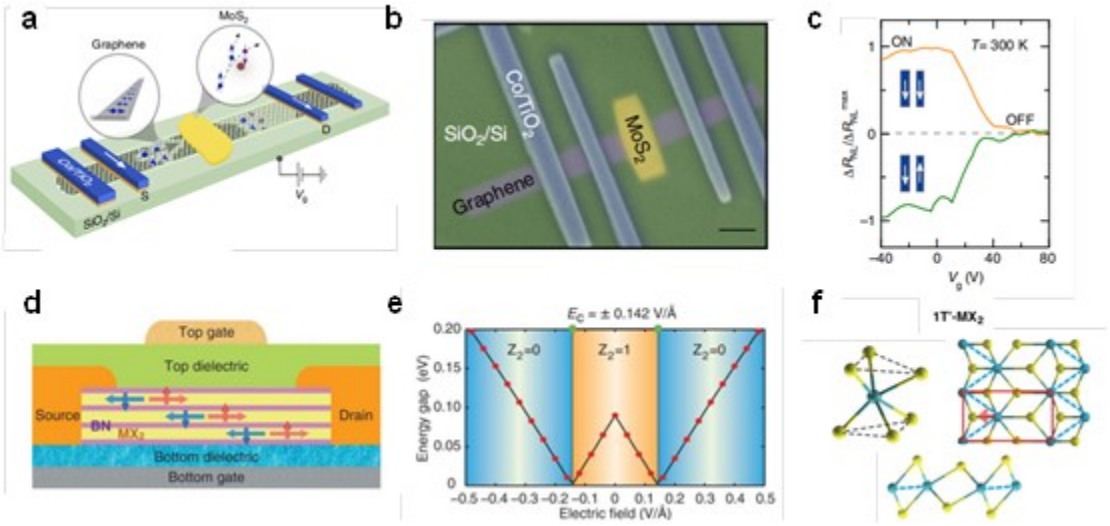


Fig. 10 (a) Schematics of the traditional structure of non-magnetic spin FET made of TMDCs with FM source (S) and drain (D) contacts. Adapted with permission [111]. Copyright 2017, Springer Nature. (b) Color scanning electron microscope image of a fabricated device made of TMDCs with FM tunnel contacts (scale bar is 1 μm). Adapted with permission [111]. Copyright 2017, Springer Nature. (c) Gate dependence of the measured non-local (NL) resistance normalized to the maximum value. Adapted with permission [111]. Copyright 2017, Springer Nature. (d) Schematic of spin Hall-effect transistor. Adapted with permission [150]. Copyright 2014, Science. (e) Topological phase diagram of 1T′–MoS_2 as a function of the vertical electric field. Adapted with permission [150]. Copyright 2014, American Association for the Advancement of Science. (f) Atomistic structures of monolayer transition metal dichalcogenides. MX_2: 1T′–MX_2, distorted 1T–MX_2, where the distorted M atoms form 1D zigzag chains indicated by the dashed blue line. The unit cell is indicated by red rectangles. Adapted with permission [150]. Copyright 2014, American Association for the Advancement of Science.

3.5.2. Phosphorene spin transistor

Since Andre Geim and Konstantin Novoselov stripped graphene from bulk graphite, it has been extensively studied in the contexts of manufacturing, processing, and application owing to its excellent optical, electrical, and mechanical properties. Inspired by the development of graphene, researchers have prepared phosphorene by using the mechanical stripping method and the CVD method. Silicene and phosphorene have been studied extensively because of their potential for use in manufacturing spin transistors.

Figs. 11a–c show a traditional BP spin valve transistor based on the SOC effect. **Fig. 11a** shows an optical image of the BP spin valve transistor. The 2D transistor of this kind is fabricated by fully encapsulating BP with h-BN layers in an inert gas. The electrodes are formed by the deposition of ferromagnetic contacts (Co). The top BN layer is a high-quality tunnel barrier. **Fig. 11b** shows the dependence of the bias current (I_{SD}) on the back-gate voltage (V_{BG}), and the I_{SD}–V_{SD} relation exhibits strong n-type conduction. As shown in **Fig. 11c**, the spin accumulation changes when the directions of magnetization of the ferromagnets are switched. Moreover, a clear signal of spin precession can be observed for both parallel and anti-parallel configurations. The observed RNL is four orders of magnitude higher than that measured in Si. Directional control of the spin current in the phosphorene spin transistor can be achieved by using the large spin signal and spin lifetime. The transistors can be scaled down to 1.4 μm in the length and 10 nm in thickness [151].

Moreover, the phosphorene layer can be made to act as a dilute magnetic semiconductor by doping it with a transition metal [152], as shown in **Fig. 11d**. This phenomenon can be also observed in the transition metal-substituted monolayer of black arsenic–phosphorus (BAsP) [153], as shown in **Fig. 11e**. Based on the spin filter effect, magnetic tunnel junctions made of these kinds of doped materials provide new methods to fabricate the spin TFET. The spin polarization and tunneling magnetoresistance (TMR) of doped BAsP are shown in **Fig. 11f**. Most interestingly, such devices made of several Ni-substituted AsP samples achieve a

100% spin polarization and a tunneling magnetoresistance above 104%, which has been proven to represent the perfect spin filtering effect [152]. Compared with traditional methods for fabricating magnetic materials, these mechanisms for fabricating magnetic semiconductors provide us with new ways to form spin TFETs.

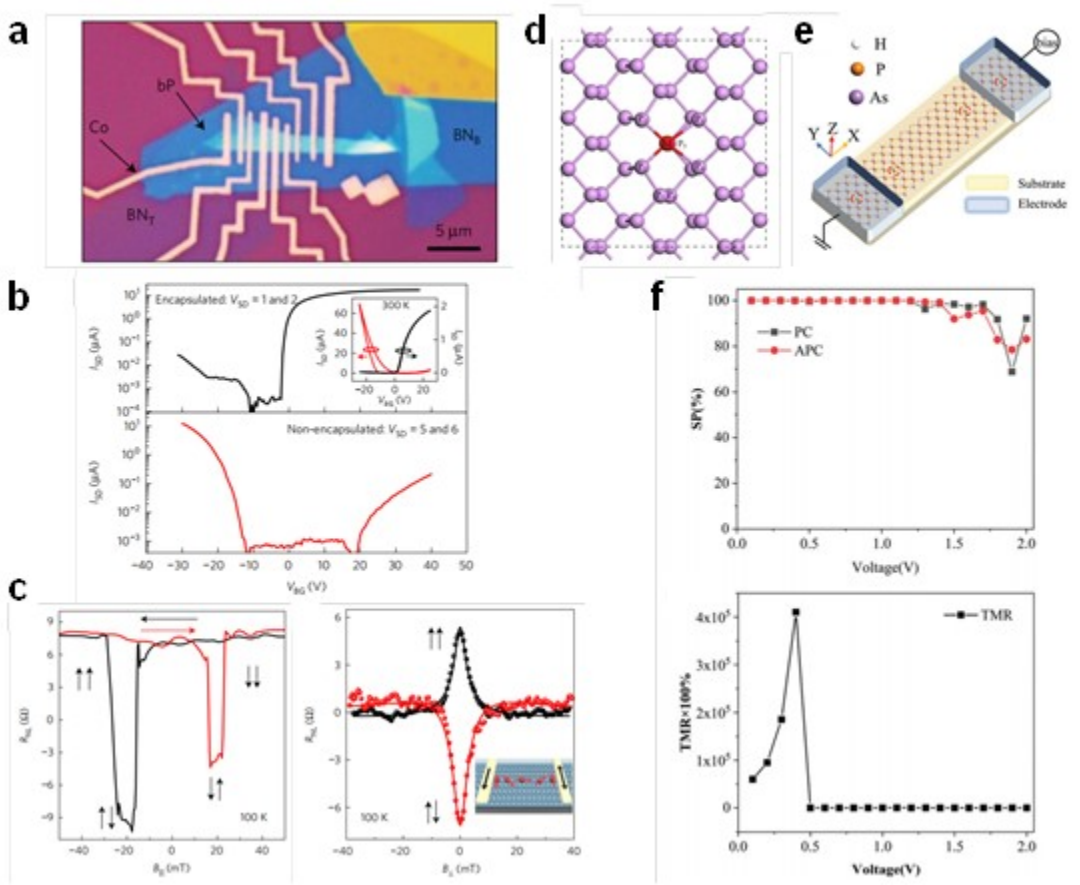


Fig. 11 (a) Optical images of the BP spin valve transistor after the metallization process. Adapted with permission [154]. Copyright 2017, Springer Nature. (b) Back-gate voltage (V_{BG}) dependence of the bias current (I_{SD}) at fixed bias voltages (V_{SD}) of 0.5 V and 0.1 V for encapsulated and non-encapsulated devices, respectively. Adapted with permission [154]. Copyright 2017, Springer Nature. (c) The non-local signal as a function of the in-plane magnetic field. The black and red horizontal arrows represent the directions of sweeping of the magnetic field (left) and the non-local signal as a function of the perpendicular magnetic field (right). Adapted with permission [154].

Copyright 2017, Springer Nature. (d) Schematic illustration of a transition metal-doped phosphorene sheet. Adapted with permission [155]. Copyright 2015, American Chemical Society. (e) A diagram of the spin transistor made of a doped BAsP model with semi-infinite left and right electrodes. Adapted with permission [153]. Copyright 2021, Physical Chemistry Chemical Physics. (f) The spin polarization and TMR curve of doped BAsP. Adapted with permission [153]. Copyright 2021, Physical Chemistry Chemical Physics.

4. Model and Simulation of 2D Semiconductor Devices and VLSI

4.1. Carrier Transport Model of 2D Semiconductors

Drift diffusion is the basic mechanism of carrier transport in semiconductor materials, including 2D semiconductors [156]. A model of drift diffusion is suitable for semiconductor devices with low power density and a large active region. The advantage lies in a faster simulation and a lower computational cost. However, it does not consider some complex physical effects in 2D semiconductor materials, such as quantum confinement effects [157-158], and this leads to a deviation when only the drift diffusion model is applied to a 2D semiconductor material or device. The model thus needs to be calibrated to an advanced physical model in general, as depicted **Fig. 12**, when a faster simulation is desired. Even if the calibrated drift diffusion model is used, some novel physical mechanisms in the 2D semiconductor device still require special attention. Examples include the contact resistor of a metal on graphene or related 2D semiconductor material, and Schottky contact between the metal and the 2D semiconductor, or graphene and a 3D semiconductor [159-162].

Quantum confinement effects play an important role in the performance of devices based on ultra-thin 2D semiconductor materials. In addition to the drift diffusion model, several

sophisticated models, including the semi-class band Boltzmann model, non-equilibrium green function (NEGF) model, and first-principle ab-initio calculation model, have been proposed [163-164] and are shown in **Fig. 12**. From left to right, the models are closer to the physical underlayer of the 2D semiconductor material, and can be used to characterize the device characteristics more precisely. The disadvantages of this technique include a high computing cost, slow simulation, and small device region [162]. The NEGF has been adopted as the standard approach to model non-equilibrium quantum transport in devices with atomic nanostructures [165]. The first-principle ab-initio calculation has been shown to be the most accurate method to assess the quantum confinement effect [157-158, 166]. Density functional theory (DFT)-based NEGF and semi-empirical tight-binding (TB)-based NEGF have been successfully applied to characterize the effect of quantum confinement of 2D semiconductor devices [164, 167], such as transistors based on graphene, WSe_2, and MoS_2 [157-158, 168-170]. A comparative examination of the graphene nanoribbon transistor (GNR-FET) has been reported by combining the extended Huckel theory (EHT) with the TB NEGF [171]. The TB NEGF has also been applied to evaluate the band structure of TMDCs [172] and BP [173], the linear giant stark effect in WSe_2 [174], and chirality in carbon nanotubes [175]. It can capture the lower-energy band structure but encounters some difficulties when reproducing high-energy states. The characteristics of quantum confinement-based transport in novel materials with a single component or a hetero-structure can be calculated based on the DFT or TB NEGF [176-177]. The electrical characteristics of transistors based on WSe_2 and TMDC, such as MoS_2, have been studied using the NEGF–Poisson equation [178].

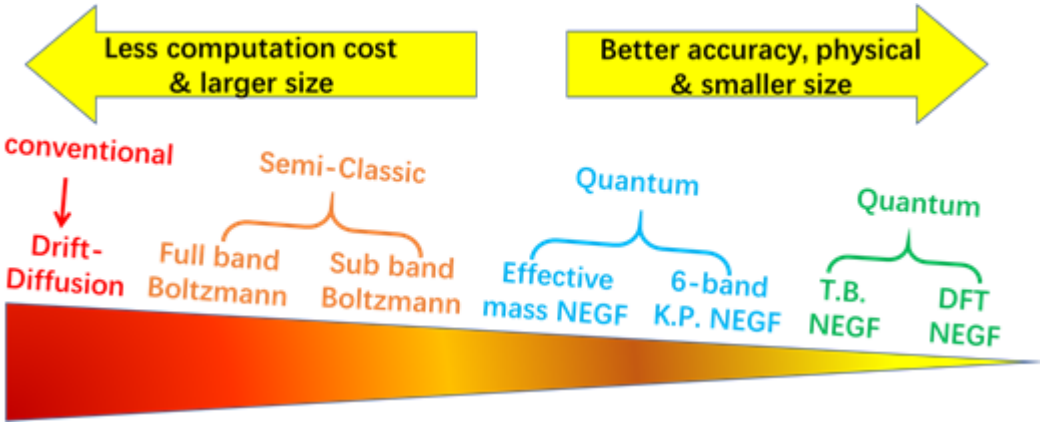


Fig. 12 Physical models of carrier transport in 2D semiconductors.

4.2. Compact Models of Emerging 2D Materials-based Devices

The model for 2D materials is based on the above physical mechanism. The most important part involves modeling the band structures and the density of states (DOS). A signature of Majorana bound states has been identified in 2D material systems with zero-energy modes and peaks in the local DOS [179]. The DOS of 2D semiconductor materials, such as WSe_2, PbI_2, MoS_2, and WS_2, can be obtained by using the BTE and NEGF [179-180]. Quantum effects have a significant impact on the performance of 2D materials, and are considered in most models of 2D semiconductor-based devices [181]. We consider the 2D graphene nanoribbon as an example. Quantum capacitance has been introduced to model the continuous increase in C_{gg} at a high gate voltage in this case [182-184]. Variable-range hopping transport in MoS_2 under contact with a metal has been proposed to characterize the decreased carrier mobility and increased contact resistance R_C [185]. A morphology-based model of 2D materials is another key component. The effect of the grain boundary not only contributes to localized mid-gap states at low temperature, but also to the center of the carrier scatter at a high temperature [186]. The mobility of 2D materials such as

MoS_2 can also be improved by using strain engineering, and this has been modeled as well [187-188].

Another class of physical models for 2D semiconductor devices consists of surface potential-based compact models. The band-tail effect, variable-range hopping transport, saturation of carrier velocity, contact resistance, and trans-capacitance-induced performance have been successfully characterized in compact models of 2D materials-based FETs [189-190]. The voltage-dependent carrier density and temperature- dependent current have been physically predicted by utilizing general percolation theory and the generalized Einstein relation in TMDC FETs [191]. Simulating the device with SPICE is the industry standard for verifying the operation of the circuit at the transistor level. A SPICE model of the TMDC FET allows for the evaluation of transistor- and circuit-level behaviors under variations in the process and different levels of bending [192]. This supports such parameters of transistor design as the width, length, thickness of the oxide layer, various channel materials (for instance, MoS_2 and WSe_2), and the applied strain

4.3 Flow of Simulation of 2D Materials-based VLSI

No mature representation of the flow of the design of 2D materials-based VLSI has been provided thus far. A simulation flow for 2D materials-based VLSI has been proposed by referring to silicon technology [193], as depicted in **Fig. 13**. The performance of the device at the transistor level is first investigated based on the materials and physical mechanisms used, and the SPICE model is then evaluated. For the device loop, the 2D semiconductor material, process flow, and device structure are tuned to obtain the target performance of the transistor in terms of I_{ON}, I_{OFF}, V_{TH}, C_{gg}, g_m, and g_{ds}. The performance of the basic circuit is assessed by directly using a SPICE simulation or a wafer test, and feedback is then provided for device development and fabrication. This completes a typical circuit loop. The layouts of standard

cells are then created and a timing library is executed, followed by the generation of the process design kit (PDK) and the chip design. Power, performance, and area (PPA) are used to evaluate the typical test keys of the circuit, and feedback is provided for the design of the device and the process, i.e., chip/IP design loop. Furthermore, assessment at the software level can be realized by the emulation method based on a hardware prototype with a gate-level delay and parasitic interconnect. The performance and power characteristics of the software/system are fed back to the chip/IP design loop to implement the highest-level system loop.

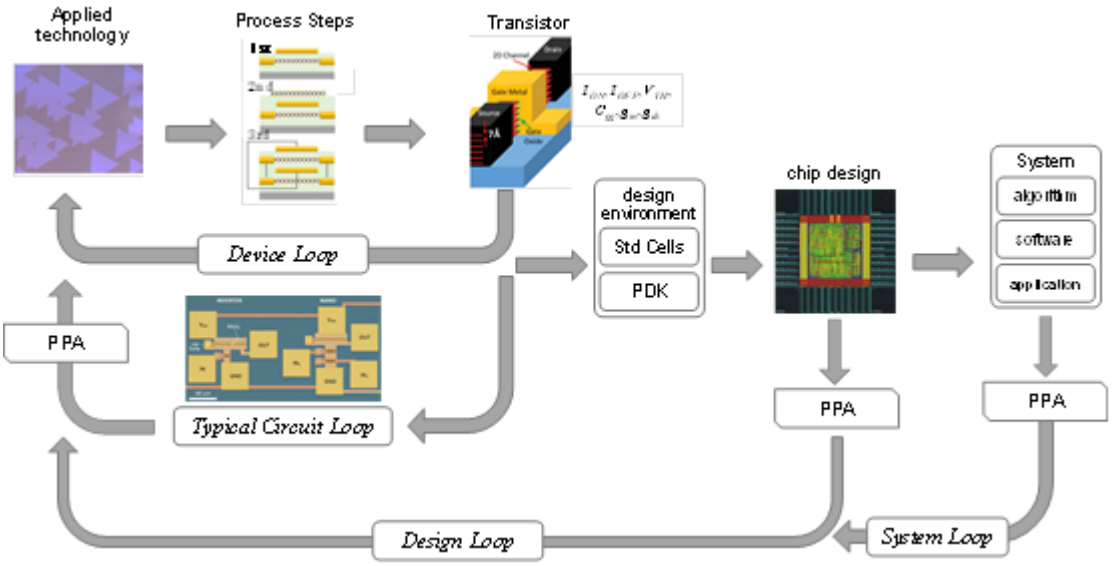


Fig. 13. Proposed design flow for VLSI based on 2D semiconductor.

All or part of the design flow in **Fig. 13** has been used for the assessment or design of novel FETs, including carbon nanotubes and 2D semiconductor materials. The device loop and typical circuit loop can be executed through simulation [194-195]—for example, to optimize such profiles of the device structure as the shape of the channel [196] and source/drain contact on MoS_2 [197]. The impact of different technologies on system performance can be obtained for monolayer black phosphorous- and MoS_2-based FETs, which in turn provides useful feedback for the development of the device and the process technology [198]. There

may be no available compact model for transistors based on 2D semiconductor materials. A kind of Verilog-A look-up table model can be adopted for a SPICE simulation of the device loop and the circuit loop [199-200]. A neural network model can also be used for novel devices based on 2D semiconductor materials [201-202]. The processes of fabrication of 2D semiconductor FETs have a great influence on the performance of the device, and one that was reported based on the mechanical exfoliation method exhibited perfect performance [5, 18, 203]. The synthesis of 2D materials has been widely studied for large-scale fabrication with fine consistence [17, 196, 204]. However, few studies have documented variations or fluctuations in the process that are bound to appear in the fabrication of 2D semiconductor-based transistors. As for the methods in Refs. [205-207], fluctuations in the process of manufacture of 2D semiconductor FETs can be evaluated by using the device and circuit loops shown in **Fig. 13**. A similar design flow was used to manufacture the beyond-silicon microprocessor RV16X-NANO based on complementary carbon nanotube transistors [208]. It overcomes nanoscale imperfections at the macroscopic scale across full wafer substrates. This successful implementation verifies the feasibility of the above design flow, and offers a promising path toward practical 2D semiconductor-based electronic systems.

5. Current Status and Future Development of 2D ICs

5.1. 2D Semiconductors in VLSI

As Moore's Law approaches the physical limit, scaling down silicon-based ICs is no longer sustainable. The channel should be made thin to attain a short length for it, which makes 2D materials irreplaceable. The IRDS 2021 suggested that 2D materials will be used for ultra-low-power applications and memristors for neuromorphic applications [209]. Since graphene was successfully dissociated and 2D materials entered researchers' field of vision,

2D FET-based ICs (2D ICs) have been continually developed. **Fig. 14** show the roadmap of the development of 2D ICs since 2010. The insert pictures are some typical examples in the roadmap. The monolayer MoS_2-based FET was first proposed by Radisavljevic et al., and its inverter consisting of two FETs was subsequently prepared [5, 210]. Wang et al. demonstrated a five-stage ring oscillator based on 12 MoS_2 FET transistors [211]. Zhao et al. reported on the large-scale and spatially controlled synthesis of MoS_2-graphene heterostructures, which were used to assemble into FETs, exhibiting good electrical properties [212]. Subsequently, a major breakthrough was the preparation of a 1-bit microprocessor based on 2D semiconductor, which consists of 115 transistors and constitutes complex circuitry [23]. Recently years, large-scale flexible FET arrays and wafer-scale FET arrays are enabled, and logic functions can be implemented [213-214]. In addition, high-density memristor crossbars based on 2D materials were also realized, used for information storage and neuromorphic computing [215-216]. The number of devices on the panel has increased from one to tens of thousands, and their functions have changed from a single switch circuit to the current inverter, adder, microprocessor, and so on. 2D ICs have thus made great strides, and offer promise for the future.

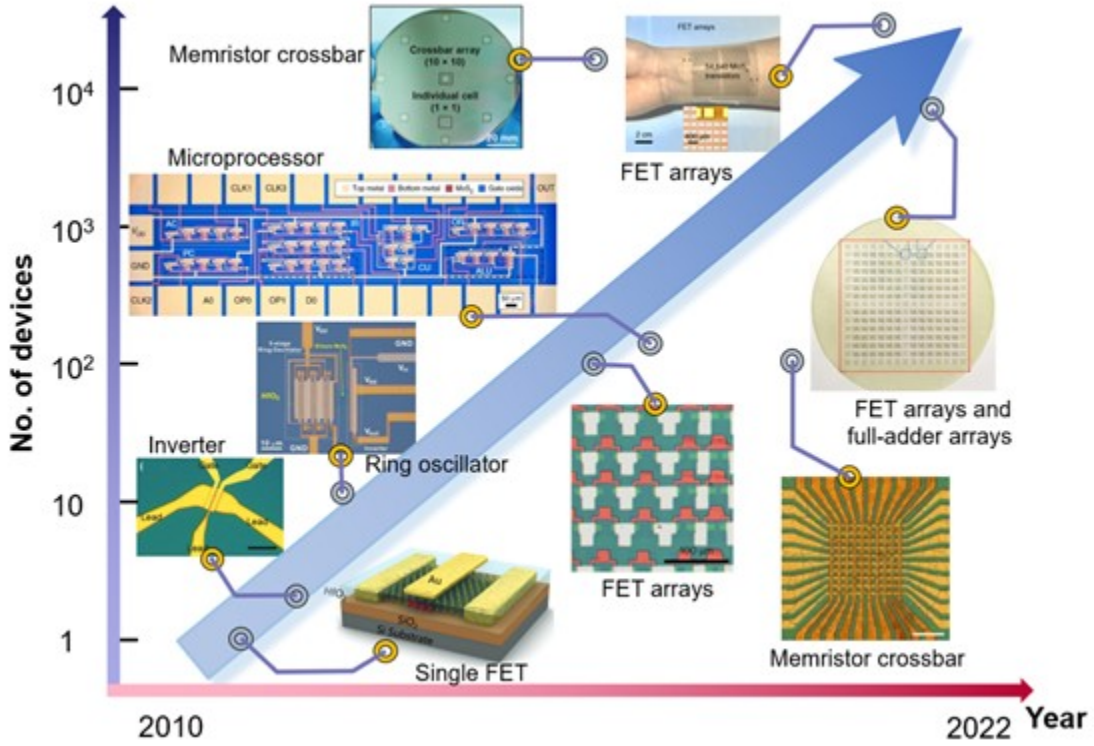


Fig. 14 The roadmap of the development of 2D ICs since 2010. Several typical microscopic images are provided. Adapted with permission [23, 210, 212, 214-219]. Copyright 2011, Springer Nature. Copyright 2011, American Chemical Society. Copyright 2012, American Chemical Society. Copyright 2016, Springer Nature. Copyright 2016, Wiley-VCH. Copyright 2017, Springer Nature. Copyright 2020, Springer Nature. Copyright 2021, Springer Nature.

5.2. Growing Wafer-scale 2D Materials

One of the main obstacles to the application of large-scale 2D ICs is the controlled growth of 2D single-crystal materials, especially their wafer-scale growth. The first exfoliation of graphene and the proof of its stability sparked a boom in the synthesis of 2D materials [220-222]. Methods for the synthesis of 2D materials generally include exfoliation, hydrothermal synthesis, and CVD [223]. CVD is the most promising method for synthesizing

single-crystal 2D semiconductors with a large area for use in ICs. Research on growing large-area or wafer-scale 2D semiconductors has continued unabated since the first synthesis of planar graphene by CVD [224]. Table 1 lists typical reports on the large-scale growth of 2D materials, including graphene, TMDCs, h-BN, and BP. A map of the evolution of the area of growth over the years is also given in **Fig. 15** to clearly show the changes in film size.

Table 1. Summary of large-scale growth of 2D materials.

Material	Method	Substrate	Feature	Grain size/ Film area	Mobility ($cm^2V^{-1}s^{-1}$)	Year
Graphene	CVD	Cu foils	Continuous film	1 cm^2	4050	2009 [225]
	CVD	$Ni/SiO_2/Si$	Continuous film	1 cm^2	3700*	2009 [226]
	LPCVD	Cu foils	SC film	0.5 mm	4000	2011 [227]
	Segregation growth	Metal film	Continuous film	81 cm^2 (4 inch)	\	2011 [228]
	APCVD	Cu foils	SC film	1.2 mm	5000-8000	2013 [229]
	CVD	Cu foils	SC film	1 cm^2	15000-30000	2013 [230]
	LPCVD	Ge/Si	SC film	20.3 cm^2 (2 inch)	7250-10620	2014 [24]
	APCVD	Cu foils	SC film	1 cm^2	\	2015 [231]
	CVD	Cu–Ni	SC film	11.4 cm^2 (1.5	10000-20	2016

		alloys		inch)	000	[232]
	CVD	Cu/sapphire	SC film	81 cm^2 (4 inch)	11000	2017 [233]
	CVD	Cu foils	SC film	250 cm^2	15000	2017 [234]
	CVD	Cu/Ni/sapphire	SC film	182 cm^2 (6 inch)	9700	2019 [27]
	CVD	Ge wafer	SC film	81 cm^2 (4 inch)	26351 ± 4847	2020 [235]
	CVD	Vicinal Ge	SC film	81 cm^2 (4 inch)	43663	2020 [236]
	CVD	Cu foils	SC film	1260 cm^2	68000	2021 [237]
	CVD	Cu/sapphire	SC film	20.3 cm^2 (2 inch)	6600	2022 [238]
MoS_2	CVD	SiO_2/Si	Continuous film	2 mm	0.02	2012 [239]
	Thermolysis process	SiO_2/Si or sapphire	Continuous film	1 cm^2	6	2012 [240]
	APCVD	SiO_2/Si	SC film	123 μm	1-8	2013 [241]
	CVD	SiO_2/Si	Continuous film	1 cm^2	2-7	2014 [242]
	LPCVD	Sapphire	SC film	350 μm	90	2015 [243]
	APCVD	h-BN/SiO_2/	Continuous	1 cm^2	\	2015

		Si	film			[244]
	MOCVD	SiO_2/Si	Continuous film	81 cm^2 (4 inch)	30	2015 [245]
	ALD	SiO_2/Si	Continuous film	81 cm^2 (4 inch)	\	2016 [246]
	CVD	Sapphire	Highly oriented film	20.3 cm^2 (2 inch)	40	2017 [25]
	MBE	h-BN/sapphire	Highly oriented film	20.3 cm^2 (2 inch)	45	2017 [247]
	CVD	Sapphire	Highly oriented film	81 cm^2 (4 inch)	70	2020 [26]
	APCVD	Vicinal Au	SC film	6.45 cm^2	11.2	2020 [248]
	CVD	Au film	SC film	20.3 cm^2 (2 inch)	\	2021 [249]
	CVD	Sapphire	Continuous film	20.3 cm^2 (2 inch)	0.1-1	2021 [250]
	LPCVD	Sapphire	SC film	20.3 cm^2 (2 inch)	102.6	2021 [251]
WSe_2	APCVD	Au foils	SC film	930 μm	143	2017 [252]
WS_2	MOCVD	SiO_2/Si	Continuous film	81 cm^2 (4 inch)	18	2015 [245]
	APCVD	Au foils	SC film	400 μm	1.7	2015

						[253]
$MoSe_2$	APCVD	Molten glass	SC film	2.5 mm	95	2017 [254]
$MoTe_2$	Seeded 2D epitaxy	SiO_2/Si	SC film	5 cm^2 (1 inch)	45	2021 [255]
BP	PLD	Mica	SC film	1 cm^2	213-617	2021 [256]
h-BN	CVD	SiO_2/Si	SC film	9 cm^2	\	2018 [257]
	LPCVD	Cu foils	SC film	100 cm^2	\	2019 [258]
	CVD	Cu/sapphire	SC film	20.3 cm^2 (2 inch)	\	2020 [259]

APCVD, ambient-pressure CVD; LPCVD, low-pressure CVD; MOCVD, metal–organic CVD; ALD, atomic layer deposition; MBE, molecular beam epitaxy; PLD, pulsed laser deposition; SC, single crystal. The mobility with an asterisk is at a low temperature and the rest are room-temperature data.

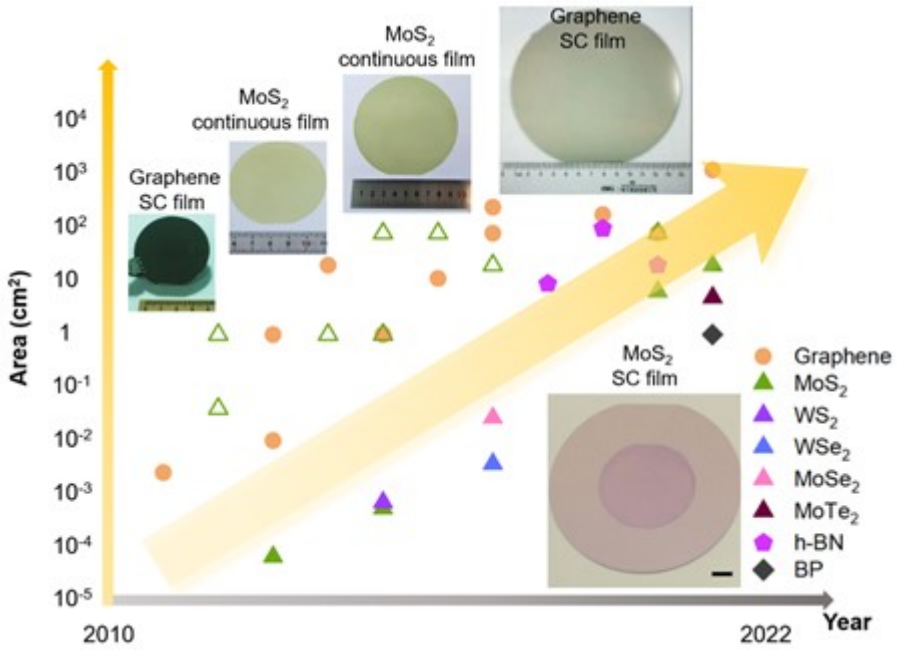


Fig. 15 Evolution in the area of growth of 2D materials since 2010. The solid shapes represent single crystals and the hollow shapes are continuous polycrystalline films. The inserts are demonstrations of several typical wafer-scale growths. SC denotes a single crystal. Adapted with permission [24-27, 251]. Copyright 2014, American Association for the Advancement of Science. Copyright 2017, American Chemical Society. Copyright 2020, American Chemical Society. Copyright 2019, Wiley-VCH. Copyright 2021, Springer Nature.

For graphene, as early as 2009, Li and Kim et al. grew large-area high-quality continuous films over 1 cm^2 using the CVD method on Cu foils and Ni layers, respectively [260-261]. The growth of centimeter-level single-crystal graphene was achieved by Hao et al. in 2013 [230]. Due to the realization of the large-area single-crystal growth of graphene, its mobility has also been improved by leaps and bounds, as shown in Table 1. In 2014, 2-inch wafer-scale single-crystal graphene was grown on Ge surface via low-pressure CVD for the first time [24], thereby enabling wafer-scale single-crystal growth of graphene. In recent years, multiple research groups have reported the growth of wafer-scale graphene single crystals. Zhang et al. proposed a new approach for the growth using Cu/Ni/sapphire wafers at

low temperature, and fabricated 6-inch single-crystal graphene [27]. In order to avoid the use of Cu and Cu-Ni alloy, better matching the IC technology, Di et al. went on to develop the growth of wafer-scale graphene on Ge substrate [235-236]. This year, epitaxial growth of wafer-scale single-crystal graphene on the sapphire substrate was achieved through multi-cycle plasma etching-assisted-CVD [238].

In contrast, large-scale single-crystal growth of TMDCs is much more difficult due to the presence of many random domain orientations. Since 2010, researchers dedicated to increasing the size of single-crystal domains from tens of microns to millimeters, or improving the crystal orientation to obtain large-area highly oriented continuous films [25-26, 239, 242-243, 245, 250, 252-253, 262]. For example, Gao et al. reported the WS_2 single-crystal domain growth up to 400 μm on Au by ambient-pressure CVD [253]. Wang et al. fabricated a 4-inch monolayer MoS_2 wafer with highly oriented and large domains on sapphire, which exhibits good electronic quality [26]. Li et al. prepared wafer-scale (2-inch) polycrystalline $HfSe_2$ by molecular beam epitaxy, and the corresponding memristor crossbar array based on $HfSe_2$ is implemented [262]. It was only in recent years that centimeter-scale single-crystal TMDCs were successfully grown [248-249, 251, 255]. In 2020, Yang et al. reported the epitaxial growth of 1-inch single-crystal MoS_2 on vicinal Au(111). The step edge of Au(111) enables MoS_2 domains to nucleate and grow along one direction, and eventually merge into single-crystal films [248]. Li et al. designed a miscut orientation towards the A axis of sapphire, and prepared a 2-inch single-crystal MoS_2 wafer through epitaxial growth on the sapphire [251]. Wafer-scale single-crystal $MoTe_2$ was also synthesized through seeded 2D epitaxial growth [255].

Insulating h-BN is an excellent dielectric material, which has great potential in 2D ICs. Due to the excessive nucleation and the threefold symmetry of the h-BN lattice, its large-area single-crystal growth is also difficult. Until recent years, large-scale or wafer-level

single-crystal h-BN was successfully prepared [257-259]. The controllable large-scale growth of single-crystal BP films has been a long-standing problem due to its rigorous growth conditions. In 2021, Wu et al. reported large-scale growth of few-layer BP with a centimeter scale through pulsed laser deposition[256]. These show that the wafer-scale growth of 2D materials has made great progress, laying the foundation for the fabrication of large-scale 2D ICs in the future.

5.3. Current development of 2D ICs

As mentioned in section I, 2D materials are promising materials for the next-generation ICs. Especially, graphene is a good candidate for future high-speed electronics and radio-frequency (RF) applications because of its high carrier mobility and saturation velocity [263]. In 2010, Lin et al. fabricated arrays of top-gated graphene FETs with various gate lengths, finding that the highest cutoff frequency reach 100 GHz [264]. Subsequently, they designed a wafer-scale graphene IC with a graphene FET and inductors, which operates as a broadband RF mixer at frequencies up to 10 GHz and possesses outstanding thermal stability between 300 K and 400 K [263]. In 2012, Cheng et al. achieved scalable fabrication of self-aligned graphene transistors as shown in **Fig. 16a**, which brings the intrinsic cutoff frequency up to a recorded 427 GHz [265]. Taking advantage of CVD growth technology and relying on the high-frequency properties of graphene, high-performance three-stage graphene RF receiver IC was fabricated by Han et al. The IC was composed of four inductors, two resistors, and three graphene FETs, performing signal amplification, filtering and down-conversion mixing, which is shown in **Fig. 16b** [266]. In addition, graphene can be used as a photodetector, integrated into CMOS circuits, working as a broadband image sensor, and becoming a digital camera, which is sensitive to ultraviolet, visible, and infrared light [267].

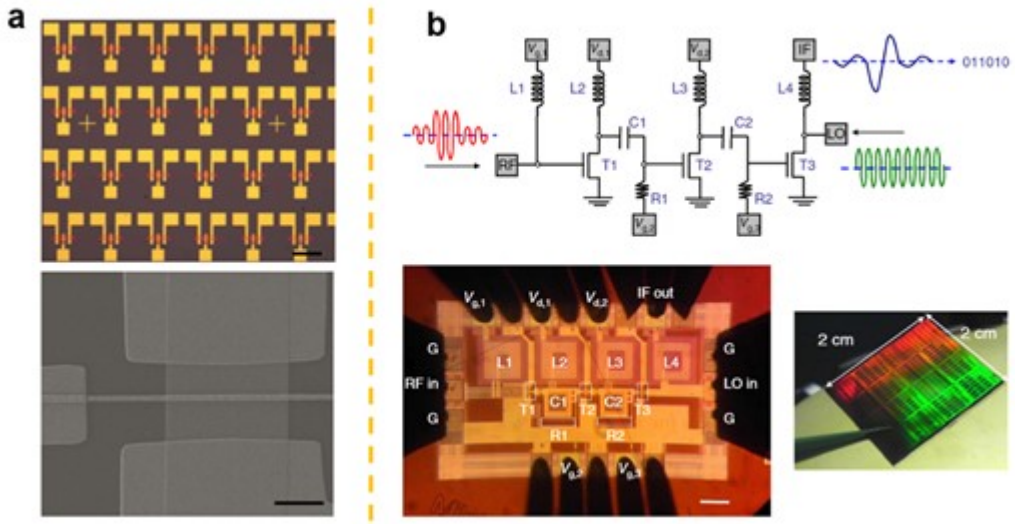


Fig. 16 Two examples of graphene ICs for RF application. (a) Optical and SEM image of graphene transistors with high cutoff frequency up to 427 GHz. Adapted with permission [265]. Copyright 2012, Proceedings of the National Academy of Sciences of the United States of America. The scale bar of the upper panel and the lower panels are 100 μm and 2 μm, respectively. (b) Circuit schematic, optical micrograph, and photo of graphene RF receiver IC, in turn. The scale bar of the second subfigure is 100 μm. Adapted with permission [266]. Copyright 2014, Springer Nature.

Compared to graphene, there are more reports on TMDCs based ICs, especially MoS_2. In 2012, Wang et al. realized fully integrated multistage logic circuits based on few-layer MoS_2 FET operating as an inverter, a NAND gate, a static random access memory, and a five-stage ring oscillator with 2 to 12 transistors [211]. In 2017, Wachter et al. proposed a 1-bit implementation of a microprocessor with 115 MoS_2 FET, but the overall yield was not ideal with only a few percent of fully functional devices [268]. In contrast, the yield of discrete devices is significantly better. Lin et al. fabricated the FETs using liquid-phase exfoliation MoS_2 and achieved a yield of ~95%, which was used to make NOT, AND, NAND, NOR, and XOR logic gates, as well as a half-adder [269]. Furthermore, in 2020, Li et al. prepared a higher device density with 1518 transistors per cm^2 based on MoS_2 FET and achieved a yield of ~97%, as shown in **Fig. 17a**. The created ICs possess flexibility, realizing functions

including inverters, NOR gates, NAND gates, AND gates, static random-access memories, and five-stage ring oscillators. To date, wafer-scale 2D ICs fabrication guided by machine-learning (ML) algorithms was proposed by Chen et al., improving manufacturing efficiency and taking an important step towards future industrialization. **Fig. 17b** exhibits the wafer-scale ICs based on MoS_2 FET fabricated by ML optimized. The average mobility and VT values of individual FET are 46.7 cm^2 V^{-1} s^{-1} and 1.9 V, respectively. For the functional circuits of 1-bit full-adder, the yield reaches ~50% [213]. Besides MoS_2, other TMDCs also have great potential in 2D ICs. For example, WSe_2 FET can be used to make an image processing array based on its multiple logic functions. At the same processing power, the transistor consumption of the image processing array is less than 16% of the traditional circuits [270]. In addition, TMDCs can be prepared to backplane thin film transistors (TFTs) for the large-area displays and sensors. For examples, Park et al. demonstrated large-area and flexible tactile sensors based on MoS_2 back-plane TFTs arrays, which offers a wide sensing range (1−120 kPa), sensitivity value ($\Delta R/R_0$: 0.011 kPa^{-1}), and response time (180 ms) with excellent linearity [271]. Choi et al. reported a flexible OLED display driven by an active matrix backplane circuit based on a large-area MoS_2 TFT [272].

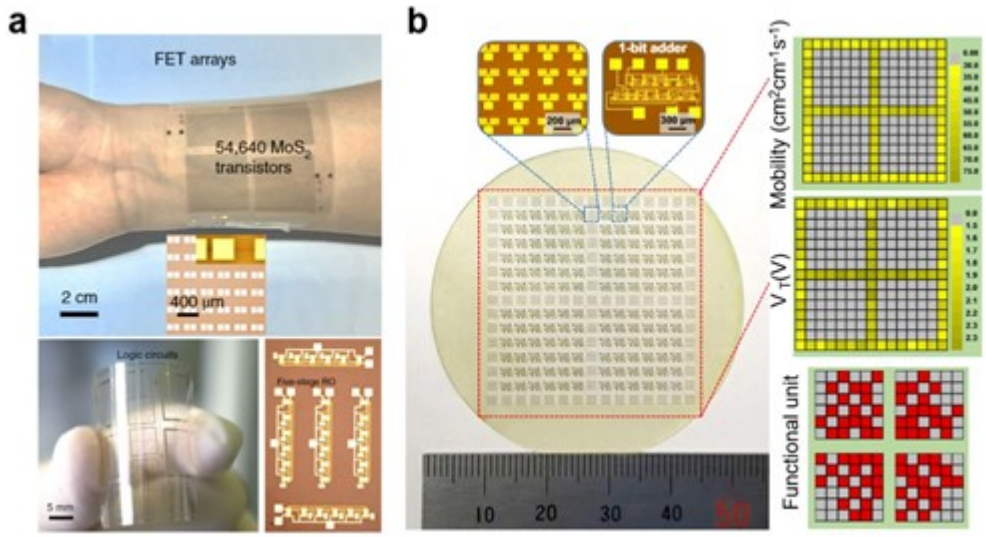


Fig. 17 Two examples of wafer-scale MoS_2 ICs for logic gate application. (a) Photograph and micrograph of integrated MoS_2 functional circuits on a flexible substrate. Adapted with permission [273] Copyright 2021, Springer Nature. (b) Photograph of a 2-inch MoS_2 wafer with 1-bit full-adder arrays and FET arrays. The statistics of mobility, threshold voltage (V_T), and yield are given on the right. Adapted with permission [274]. Copyright 2020, Springer Nature.

Compared with traditional silicon-based transistors, the mobility of MoS_2 FET is particularly insufficient in modern ICs. Thus, other materials were developed to try to make FETs. BP is one of them. In 2014, BP FET was successfully fabricated and obtained ultra-high mobility up to ~1000 $cm^2 V^{-1} s^{-1}$ at room temperature [275]. Proper doping can transform the conductivity of BP from p-type to n-type. Based on this, Liu et al. fabricated monolithically BP complementary inverter circuits with a switching frequency up to 100 kHz and remarkable electrical stability upon mechanical bending. Also, Chen et al. obtained n-type BP FET via Al doping and achieved a complementary inverter logic circuit shown in **Fig. 18a**. A three-stage ring oscillator modeled based on the BP inverter showed low propagation delay per stage [276-277]. However, as far as we know, large-scale BP-based ICs have not yet been realized, which may be due to the instability of BP in the air, resulting in the need for dense encapsulation of fabricated circuits.

Limited by the instability of BP in air, some new air-stable 2D materials possessing high mobility are developed, such as Bi_2O_2Se. The Hall mobility of pristine Bi_2O_2Se is up to 20000 $cm^2 V^{-1} s^{-1}$, and the fabricated top-gate FET based on Bi_2O_2Se exhibited high mobility of 450 $cm^2 V^{-1} s^{-1}$, large on-off ratio, and near-ideal subthreshold swing values [278]. Subsequently, the wafer-scale single-crystal Bi_2O_2Se film was synthesized by CVD, and Bi_2O_2Se based inverter and integrated logic devices were constructed [279-281]. The Bi_2O_2Se based FET and integrated devices are shown in **Fig. 18b-c**.

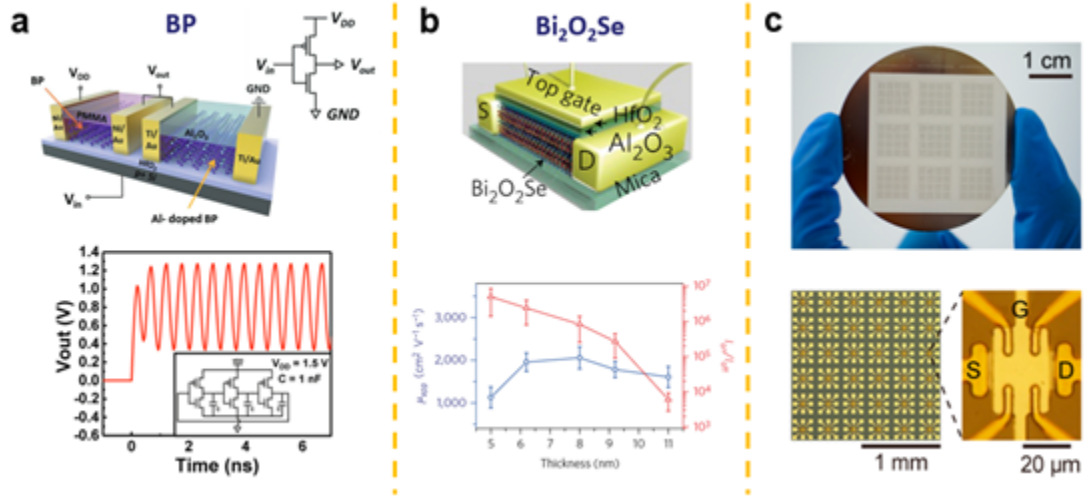


Fig. 18 Examples of BP and Bi_2O_2Se ICs for logic gate application. (a) Schematic structure of the BP complementary inverter and simulated output characteristics of a BP three-stage oscillator. Adapted with permission [276]. Copyright 2018, Wiley-VCH. (b) Bi_2O_2Se -channel FETs with high mobility and large on/off ratio. Adapted with permission [278]. Copyright 2017, Springer Nature. (c) The exhibition of wafer-scale Bi_2O_2Se discrete FET at different scales. Adapted with permission [281]. Copyright 2019, American Chemical Society.

5.4. Challenges for the future development

5.4.1 The growth of the 2D materials

Even though many 2D materials can be grown into large-area single crystals, it has to be admitted that it is very difficult to avoid defects, impurities, and grain boundaries during the growth process. The defects, impurities, grain boundaries, even though the wrinkles and thickness fluctuations have a great impact on the performance of the 2D devices. At present, reproducible preparation of uniform large-area single-crystal 2D materials remains a challenge. Moreover, the realization of most current 2D ICs relies on the transfer of 2D

materials to the target substrate, which may cause secondary damage to the materials. The direct growth of 2D materials on the circuit substrate is a promising route to improve the reliability of the devices. This also brings about the challenge of the thermal budget. For example, the growth of crystalline 2D materials by CVD usually requires a high temperature above 900℃, but this temperature has exceeded the temperature of front-end-of-line (FEOL) and BEOL processes of ~450 ℃ [282]. This requires a completely new process line for the manufacture of 2D ICs, which is different from the traditional silicon-based process. Therefore, there is still room for improving the growth of 2D film used in wafer-scale 2D ICs.

5.4.2 Contact engineering

The electrical properties of 2D FET are strongly limited by the contact resistance between the metal electrode and the 2D channel, especially when the device enters the nanoscale [283]. Optimizing the contact of 3D metals with 2D materials is a very important technical challenge. For an individual device, besides choosing a suitable semi-metallic contact electrode, such as Bi, to suppress the MIGS, mentioned above, there are some solutions worth considering to reduce contact resistance. 1) Compared to traditional metal/semimetal contact, 2D family (such as graphene) is preferred to achieve low contact resistance, and can be used to realize purely 2D circuits. 2) Edge contact instead of top contact can overcome the vdW gap, and lower the corresponding tunnel barrier, thereby reduce the contact resistance. 3) Phase engineering is another effective method, originating from the existence of different phases of TMDCs (metal and semiconductor phase) [78, 284-286]. However, these methods are not perfect. 2D contact electrodes create large vdW gaps; edge contacts are difficult to accomplish in the process preparation; phase engineering is limited by the phase control of the material itself. In addition, contact scaling further increases the difficulty of resistance reduction. More importantly, the reliability and

repeatability of extending these methods to large-scale 2D ICs are unknown. Large-scale process implementation in 2D ICs should also be examined. To realize the preparation and application of large-area 2D devices, it is necessary to develop a metal electrode preparation process compatible with large-area processes. Although some methods such as semimetal contact and alloy contact are reported to be promising, further improving thermal stability compatible with BEOL is quite important.

5.4.3 Doping

Through substitutional doping by elements such as niobium and rhenium, 2D materials can be converted to n- and p-type. However, it is very difficult to achieve controllable doping and spatially pattern the dopants, during the growth stage of the material. Even though patterning is possible, for example by plasma doping, lattice defects may be introduced, resulting in performance degradation. Additionally, atomic substitution has indeed been achieved in the lattice, but it does not mean that the doping is activated and the n- or p-type of the material is transformed [287]. For 2D materials, a more potential doping strategy is interface charge transfer doping, introduced in *2.2.2*. However, the doping efficiency and stability of this process are challenged [288]. In large-scale ICs, the realization of complementary FET requires the help of doping, and the efficiency and stability of doping are critical to the circuit. It is critical to find reliable doping strategies that can be applied to production lines. Going forward, optimizing existing or finding new dopants remains important to improve the stability and controllability of doping.

5.4.4 Dielectric integration

Integration of suitable and ultrathin dielectrics with channel materials is indispensable to enable the scaling down of FETs. According to the IRDS roadmap, the EOT must not exceed 0.5 nm after the 3 nm node [209]. Regarding gate dielectric scaling, it is necessary to balance the thickness of the dielectric and the gate capacitance to ensure that gate leakage current is

minimized and that efficient gate coupling can be provided. For 2D FETs, h-BN is a layered insulating dielectric that is often considered. However, with the scaling down of devices, especially when the EOT is required to be lower than 1 nm, h-BN is not suitable as a gate insulator due to its relatively small dielectric constant [289]. Thus, 2D FETs need high-quality thin high-κ dielectric to improve gate control. The dangling bond-free surface of 2D materials makes it challenging to directly grow high-quality thin gate dielectrics on top of 2D channels. There have been some efforts to realize scalable, high-κ dielectrics, including HfO_2, CaF_2, Bi_2SeO_5, MoO_3, and so on, on top of 2D materials [290-293]. While some of these have shown real promise, the reality is that these viable technologies need to be compatible with specific processes. It is necessary to continue to develop them for consistency and scalability to be applicable to large-scale manufacturing scenarios. We believe that the next generation of 2D material-based VLSI can be expected to achieve performance improvements with further exploration of suitable gate insulators or gate-insulator stacks formed from combinations of several insulators.

5.5. Outlook of 2D ICs

In the post-Moore era, the development of ICs is not only the pursuit of speed and cost, but also the extension and expansion of functions. Flexible wearable electronic devices have become a great demand for future development. 2D ICs have become a potential force in the field of flexible electronics in the future due to their inherent flexibility.

In order to improve the integration density of current lateral circuits, 3D vertical 2D ICs were proposed because of the thinness and ease of vertical stacking of 2D materials [42, 294]. 3D integration and packaging will become the future development trend to meet the needs of high-density ICs. Furthermore, the integration of multiple functional 2D devices, as well as

the complementary combination of 2D and silicon-based devices will also become a potential possibility in the future.

The challenges faced under the traditional computing architecture are the problems of memory wall and Von Neumann bottleneck. One solution is logic-in-memory computing. The developed logic-in-memory devices and circuits based on MoS_2 floating-gate FETs opened the way to the realization of energy-efficient circuits based on 2D materials [295]. 2D ICs have great potential to enable computation logic-in-memory computing.

Acknowledgements

This work was supported in part by National Natural Science Foundation of China under Grant 62022047, Grant 61874065, Grant U20A20168 and Grant 51861145202, in part by the National Key R&D Program under Grant 2016YFA0200400, in part by Fok Ying-Tong Education Foundation under Grant 171051, in part by Beijing Natural Science Foundation (M22020), in part by Beijing National Research Center for Information Science and Technology Youth Innovation Fund (BNR2021RC01007) and in part by State Key Laboratory of New Ceramic and Fine Processing Tsinghua University (No. KF202109), in part by Tsinghua-Foshan Innovation Special Fund(TFISF) (2021THFS0217), in part by the Research Fund from Beijing Innovation Center for Future Chip and the Independent Research Program of Tsinghua University under Grant 20193080047.

Received: ((will be filled in by the editorial staff))
Revised: ((will be filled in by the editorial staff))
Published online: ((will be filled in by the editorial staff))

References

[1] J. Bardeen, W. H. Brattain, *Phys. Rev.* **1948**, 74, 230.

[2] J. S. Kilby, *IEEE Trans. Electron Devices* **1976**, 23, 648.

[3] G. E. Moore, McGraw-Hill New York, 1965.

[4] G. E. Moore, 1975.

[5] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, A. Kis, *Nat. Nanotechnol.* **2011**, 6, 147.

[6] Q. H. Wang, K. Kalantar-Zadeh, A. Kis, J. N. Coleman, M. S. Strano, *Nat. Nanotechnol.* **2012**, 7, 699.

[7] K. I. Bolotin, K. J. Sikes, Z. Jiang, M. Klima, G. Fudenberg, J. Hone, P. Kim, H. L. Stormer, *Solid State Commun.* **2008**, 146, 351.

[8] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, M. I. Katsnelson, I. V. Grigorieva, S. V. Dubonos, A. A. Firsov, *Nature* **2005**, 438, 197.

[9] Y. Zhang, Y.-W. Tan, H. L. Stormer, P. Kim, *Nature* **2005**, 438, 201.

[10] X. Du, I. Skachko, F. Duerr, A. Luican, E. Y. Andrei, *Nature* **2009**, 462, 192.

[11] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, A. A. Firsov, *Science* **2004**, 306, 666.

[12] Schultz, Peter A, *Phys. Rev. Lett.* **2006**, 246401.

[13] X. Wang, Y. Ouyang, X. Li, H. Wang, J. Guo, H. Dai, *Phys. Rev. Lett.* **2008**, 100, 206803.

[14] A. Kozhakhmetov, T. H. Choudhury, Z. Y. Al Balushi, M. Chubarov, J. M. Redwing, *J. Cryst. Growth* **2018**, 486, 137.

[15] J. Shi, X. Wang, S. Zhang, L. Xiao, Y. Huan, Y. Gong, Z. Zhang, Y. Li, X. Zhou, M. Hong, Q. Fang, Q. Zhang, X. Liu, L. Gu, Z. Liu, Y. Zhang, *Nat. Commun.* **2017**, 8, 958.

[16] L. Yu, A. Zubair, E. J. G. Santos, X. Zhang, Y. Lin, Y. Zhang, T. Palacios, *Nano Lett.* **2015**, 15, 4928.

[17] A. Kozhakhmetov, R. Torsi, C. Y. Chen, J. A. Robinson, *J. Phys.: Mater.* **2020**, 4, 012001.

[18] H. Fang, S. Chuang, T. C. Chang, K. Takei, T. Takahashi, A. Javey, *Nano Lett.* **2012**, 12, 3788.

[19] S. Fathipour, N. Ma, W. S. Hwang, V. Protasenko, S. Vishwanath, H. G. Xing, H. Xu, D. Jena, J. Appenzeller, A. Seabaugh, *Appl. Phys. Lett.* **2014**, 105, 192101.

[20] W. Zhang, Y. Liu, X. Pei, Z. Yuan, Y. Zhang, Z. Zhao, H. Hao, R. Long, N. Liu, *Adv. Funct. Mater.* **2021**.

[21] T.-H. Han, H. Kim, S.-J. Kwon, T.-W. Lee, *Materials Science and Engineering: R: Reports* **2017**, 118, 1.

[22] C. Koo Hyun, H. Kwon Jae, J. Eom, J. Chang, H. Han Suk, M. Johnson, *Science* **2009**, 325, 1515.

[23] S. Wachter, D. K. Polyushkin, O. Bethge, T. Mueller, *Nat. Commun.* **2017**, 8, 14948.

[24] J.-H. Lee, E. K. Lee, W.-J. Joo, Y. Jang, B.-S. Kim, J. Y. Lim, S.-H. Choi, S. J. Ahn, J. R. Ahn, M.-H. Park, *Science* **2014**, 344, 286.

[25] H. Yu, M. Liao, W. Zhao, G. Liu, X. J. Zhou, Z. Wei, X. Xu, K. Liu, Z. Hu, K. Deng, *ACS nano* **2017**, 11, 12001.

[26] Q. Wang, N. Li, J. Tang, J. Zhu, Q. Zhang, Q. Jia, Y. Lu, Z. Wei, H. Yu, Y. Zhao, *Nano Lett.* **2020**, 20, 7193.

[27] X. Zhang, T. Wu, Q. Jiang, H. Wang, H. Zhu, Z. Chen, R. Jiang, T. Niu, Z. Li, Y. Zhang, *Small* **2019**, 15, 1805395.

[28] M. Schmidt, M. C. Lemme, H. D. B. Gottlob, F. Driussi, L. Selmi, H. Kurz, *Solid-State Electron.* **2009**, 53, 1246.

[29] B. Yu, L. Chang, S. Ahmed, H. Wang, S. Bell, C.-Y. Yang, C. Tabery, C. Ho, Q. Xiang, T.-J. King, 2002.

[30] G. Bae, D. I. Bae, M. Kang, S. M. Hwang, S. S. Kim, B. Seo, T. Y. Kwon, T. J. Lee, C. Moon, Y. M. Choi, 2018.

[31] K. H. Yeo, S. D. Suk, M. Li, Y.-y. Yeoh, K. H. Cho, K.-H. Hong, S. Yun, M. S. Lee, N. Cho, K. Lee, 2006.

[32] Lu, Peng, IEEE Trans. Electron Devices **2021**, 68, 1352.

[33] X. Cui, G.-H. Lee, Y. D. Kim, G. Arefe, P. Y. Huang, C.-H. Lee, D. A. Chenet, X. Zhang, L. Wang, F. Ye, *Nat. Nanotechnol.* **2015**, 10, 534.

[34] S. Y. Kim, S. Park, W. Choi, *Appl. Phys. Lett.* **2016**, 109, 152101.

[35] S. B. Desai, S. R. Madhvapathy, A. B. Sachid, J. P. Llinas, Q. Wang, G. H. Ahn, G. Pitner, M. J. Kim, J. Bokor, C. Hu, *Science* **2016**, 354, 99.

[36] F. Wu, H. Tian, Y. Shen, Z. Hou, J. Ren, G. Gou, Y. Sun, Y. Yang, T.-L. Ren, *Nature* **2022**, 603, 259.

[37] L. Xie, M. Liao, S. Wang, H. Yu, L. Du, J. Tang, J. Zhao, J. Zhang, P. Chen, X. Lu, *Adv. Mater.* **2017**, 29, 1702522.

[38] F. Wu, J. Ren, Y. Yang, Z. Yan, H. Tian, G. Gou, X. Wang, Z. Zhang, X. Yang, X. Wu, *Adv. Electron. Mater.* **2021**, 2100543.

[39] M.-L. Chen, X. Sun, H. Liu, H. Wang, Q. Zhu, S. Wang, H. Du, B. Dong, J. Zhang, Y. Sun, S. Qiu, T. Alava, S. Liu, D.-M. Sun, Z. Han, *Nat. Commun.* **2020**, 11, 1205.

[40] Z. Tang, C. Liu, X. Huang, S. Zeng, L. Liu, J. Li, Y. G. Jiang, D. W. Zhang, P. Zhou, *Nano Lett* **2021**, 21, 1758.

[41] X. Huang, C. Liu, Z. Tang, S. Zeng, L. Liu, X. Hou, H. Chen, J. Li, Y.-G. Jiang, D. W. Zhang, P. Zhou, in *2020 IEEE International Electron Devices Meeting (IEDM)*, 2020.

[42] J. Tang, Q. Wang, Z. Wei, C. Shen, X. Lu, S. Wang, Y. Zhao, J. Liu, N. Li, Y. Chu, *Adv. Electron. Mater.* **2020**, 6, 2000550.

[43] J. Tang, Q. Wang, Z. Wei, C. Shen, X. Lu, S. Wang, Y. Zhao, J. Liu, N. Li, Y. Chu, J. Tian, F. Wu, W. Yang, C. He, R. Yang, D. Shi, K. Watanabe, T. Taniguchi, G. Zhang, *Adv. Electron. Mater.* **2020**, 6.

[44] D. Verreck, G. Arutchelvan, C. J. L. De La Rosa, A. Leonhardt, D. Chiappe, A. K. A. Lu, G. Pourtois, P. Matagne, M. M. Heyns, S. De Gendt, *IEEE Trans. Electron Devices* **2018**, 65, 4635.

[45] Z. Dong, J. Guo, *IEEE Trans. Electron Devices* **2017**, 64, 622.

[46] H. Zhang, B. Shi, L. Xu, J. Yan, W. Zhao, Z. Zhang, Z. Zhang, J. Lu, *ACS Appl. Electron. Mater.* **2021**, 3, 1560.

[47] A. Vandooren, J. Franco, Z. Wu, B. Parvais, W. Li, L. Witters, A. Walke, L. Peng, V. Deshpande, N. Rassoul, 2018.

[48] J. Ryckaert, P. Schuddinck, P. Weckx, G. Bouche, B. Vincent, J. Smith, Y. Sherazi, A. Mallik, H. Mertens, S. Demuynck, 2018.

[49] S. Subramanian, M. Hosseini, T. Chiarella, S. Sarkar, P. Schuddinck, B. T. Chan, D. Radisic, G. Mannaert, A. Hikavyy, E. Rosseel, 2020.

[50] S. Barraud, B. Previtali, C. Vizioz, J. M. Hartmann, J. Sturm, J. Lassarre, C. Perrot, P. Rodriguez, V. Loup, A. Magalhaes-Lucas, 2020.

[51] X. Xiong, T. Wu, C. Cheng, S. Zhan, I. Ni, S. Wang, Y. Chang, S. Liew, E. Chen, W. Chang, C. Wu, J. Cai, H. Wong, H. Wang, presented at 2021 IEEE International Electron Devices Meeting (IEDM), **2021**, San Francisco, CA, USA.

[52] M. Li, R. Huang, *SCIENTIA SINICA Informationis* **2018**, 48, 963.

[53] A. Rai, A. Valsaraj, H. C. Movva, A. Roy, R. Ghosh, S. Sonde, S. Kang, J. Chang, T. Trivedi, R. Dey, S. Guchhait, S. Larentis, L. F. Register, E. Tutuc, S. K. Banerjee, *Nano Lett.* **2015**, 15, 4329.

[54] J. Suh, T. E. Park, D. Y. Lin, D. Fu, J. Park, H. J. Jung, Y. Chen, C. Ko, C. Jang, Y. Sun, R. Sinclair, J. Chang, S. Tongay, J. Wu, *Nano Lett.* **2014**, 14, 6976.

[55] A. Nipane, D. Karmakar, N. Kaushik, S. Karande, S. Lodha, *ACS nano* **2016**, 10, 2128.

[56] L. Cai, C. J. McClellan, A. L. Koh, H. Li, E. Yalon, E. Pop, X. Zheng, *Nano Lett.* **2017**, 17, 3854.

[57] S. Vaziri, V. Chen, L. Cai, Y. Jiang, M. E. Chen, R. W. Grady, X. Zheng, E. Pop, *IEEE Electron Device Lett.* **2020**, 41, 1592.

[58] K. Schauble, D. Zakhidov, E. Yalon, S. Deshmukh, R. W. Grady, K. A. Cooley, C. J. McClellan, S. Vaziri, D. Passarello, S. E. Mohney, *ACS nano* **2020**, 14, 14798.

[59] H. Fang, M. Tosun, G. Seol, T. C. Chang, K. Takei, J. Guo, A. Javey, *Nano Lett.* **2013**, 13, 1991.

[60] C. J. McClellan, E. Yalon, K. K. H. Smithe, S. V. Suryavanshi, E. Pop, *ACS nano* **2021**, 15, 1587.

[61] D. Kiriya, M. Tosun, P. Zhao, J. S. Kang, A. Javey, *JACS* **2014**, 136, 7853.

[62] S. Fathipour, P. Pandey, S. Fullerton-Shirey, A. Seabaugh, *J. Appl. Phys.* **2016**, 120, 234902.

[63] A. Leonhardt, D. Chiappe, V. V. Afanas' ev, S. El Kazzi, I. Shlyakhov, T. Conard, A. Franquet, C. Huyghebaert, S. de Gendt, *ACS Appl. Mater. Interfaces* **2019**, 11, 42697.

[64] H. Gao, J. Suh, M. C. Cao, A. Y. Joe, F. Mujid, K.-H. Lee, S. Xie, P. Poddar, J.-U. Lee, K. Kang, *Nano Lett.* **2020**, 20, 4095.

[65] S. Fan, S. J. Yun, W. J. Yu, Y. H. Lee, *Adv. Sci.* **2020**, 7, 1902751.

[66] P.-C. Shen, Y. Lin, C. Su, C. McGahan, A.-Y. Lu, X. Ji, X. Wang, H. Wang, N. Mao, Y. Guo, J.-H. Park, Y. Wang, W. Tisdale, J. Li, X. Ling, K. E. Aidala, T. Palacios, J. Kong, *Nat. Electron.* **2021**, 5, 28.

[67] B. H. Moon, G. H. Han, H. Kim, H. Choi, J. J. Bae, J. Kim, Y. Jin, H. Y. Jeong, M.-K. Joo, Y. H. Lee, *ACS Appl. Mater. Interfaces* **2017**, 9, 11240.

[68] S. Das, H.-Y. Chen, A. V. Penumatcha, J. Appenzeller, *Nano Lett.* **2013**, 13, 100.

[69] Y. Guo, D. Liu, J. Robertson, *ACS Appl. Mater. Interfaces* **2015**, 7, 25709.

[70] H. Yuan, G. Cheng, L. You, H. Li, H. Zhu, W. Li, J. J. Kopanski, Y. S. Obeng, A. R. Hight Walker, D. J. Gundlach, *ACS Appl. Mater. Interfaces* **2015**, 7, 1180.

[71] C. Kim, I. Moon, D. Lee, M. S. Choi, F. Ahmed, S. Nam, Y. Cho, H.-J. Shin, S. Park, W. J. Yoo, *ACS nano* **2017**, 11, 1588.

[72] P. Bampoulis, R. van Bremen, Q. Yao, B. Poelsema, H. J. W. Zandvliet, K. Sotthewes, *ACS Appl. Mater. Interfaces* **2017**, 9, 19278.

[73] P.-C. Shen, C. Su, Y. Lin, A.-S. Chou, C.-C. Cheng, J.-H. Park, M.-H. Chiu, A.-Y. Lu, H.-L. Tang, M. M. Tavakoli, *Nature* **2021**, 593, 211.

[74] P.-C. Shen, Y. Lin, C. Su, C. McGahan, A.-Y. Lu, X. Ji, X. Wang, H. Wang, N. Mao, Y. Guo, *Nat. Electron.* **2022**, 5, 28.

[75] W. Zhou, X. Zou, S. Najmaei, Z. Liu, Y. Shi, J. Kong, J. Lou, P. M. Ajayan, B. I. Yakobson, J.-C. Idrobo, *Nano Lett.* **2013**, 13, 2615.

[76] J. Tersoff, *Phys. Rev. Lett.* **1984**, 52, 465.

[77] X. Cui, E.-M. Shih, L. A. Jauregui, S. H. Chae, Y. D. Kim, B. Li, D. Seo, K. Pistunova, J. Yin, J.-H. Park, *Nano Lett.* **2017**, 17, 4781.

[78] A. Allain, J. Kang, K. Banerjee, A. Kis, *Nat. Mater.* **2015**, 14, 1195.

[79] S. S. Chee, D. Seo, H. Kim, H. Jang, S. Lee, S. P. Moon, K. H. Lee, S. W. Kim, H. Choi, M. H. Ham, *Adv. Mater.* **2019**, 31, 1804422.

[80] Y. Wang, J. C. Kim, R. J. Wu, J. Martinez, X. Song, J. Yang, F. Zhao, A. Mkhoyan, H. Y. Jeong, M. Chhowalla, *Nature* **2019**, 568, 70.

[81] A. Chou, T. Wu, C. Cheng, S. Zhan, I. Ni, S. Wang, Y. Chang, S. Liew, E. Chen, W. Chang, C. Wu, J. Cai, H. Wong, H. Wang, presented at 2021 IEEE International Electron Devices Meeting (IEDM), **2021**, San Francisco, CA, USA.

[82] K. P. O'Brien, presented at 2021 IEEE International Electron Devices Meeting (IEDM), **2021**, San Francisco, CA, USA.

[83] A. Kumar, presented at 2021 IEEE International Electron Devices Meeting (IEDM), **2021**, San Francisco, CA, USA.

[84] M. Amani, D.-H. Lien, D. Kiriya, J. Xiao, A. Azcatl, J. Noh, S. R. Madhvapathy, R. Addou, S. Kc, M. Dubey, *Science* **2015**, 350, 1065.

[85] Z. Yu, Y. Pan, Y. Shen, Z. Wang, Z.-Y. Ong, T. Xu, R. Xin, L. Pan, B. Wang, L. Sun, *Nat. Commun.* **2014**, 5, 1.

[86] H. Nan, Z. Wang, W. Wang, Z. Liang, Y. Lu, Q. Chen, D. He, P. Tan, F. Miao, X. Wang, *ACS nano* **2014**, 8, 5738.

[87] Y. Liu, J. Guo, E. Zhu, L. Liao, S. J. Lee, M. Ding, I. Shakir, V. Gambin, Y. Huang, X. Duan, *Nature* **2018**, 557, 696.

[88] T. D. Ngo, Z. Yang, M. Lee, F. Ali, I. Moon, D. G. Kim, T. Taniguchi, K. Watanabe, K. Y. Lee, W. J. Yoo, *Adv. Electron. Mater.* **2021**, 7.

[89] S. McDonnell, R. Addou, C. Buie, R. M. Wallace, C. L. Hinkle, *ACS nano* **2014**, 8, 2880.

[90] R. Jhaveri, V. Nagavarapu, J. C. S. Woo, *IEEE Trans. Electron Devices* **2008**, 56, 93.

[91] X. X. Li, Z. Q. Fan, P. Z. Liu, M. L. Chen, X. Liu, C. K. Jia, D. M. Sun, X. W. Jiang, Z. Han, V. Bouchiat, J. J. Guo, J. H. Chen, Z. D. Zhang, *Nat. Commun.* **2017**, 8, 970.

[92] L. Wang, I. Meric, P. Y. Huang, Q. Gao, Y. Gao, H. Tran, T. Taniguchi, K. Watanabe, L. M. Campos, D. A. Muller, *Science* **2013**, 342, 614.

[93] H. Choi, B. H. Moon, J. H. Kim, S. J. Yun, G. H. Han, S.-g. Lee, H. Z. Gul, Y. H. Lee, *ACS Nano* **2019**, 13, 13169.

[94] Z. Yang, C. Kim, K. Y. Lee, M. Lee, S. Appalakondaiah, C. H. Ra, K. Watanabe, T. Taniguchi, K. Cho, E. Hwang, *Adv. Mater.* **2019**, 31, 1808231.

[95] T. D. Ngo, Z. Yang, M. Lee, F. Ali, I. Moon, D. G. Kim, T. Taniguchi, K. Watanabe, K.-Y. Lee, W. J. Yoo, *Adv. Electron. Mater.* **2021**, 7, 2001212.

[96] B. H. Moon, G. H. Han, H. Kim, H. Choi, J. J. Bae, J. Kim, Y. Jin, H. Y. Jeong, M.-K. Joo, Y. H. Lee, S. C. Lim, *ACS Appl. Mater. Interfaces* **2017**, 9, 11240.

[97] J. Appenzeller, Y. M. Lin, J. Knoch, P. Avouris, *Phys. Rev. Lett.* **2004**, 93, 196805.

[98] W. Y. Choi, B.-G. Park, J. D. Lee, T.-J. K. Liu, *IEEE Electron Device Lett.* **2007**, 28, 743.

[99] A. M. Ionescu, H. Riel, *Nature* **2011**, 479, 329.

[100] A. C. Seabaugh, Q. Zhang, *Proceedings of the IEEE* **2010**, 98, 2095.

[101] S. Salahuddin, S. Datta, *Nano Lett.* **2008**, 8, 405.

[102] J. Jo, W. Y. Choi, J.-D. Park, J. W. Shim, H.-Y. Yu, C. Shin, *Nano Lett.* **2015**, 15, 4553.

[103] A. I. Khan, K. Chatterjee, J. P. Duarte, Z. Lu, A. Sachid, S. Khandelwal, R. Ramesh, C. Hu, S. Salahuddin, *IEEE Electron Device Lett.* **2015**, 37, 111.

[104] A. I. Khan, K. Chatterjee, B. Wang, S. Drapcho, L. You, C. Serrao, S. R. Bakaul, R. Ramesh, S. Salahuddin, *Nat. Mater.* **2015**, 14, 182.

[105] A. Islam Khan, D. Bhowmik, P. Yu, S. Joo Kim, X. Pan, R. Ramesh, S. Salahuddin, *Appl. Phys. Lett.* **2011**, 99, 113501.

[106] F. A. McGuire, Y.-C. Lin, K. Price, G. B. Rayner, S. Khandelwal, S. Salahuddin, A. D. Franklin, *Nano Lett.* **2017**, 17, 4801.

[107] E. Ko, J. W. Lee, C. Shin, *IEEE Electron Device Lett.* **2017**, 38, 418.

[108] N. Abelé, R. Fritschi, K. Boucart, F. Casset, P. Ancey, A. M. Ionescu, 2005.

[109] K. Akarvardar, D. Elata, R. Parsa, G. C. Wan, K. Yoo, J. Provine, P. Peumans, R. T. Howe, H. S. Wong, 2007.

[110] N. Oliva, L. Capua, M. Cavalieri, A. M. Ionescu, 2019.

[111] A. Dankert, S. P. Dash, *Nat. Commun.* **2017**, 8, 1.

[112] H. B. Jeon, G. H. Shin, K. J. Lee, S. Y. Choi, *Adv. Electron. Mater.* **2020**, 6, 2000091.

[113] D. Sarkar, X. Xie, W. Liu, W. Cao, J. Kang, Y. Gong, S. Kraemer, P. M. Ajayan, K. Banerjee, *Nature* **2015**, 526, 91.

[114] J. He, N. Fang, K. Nakamura, K. Ueno, T. Taniguchi, K. Watanabe, K. Nagashio, *Adv. Electron. Mater.* **2018**, 4, 1800207.

[115] S. Kim, G. Myeong, W. Shin, H. Lim, B. Kim, T. Jin, S. Chang, K. Watanabe, T. Taniguchi, S. Cho, *Nat. Nanotechnol.* **2020**, 15, 203.

[116] X. Jiang, X. Shi, M. Zhang, Y. Wang, Z. Gu, L. Chen, H. Zhu, K. Zhang, Q. Sun, D. W. Zhang, *ACS Appl. Nano Mater.* **2019**, 2, 5674.

[117] N. T. Duong, C. Park, D. H. Nguyen, P. H. Nguyen, T. U. Tran, D. Y. Park, J. Lee, D. A. Nguyen, J. H. Oh, Y. S. Yu, M. S. Jeong, *Nano Today* **2021**, 40.

[118] J. Xu, J. Jia, S. Lai, J. Ju, S. Lee, *Appl. Phys. Lett.* **2017**, 110.

[119] T. Roy, M. Tosun, M. Hettick, G. H. Ahn, C. Hu, A. Javey, *Appl. Phys. Lett.* **2016**, 108.

[120] X. Yan, C. Liu, C. Li, W. Bao, S. Ding, D. W. Zhang, P. Zhou, *Small* **2017**, 13.

[121] N. Oliva, J. Backman, L. Capua, M. Cavalieri, M. Luisier, A. M. Ionescu, *npj 2D Mater. Appl.* **2020**, 4.

[122] S. Salahuddin, S. Datta, *Nano Lett.* **2008**, 8, 405.

[123] M. A. Alam, M. Si, P. D. Ye, *Appl. Phys. Lett.* **2019**, 114.

[124] Z. Yu, H. Wang, W. Li, S. Xu, X. Song, S. Wang, P. Wang, P. Zhou, Y. Shi, Y. Chai, 2017.

[125] M. Si, C. J. Su, C. Jiang, N. J. Conrad, H. Zhou, K. D. Maize, G. Qiu, C. T. Wu, A. Shakouri, M. A. Alam, P. D. Ye, *Nat. Nanotechnol.* **2018**, 13, 24.

[126] A. Nourbakhsh, A. Zubair, S. Joglekar, M. Dresselhaus, T. Palacios, *Nanoscale* **2017**, 9, 6122.

[127] M. Si, C. Jiang, W. Chung, Y. Du, M. A. Alam, P. D. Ye, *Nano Lett.* **2018**, 18, 3682.

[128] J. Dong, Z. Sheng, R. Yu, W. Hu, Y. Wang, H. Sun, D. W. Zhang, P. Zhou, Z. Zhang, *Adv. Electron. Mater.* **2021**, 8.

[129] H. Tian, Y.-X. Li, L. Li, X. Wang, R. Liang, Y. Yang, T.-L. Ren, *IEEE Trans. Electron Devices* **2019**, 66, 1579.

[130] J. Wang, X. Guo, Z. Yu, Z. Ma, Y. Liu, Z. Lin, M. Chan, Y. Zhu, X. Wang, Y. Chai, *Adv. Funct. Mater.* **2020**, 30.

[131] Y.-C. Lin, G. B. Rayner, J. Cardenas, A. D. Franklin, *Appl. Phys. Lett.* **2021**, 118.

[132] F. Liu, L. You, K. L. Seyler, X. Li, P. Yu, J. Lin, X. Wang, J. Zhou, H. Wang, H. He, S. T. Pantelides, W. Zhou, P. Sharma, X. Xu, P. M. Ajayan, J. Wang, Z. Liu, *Nat. Commun.* **2016**, 7, 12357.

[133] X. Wang, P. Yu, Z. Lei, C. Zhu, X. Cao, F. Liu, L. You, Q. Zeng, Y. Deng, C. Zhu, J. Zhou, Q. Fu, J. Wang, Y. Huang, Z. Liu, *Nat. Commun.* **2019**, 10, 3037.

[134] W. Cao, K. Banerjee, *Nat. Commun*. **2020**, 11, 196.

[135] R. Zhao, X. Zhao, H. Liu, M. Shao, Q. Feng, T. Liu, T. Lu, X. Wu, Y. Yi, T.-L. Ren, *IEEE Electron Device Lett.* **2021**, 42, 1164.

[136] Y. Zheng, G. X. Ni, C. T. Toh, C. Y. Tan, K. Yao, B. Ozyilmaz, *Phys. Rev. Lett.* **2010**, 105, 166602.

[137] L. Chen, L. Wang, Y. Peng, X. Feng, S. Sarkar, S. Li, B. Li, L. Liu, K. Han, X. Gong, *Adv. Electron. Mater.* **2020**, 6, 2000057.

[138] C. Qiu, F. Liu, L. Xu, B. Deng, M. Xiao, J. Si, L. Lin, Z. Zhang, J. Wang, H. Guo, *Science* **2018**, 361, 387.

[139] W. Zhang, B. Gao, J. Tang, P. Yao, S. Yu, M.-F. Chang, H.-J. Yoo, H. Qian, H. Wu, *Nat. Electron.* **2020**, 3, 371.

[140] H. S. P. Wong, H.-Y. Lee, S. Yu, Y.-S. Chen, Y. Wu, P.-S. Chen, B. Lee, F. T. Chen, M.-J. Tsai, *Proceedings of the IEEE* **2012**, 100, 1951.

[141] H. Tian, X. Wang, H. Zhao, W. Mi, Y. Yang, P. W. Chiu, T. L. Ren, *Adv. Electron. Mater.* **2018**, 4, 1700608.

[142] X.-F. Wang, H. Tian, Y. Liu, S. Shen, Z. Yan, N. Deng, Y. Yang, T.-L. Ren, *ACS nano* **2019**, 13, 2205.

[143] Q. Hua, G. Gao, C. Jiang, J. Yu, J. Sun, T. Zhang, B. Gao, W. Cheng, R. Liang, H. Qian, W. Hu, Q. Sun, Z. L. Wang, H. Wu, *Nat. Commun.* **2020**, 11, 6207.

[144] F. Zahoor, T. Z. A. Zulkifli, F. A. Khanday, *Nanoscale Res. Lett.* **2020**, 15, 1.

[145] J. Lin, X. Chen, X. Duan, Z. Yu, W. Niu, M. Zhang, C. Liu, G. Li, Y. Liu, X. Liu, *Adv. Sci.* **2022**, 2104439.

[146] S. Datta, B. Das, *Appl. Phys. Lett.* **1990**, 665, 56.

[147] A. Dankert, S. P. Dash, *Nat. Commun.* **2017**, 8, 16093.

[148] L. Yang, N. A. Sinitsyn, W. Chen, J. Yuan, J. Zhang, J. Lou, S. Crooker, *Nat. Phys.* **2015**, 11, 830.

[149] S. Gupta, F. Rortais, R. Ohshima, Y. Ando, T. Endo, Y. Miyata, M. Shiraishi, *Sci. Rep.* **2019**.

[150] X. Qian, J. Liu, L. Fu, J. Li, *Science* **2014**, 346, 1344.

[151] A. Avsar, J. Y. Tan, M. Kurpas, M. Gmitra, K. Watanabe, T. Taniguchi, J. Fabian, B. ?zyilmaz, *Nat. Phys.*.

[152] A. Hashmi, J. Hong, *J. Phys. Chem. C* **2015**, 119, 150408123826004.

[153] C. Zheng, K. Jiang, K. Yao, S. Zhu, K. Wu, *Phys. Chem. Chem. Phys.* **2021**, 23, 24570.

[154] A. Avsar, J. Y. Tan, M. Kurpas, M. Gmitra, K. Watanabe, T. Taniguchi, J. Fabian, B. Özyilmaz, *Nat. Phys.* **2017**, 13, 888.

[155] A. Hashmi, J. Hong, *J. Phys. Chem. C* **2015**, 119, 9198.

[156] D. A. Neamen, *Semiconductor Physics and Devices: Basic Principles, Fourth Edition*, McGraw-Hill, **2011**.

[157] M. Amato, M. Palummo, S. Ossicini, *Phys. Rev. B* **2009**, 80, 235333.

[158] M. Amato, M. Palummo, R. Rurali, S. Ossicini, *Chemical Reviews* **2014**, 114, 1371.

[159] Y. Xu, C. Cheng, S. Du, J. Yang, B. Yu, J. Luo, W. Yin, E. Li, S. Dong, P. Ye, X. Duan, *ACS Nano* **2016**, 10, 4895.

[160] E. J. Telford, A. Benyamini, D. Rhodes, D. Wang, Y. Jung, A. Zangiabadi, K. Watanabe, T. Taniguchi, S. Jia, K. Barmak, A. N. Pasupathy, C. R. Dean, J. Hone, *Nano Lett.* **2018**, 18, 1416.

[161] C. Grillet, D. Logoteta, A. Cresti, M. G. Pala, *IEEE Trans. Electron Devices* **2017**, 64, 2425.

[162] C. Medina-Bailon, H. Carrillo-Nunez, J. Lee, C. Sampedro, J. L. Padilla, L. Donetti, V. Georgiev, F. Gamiz, A. Asenov, *Micromachines* **2020**, 11.

[163] H. H. Radamson, H. Zhu, Z. Wu, X. He, H. Lin, J. Liu, J. Xiang, Z. Kong, W. Xiong, J. Li, H. Cui, J. Gao, H. Yang, Y. Du, B. Xu, B. Li, X. Zhao, J. Yu, Y. Dong, G. Wang, *Nanomaterials* **2020**, 10.

[164] V. Moroz, S. Smidstrup, M. Choi, A. Svizhenko, presented at *VLSI Techology Short Course 1.4, 2018 Symposia on VLSI Technology and Circuits*, **2018**.

[165] S. Berrada, H. Carrillo-Nunez, J. Lee, C. Medina-Bailon, T. Dutta, O. Badami, F. Adamu-Lema, V. Thirunavukkarasu, V. Georgiev, A. Asenov, *J. Comput. Electron.* **2020**, 19, 1031.

[166] L. Yang, R. N. Musin, X.-Q. Wang, M. Y. Chou, *Phys. Rev. B* **2008**, 77, 195325.

[167] O. Badami, C. Medina-Bailon, S. Berrada, H. Carrillo-Nunez, J. Lee, V. Georgiev, A. Asenov, *Appl. Sci.* **2019**, 9.

[168] H. Qiu, T. Xu, Z. Wang, W. Ren, H. Nan, Z. Ni, Q. Chen, S. Yuan, F. Miao, F. Song, G. Long, Y. Shi, L. Sun, J. Wang, X. Wang, *Nat. Commun.* **2013**, 4, 2642.

[169] W. Liu, J. Kang, D. Sarkar, Y. Khatami, D. Jena, K. Banerjee, *Nano Lett.* **2013**, 13, 1983.

[170] S. Singh, I. Kaur, *Physica E: Low-dimensional Systems and Nanostructures* **2020**, 118, 113960.

[171] Z. Ming, R. Qiushi, G. Ximeng, Z. Jinyu, W. Yan, Y. Zhiping, presented at *2008 International Conference on Simulation of Semiconductor Processes and Devices*, 9-11 Sept. 2008, **2008**.

[172] S. Fang, R. Kuate Defo, S. N. Shirodkar, S. Lieu, G. A. Tritsaris, E. Kaxiras, *Phys. Rev. B* **2015**, 92, 205108.

[173] A. N. Rudenko, M. I. Katsnelson, *Phys. Rev. B* **2014**, 89, 201408.

[174] M. Shahbazi, *Physica B: Condensed Matter* **2018**, 545, 159.

[175] J. Jiang, R. Saito, G. G. Samsonidze, A. Jorio, S. G. Chou, G. Dresselhaus, M. S. Dresselhaus, *Phys. Rev. B* **2007**, 75, 035407.

[176] R. Wilson Neil, V. Nguyen Paul, K. Seyler, P. Rivera, J. Marsden Alexander, P. L. Laker Zachary, C. Constantinescu Gabriel, V. Kandyba, A. Barinov, D. M. Hine Nicholas, X. Xu, H. Cobden David, *Sci. Adv.*, 3, e1601832.

[177] X.-J. Zhang, B.-G. Liu, *Semicond. Sci. Technol.* **2016**, 31, 125002.

[178] W. Cao, J. Kang, D. Sarkar, W. Liu, K. Banerjee, presented at *2014 IEEE International Electron Devices Meeting*, 15-17 Dec. 2014, **2014**.

[179] Y. Lee, T. Agarwal, M. Luisier, presented at *2020 IEEE International Electron Devices Meeting (IEDM)*, 12-18 Dec. 2020, **2020**.

[180] Y. Lee, S. Fiore, M. Luisier, presented at *2019 IEEE International Electron Devices Meeting (IEDM)*, 7-11 Dec. 2019, **2019**.

[181] J. Xia, F. Chen, J. Li, N. Tao, *Nat. Nanotechnol.* **2009**, 4, 505.

[182] Z. Johari, N. A. Amin, M. T. Ahmadi, D. C. Y. Chek, S. M. Mousavi, R. Ismail, *AIP Conference Proceedings* **2011**, 1341, 384.

[183] T. Sruthi, K. Tarafder, *Bulletin of Materials Science* **2019**, 42, 257.

[184] T. Fang, A. Konar, H. Xing, D. Jena, *Appl. Phys. Lett.* **2007**, 91, 092109.

[185] S. Peng, Z. Jin, Y. Yao, L. Li, D. Zhang, J. Shi, X. Huang, J. Niu, Y. Zhang, G. Yu, *Adv. Electron. Mater.* **2019**, 5, 1900042.

[186] L. Du, H. Yu, L. Xie, S. Wu, S. Wang, X. Lu, M. Liao, J. Meng, J. Zhao, J. Zhang, J. Zhu, P. Chen, G. Wang, R. Yang, D. Shi, G. Zhang, *Crystals* **2016**, 6.

[187] M. Hosseini, M. Elahi, M. Pourfath, D. Esseni, *J. Phys. D: Appl. Phys.* **2015**, 48, 375104.

[188] J. Jiang, Y. Zhang, A. Wang, J. Duan, H. Ji, J. Pang, Y. Sang, X. Feng, H. Liu, L. Han, *ACS Appl. Electron. Mater.* **2020**, 2, 2132.

[189] Y. Liu, J. Zeng, Z. Zhu, X. Dong, W. Deng, *Japanese J. Appl. Phys.* **2020**, 59, 104004.

[190] J. Cao, S. Peng, W. Liu, Q. Wu, L. Li, D. Geng, G. Yang, Z. Ji, N. Lu, M. Liu, *J. Appl. Phys.* **2018**, 123, 064501.

[191] L. Wang, Y. Li, X. Gong, A. V. Y. Thean, G. Liang, *IEEE Electron Device Lett.* **2018**, 39, 761.

[192] Y.-Y. Chen, Z. Sun, D. Chen, in *Proceedings of the 52nd Annual Design Automation Conference*, Association for Computing Machinery, San Francisco, California 2015.

[193] E. M. Bazizi, A. Pal, J. Kim, L. Jiang, V. Reddy, B. Alexander, B. Ayyagari-Sangamalli, *IEEE Trans. Electron Devices* **2021**, 68, 5358.

[194] M. Turowski, A. Raman, A. Fedoseyev, presented at *2009 MIXDES-16th International Conference Mixed Design of Integrated Circuits & Systems*, 25-27 June 2009, **2009**.

[195] T. Ma, V. Moroz, R. Borges, K. E. Sayed, P. Asenov, A. Asenov, presented at *2016 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)*, 6-8 Sept. 2016, **2016**.

[196] D.-H. Zhao, Z.-L. Tian, H. Liu, Z.-H. Gu, H. Zhu, L. Chen, Q.-Q. Sun, D. W. Zhang, *ACS Appl. Mater. Interfaces* **2020**, 12, 14308.

[197] A. S. Chou, C. C. Cheng, S. L. Liew, P. H. Ho, S. Y. Wang, Y. C. Chang, C. K. Chang, Y. C. Su, Z. D. Huang, F. Y. Fu, C. F. Hsu, Y. Y. Chung, W. H. Chang, L. J. Li, C. I. Wu, *IEEE Electron Device Lett.* **2021**, 42, 272.

[198] C. S. Lee, B. Cline, S. Sinha, G. Yeric, H. S. P. Wong, presented at *2016 IEEE International Electron Devices Meeting (IEDM)*, 3-7 Dec. 2016, **2016**.

[199] Y.-N. Chen, C.-J. Chen, M.-L. Fan, V. P. Hu, P. Su, C.-T. Chuang, *Journal of Low Power Electronics and Applications* **2015**, 5.

[200] M. Fahad, Z. Zhao, A. Srivastava, L. Peng, presented at *2016 IEEE International Symposium on Nanoelectronic and Information Systems (iNIS)*, 19-21 Dec. 2016, **2016**.

[201] A. Mallik, D. Garbin, A. Fantini, D. Rodopoulos, R. Degraeve, J. Stuijt, A. K. Das, S. Schaafsma, P. Debacker, G. Donadio, H. Hody, L. Goux, G. S. Kar, A. Furnemont, A. Mocuta, P. Raghavan, presented at *2017 Symposium on VLSI Technology*, 5-8 June 2017, **2017**.

[202] Z. Zhang, R. Wang, C. Chen, Q. Huang, Y. Wang, C. Hu, D. Wu, J. Wang, R. Huang, presented at *2019 Silicon Nanoelectronics Workshop (SNW)*, 9-10 June 2019, **2019**.

[203] J. Seo, J. H. Lee, J. Pak, K. Cho, J. K. Kim, J. Kim, J. Jang, H. Ahn, S. C. Lim, S. Chung, K. Kang, T. Lee, *ADV. SCI.* **2021**, 8.

[204] L. Ansari, S. Monaghan, N. McEvoy, C. Ó. Coileáin, C. P. Cullen, J. Lin, R. Siris, T. Stimpel-Lindner, K. F. Burke, G. Mirabelli, R. Duffy, E. Caruso, R. E. Nagle, G. S. Duesberg, P. K. Hurley, F. Gity, *npj 2D Mater. Appl.* **2019**, 3, 33.

[205] X. Wang, B. Cheng, D. Reid, A. Pender, P. Asenov, C. Millar, A. Asenov, *IEEE Trans. Electron Devices* **2015**, 62, 3139.

[206] G. Hills, J. Zhang, M. M. Shulaker, H. Wei, C. S. Lee, A. Balasingam, H. S. P. Wong, S. Mitra, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* **2015**, 34, 1082.

[207] L. H. Brendler, A. L. Zimpeck, C. Meinhardt, R. A. L. Reis, *Microelectronics Reliability* **2019**, 100-101, 113448.

[208] G. Hills, C. Lau, A. Wright, S. Fuller, M. D. Bishop, T. Srimani, P. Kanhaiya, R. Ho, A. Amer, Y. Stein, D. Murphy, Arvind, A. Chandrakasan, M. M. Shulaker, *Nature* **2019**, 572, 595.

[209] International Roadmap for Devices and Systems (IEEE, 2021); https://irds.ieee.org/editions/2021

[210] B. Radisavljevic, M. B. Whitwick, A. Kis, *ACS Nano* **2011**, 5, 9934.

[211] H. Wang, L. Yu, Y.-H. Lee, Y. Shi, A. Hsu, M. L. Chin, L.-J. Li, M. Dubey, J. Kong, T. Palacios, *Nano Lett.* **2012**, 12, 4674.

[212] M. Zhao, Y. Ye, Y. Han, Y. Xia, H. Zhu, S. Wang, Y. Wang, D. A. Muller, X. Zhang, *Nat. Nanotechnol.* **2016**, 11, 954.

[213] X. Chen, Y. Xie, Y. Sheng, H. Tang, Z. Wang, Y. Wang, Y. Wang, F. Liao, J. Ma, X. Guo, *Nat. Commun.* **2021**, 12, 1.

[214] N. Li, Q. Wang, C. Shen, Z. Wei, H. Yu, J. Zhao, X. Lu, G. Wang, C. He, L. Xie, *Nat. Electron.* **2020**, 3, 711.

[215] S. Chen, M. R. Mahmoodi, Y. Shi, C. Mahata, B. Yuan, X. Liang, C. Wen, F. Hui, D. Akinwande, D. B. Strukov, M. Lanza, *Nat. Electron.* **2020**, 3, 638.

[216] D. Son, S. I. Chae, M. Kim, M. K. Choi, J. Yang, K. Park, V. S. Kale, J. H. Koo, C. Choi, M. Lee, J. H. Kim, T. Hyeon, D. H. Kim, *Adv. Mater.* **2016**, 28, 9326.

[217] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, A. Kis, *Nat. Nanotechnol.* **2011**, 6, 147.

[218] H. Wang, L. Yu, Y. H. Lee, Y. Shi, A. Hsu, M. L. Chin, L. J. Li, M. Dubey, J. Kong, T. Palacios, *Nano Lett.* **2012**, 12, 4674.

[219] X. Chen, Y. Xie, Y. Sheng, H. Tang, Z. Wang, Y. Wang, Y. Wang, F. Liao, J. Ma, X. Guo, L. Tong, H. Liu, H. Liu, T. Wu, J. Cao, S. Bu, H. Shen, F. Bai, D. Huang, J. Deng, A. Riaud, Z. Xu, C. Wu, S. Xing, Y. Lu, S. Ma, Z. Sun, Z. Xue, Z. Di, X. Gong, D. W. Zhang, P. Zhou, J. Wan, W. Bao, *Nat. Commun.* **2021**, 12, 5953.

[220] K. S. Novoselov, A. K. Geim, S. V. Morozov, D.-e. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, A. A. Firsov, *Science* **2004**, 306, 666.

[221] G. Li, Y.-Y. Zhang, H. Guo, L. Huang, H. Lu, X. Lin, Y.-L. Wang, S. Du, H.-J. Gao, *Chem. Soc. Rev.* **2018**, 47, 6073.

[222] W. Yao, B. Wu, Y. Liu, *ACS nano* **2020**, 14, 9320.

[223] A. Gupta, T. Sakthivel, S. Seal, *Progress in Materials Science* **2015**, 73, 44.

[224] P. R. Somani, S. P. Somani, M. Umeno, *Chem. Phys. Lett.* **2006**, 430, 56.

[225] X. Li, W. Cai, J. An, S. Kim, J. Nah, D. Yang, R. Piner, A. Velamakanni, I. Jung, E. Tutuc, *Science* **2009**, 324, 1312.

[226] K. S. Kim, Y. Zhao, H. Jang, S. Y. Lee, J. M. Kim, K. S. Kim, J. H. Ahn, *Nature* **2009**, 457, 706.

[227] X. Li, C. W. Magnuson, A. Venugopal, R. M. Tromp, J. B. Hannon, E. M. Vogel, L. Colombo, R. S. Ruoff, *JACS* **2011**, 133, 2816.

[228] N. Liu, L. Fu, B. Dai, K. Yan, X. Liu, R. Zhao, Y. Zhang, Z. Liu, *Nano Lett.* **2011**, 11, 297.

[229] T. Wu, G. Ding, H. Shen, H. Wang, L. Sun, D. Jiang, X. Xie, M. Jiang, *Adv. Funct. Mater.* **2013**, 23, 198.

[230] Y. Hao, M. S. Bharathi, L. Wang, Y. Liu, H. Chen, S. Nie, X. Wang, H. Chou, C. Tan, B. Fallahazad, *Science* **2013**, 342, 720.

[231] J. Li, X.-Y. Wang, X.-R. Liu, Z. Jin, D. Wang, L.-J. Wan, *J. Mater. Chem. C* **2015**, 3, 3530.

[232] T. Wu, X. Zhang, Q. Yuan, J. Xue, G. Lu, Z. Liu, H. Wang, H. Wang, F. Ding, Q. Yu, *Nat. Mater.* **2016**, 15, 43.

[233] B. Deng, Z. Pang, S. Chen, X. Li, C. Meng, J. Li, M. Liu, J. Wu, Y. Qi, W. Dang, *ACS nano* **2017**, 11, 12337.

[234] X. Xu, Z. Zhang, J. Dong, D. Yi, J. Niu, M. Wu, L. Lin, R. Yin, M. Li, J. Zhou, *Science bulletin* **2017**, 62, 1074.

[235] T. Wang, P. Li, X. Hu, M. Gao, Z. Di, Z. Xue, M. Zhang, *Appl. Surf. Sci.* **2020**, 529, 147066.

[236] P. Li, W. Wei, M. Zhang, Y. Mei, P. K. Chu, X. Xie, Q. Yuan, Z. Di, *Nano Today* **2020**, 34, 100908.

[237] L. Sun, B. Chen, W. Wang, Y. Li, X. Zeng, H. Liu, Y. Liang, Z. Zhao, A. Cai, R. Zhang, *ACS nano* **2021**.

[238] J. Li, M. Chen, A. Samad, H. Dong, A. Ray, J. Zhang, X. Jiang, U. Schwingenschlögl, J. Domke, C. Chen, *Nat. Mater.* **2022**, 1.

[239] Y. H. Lee, X. Q. Zhang, W. Zhang, M. T. Chang, C. T. Lin, K. D. Chang, Y. C. Yu, J. T. W. Wang, C. S. Chang, L. J. Li, *Adv. Mater.* **2012**, 24, 2320.

[240] K.-K. Liu, W. Zhang, Y.-H. Lee, Y.-C. Lin, M.-T. Chang, C.-Y. Su, C.-S. Chang, H. Li, Y. Shi, H. Zhang, *Nano Lett.* **2012**, 12, 1538.

[241] A. M. Van Der Zande, P. Y. Huang, D. A. Chenet, T. C. Berkelbach, Y. You, G.-H. Lee, T. F. Heinz, D. R. Reichman, D. A. Muller, J. C. Hone, *Nat. Mater.* **2013**, 12, 554.

[242] J. Zhang, H. Yu, W. Chen, X. Tian, D. Liu, M. Cheng, G. Xie, W. Yang, R. Yang, X. Bai, *ACS nano* **2014**, 8, 6024.

[243] W. Chen, J. Zhao, J. Zhang, L. Gu, Z. Yang, X. Li, H. Yu, X. Zhu, R. Yang, D. Shi, *JACS* **2015**, 137, 15632.

[244] S. Wang, X. Wang, J. H. Warner, *ACS nano* **2015**, 9, 5246.

[245] K. Kang, S. Xie, L. Huang, Y. Han, P. Y. Huang, K. F. Mak, C.-J. Kim, D. Muller, J. Park, *Nature* **2015**, 520, 656.

[246] J. J. Pyeon, S. H. Kim, D. S. Jeong, S.-H. Baek, C.-Y. Kang, J.-S. Kim, S. K. Kim, *Nanoscale* **2016**, 8, 10792.

[247] D. Fu, X. Zhao, Y.-Y. Zhang, L. Li, H. Xu, A. R. Jang, S. I. Yoon, P. Song, S. M. Poh, T. Ren, *JACS* **2017**, 139, 9392.

[248] P. Yang, S. Zhang, S. Pan, B. Tang, Y. Liang, X. Zhao, Z. Zhang, J. Shi, Y. Huan, Y. Shi, *ACS nano* **2020**, 14, 5036.

[249] J. Li, S. Wang, Q. Jiang, H. Qian, S. Hu, H. Kang, C. Chen, X. Zhan, A. Yu, S. Zhao, *Small* **2021**, 17, 2100743.

[250] X. Feng, S. Li, S. L. Wong, S. Tong, L. Chen, P. Zhang, L. Wang, X. Fong, D. Chi, K.-W. Ang, *ACS Nano* **2021**, 15, 1764.

[251] T. Li, W. Guo, L. Ma, W. Li, Z. Yu, Z. Han, S. Gao, L. Liu, D. Fan, Z. Wang, *Nat. Nanotechnol.* **2021**, 16, 1201.

[252] Y. Gao, Y. L. Hong, L. C. Yin, Z. Wu, Z. Yang, M. L. Chen, Z. Liu, T. Ma, D. M. Sun, Z. Ni, *Adv. Mater.* **2017**, 29, 1700990.

[253] Y. Gao, Z. Liu, D.-M. Sun, L. Huang, L.-P. Ma, L.-C. Yin, T. Ma, Z. Zhang, X.-L. Ma, L.-M. Peng, *Nat. Commun.* **2015**, 6, 1.

[254] J. Chen, X. Zhao, S. J. R. Tan, H. Xu, B. Wu, B. Liu, D. Fu, W. Fu, D. Geng, Y. Liu, *JACS* **2017**, 139, 1073.

[255] X. Xu, Y. Pan, S. Liu, B. Han, P. Gu, S. Li, W. Xu, Y. Peng, Z. Han, J. Chen, *Science* **2021**, 372, 195.

[256] Z. Wu, Y. Lyu, Y. Zhang, R. Ding, B. Zheng, Z. Yang, S. P. Lau, X. H. Chen, J. Hao, *Nat. Mater.* **2021**, 20, 1203.

[257] J. S. Lee, S. H. Choi, S. J. Yun, Y. I. Kim, S. Boandoh, J.-H. Park, B. G. Shin, H. Ko, S. H. Lee, Y.-M. Kim, *Science* **2018**, 362, 817.

[258] L. Wang, X. Xu, L. Zhang, R. Qiao, M. Wu, Z. Wang, S. Zhang, J. Liang, Z. Zhang, Z. Zhang, W. Chen, X. Xie, J. Zong, Y. Shan, Y. Guo, M. Willinger, H. Wu, Q. Li, W. Wang, P. Gao, S. Wu, Y. Zhang, Y. Jiang, D. Yu, E. Wang, X. Bai, Z.-J. Wang, F. Ding, K. Liu, *Nature* **2019**, 570, 91.

[259] T.-A. Chen, C.-P. Chuu, C.-C. Tseng, C.-K. Wen, H. S. P. Wong, S. Pan, R. Li, T.-A. Chao, W.-C. Chueh, Y. Zhang, *Nature* **2020**, 579, 219.

[260] X. Li, W. Cai, J. An, S. Kim, J. Nah, D. Yang, R. Piner, A. Velamakanni, I. Jung, E. Tutuc, S*cience* **2009**, 324, 1312.

[261] K. S. Kim, Y. Zhao, H. Jang, S. Y. Lee, J. M. Kim, K. S. Kim, J.-H. Ahn, P. Kim, J.-Y. Choi, B. H. Hong, *nature* **2009**, 457, 706.

[262] S. Li, M.-E. Pam, Y. Li, L. Chen, Y.-C. Chien, X. Fong, D. Chi, K.-W. Ang, *Adv. Mater.* **2021**, n/a, 2103376.

[263] Y.-M. Lin, A. Valdes-Garcia, S.-J. Han, D. B. Farmer, I. Meric, Y. Sun, Y. Wu, C. Dimitrakopoulos, A. Grill, P. Avouris, *Science* **2011**, 332, 1294.

[264] Y. M. Lin, C. Dimitrakopoulos, K. A. Jenkins, D. B. Farmer, H. Y. Chiu, A. Grill, P. Avouris, *Science* **2010**, 327, 662.

[265] R. Cheng, J. Bai, L. Liao, H. Zhou, Y. Chen, L. Liu, Y.-C. Lin, S. Jiang, Y. Huang, X. Duan, *Proc. Natl. Acad. Sci.* **2012**, 109, 11588.

[266] S.-J. Han, A. V. Garcia, S. Oida, K. A. Jenkins, W. Haensch, *Nat. Commun.* **2014**, 5, 1.

[267] S. Goossens, G. Navickaite, C. Monasterio, S. Gupta, J. J. Piqueras, R. Pérez, G. Burwell, I. Nikitskiy, T. Lasanta, T. Galán, *Nat. Photonics* **2017**, 11, 366.

[268] S. Wachter, D. K. Polyushkin, O. Bethge, T. Mueller, *Nat. Commun.* **2017**, 8, 1.

[269] Z. Lin, Y. Liu, U. Halim, M. Ding, Y. Liu, Y. Wang, C. Jia, P. Chen, X. Duan, C. Wang, *Nature* **2018**, 562, 254.

[270] S. Zeng, C. Liu, X. Huang, Z. Tang, L. Liu, P. Zhou, *Nat. Commun.* **2022**, 13, 1.

[271] Y. J. Park, B. K. Sharma, S. M. Shinde, M.-S. Kim, B. Jang, J.-H. Kim, J.-H. Ahn, *ACS Nano* **2019**, 13, 3023.

[272] M. Choi, J. Park Yong, K. Sharma Bhupendra, S.-R. Bae, Y. Kim Soo, J.-H. Ahn, *Sci. Adv.*, 4, eaas8721.

[273] D. K. Polyushkin, S. Wachter, L. Mennel, M. Paur, M. Paliy, G. Iannaccone, G. Fiori, D. Neumaier, B. Canto, T. Mueller, *Nat. Electron.* **2020**, 3, 486.

[274] X. Chen, Y. Xie, Y. Sheng, H. Tang, Z. Wang, Y. Wang, Y. Wang, F. Liao, J. Ma, X. Guo, L. Tong, H. Liu, H. Liu, T. Wu, J. Cao, S. Bu, H. Shen, F. Bai, D. Huang, J. Deng, A. Riaud, Z. Xu, C. Wu, S. Xing, Y.

Lu, S. Ma, Z. Sun, Z. Xue, Z. Di, X. Gong, D. W. Zhang, P. Zhou, J. Wan, W. Bao, *Nat. Commun.* **2021**, 12, 5953.

[275] L. Li, Y. Yu, G. J. Ye, Q. Ge, X. Ou, H. Wu, D. Feng, X. H. Chen, Y. Zhang, *Nat. Nanotechnol.* **2014**, 9, 372.

[276] L. Chen, S. Li, X. Feng, L. Wang, X. Huang, B. C. K. Tee, K. W. Ang, *Adv. Electron. Mater.* **2018**, 4, 1800274.

[277] Y. Liu, K.-W. Ang, *ACS nano* **2017**, 11, 7416.

[278] J. Wu, H. Yuan, M. Meng, C. Chen, Y. Sun, Z. Chen, W. Dang, C. Tan, Y. Liu, J. Yin, *Nat. Nanotechnol.* **2017**, 12, 530.

[279] T. Li, H. Peng, *Acc. Mater. Res.* **2021**, 2, 842.

[280] T. Li, T. Tu, Y. Sun, H. Fu, J. Yu, L. Xing, Z. Wang, H. Wang, R. Jia, J. Wu, *Nat. Electron.* **2020**, 3, 473.

[281] C. Tan, M. Tang, J. Wu, Y. Liu, T. Li, Y. Liang, B. Deng, Z. Tan, T. Tu, Y. Zhang, *Nano Lett.* **2019**, 19, 2148.

[282] K. Zhu, C. Wen, A. A. Aljarb, F. Xue, X. Xu, V. Tung, X. Zhang, H. N. Alshareef, M. Lanza, *Nat. Electron.* **2021**, 4, 775.

[283] S. Das, A. Sebastian, E. Pop, C. J. McClellan, A. D. Franklin, T. Grasser, T. Knobloch, Y. Illarionov, A. V. Penumatcha, J. Appenzeller, *Nat. Electron.* **2021**, 4, 786.

[284] D. S. Schulman, A. J. Arnold, S. Das, *Chem. Soc. Rev.* **2018**, 47, 3037.

[285] Y. Zheng, J. Gao, C. Han, W. Chen, *Cell Rep. Phys. Sci.* **2021**, 2, 100298.

[286] X. Song, Z. Guo, Q. Zhang, P. Zhou, W. Bao, D. W. Zhang, *Small* **2017**, 13, 1700098.

[287] S. Das, A. Sebastian, E. Pop, C. J. McClellan, A. D. Franklin, T. Grasser, T. Knobloch, Y. Illarionov, A. V. Penumatcha, J. Appenzeller, Z. Chen, W. Zhu, I. Asselberghs, L.-J. Li, U. E. Avci, N. Bhat, T. D. Anthopoulos, R. Singh, *Nat. Electron.* **2021**, 4, 786.

[288] Z. Wang, H. Xia, P. Wang, X. Zhou, C. Liu, Q. Zhang, F. Wang, M. Huang, S. Chen, P. Wu, Y. Chen, J. Ye, S. Huang, H. Yan, L. Gu, J. Miao, T. Li, X. Chen, W. Lu, P. Zhou, W. Hu, *Adv. Mater.* **2021**, 33, 2104942.

[289] T. Knobloch, Y. Y. Illarionov, F. Ducry, C. Schleich, S. Wachter, K. Watanabe, T. Taniguchi, T. Mueller, M. Waltl, M. Lanza, M. I. Vexler, M. Luisier, T. Grasser, *Nat. Electron.* **2021**, 4, 98.

[290] W. Li, J. Zhou, S. Cai, Z. Yu, J. Zhang, N. Fang, T. Li, Y. Wu, T. Chen, X. Xie, H. Ma, K. Yan, N. Dai, X. Wu, H. Zhao, Z. Wang, D. He, L. Pan, Y. Shi, P. Wang, W. Chen, K. Nagashio, X. Duan, X. Wang, *Nat. Electron.* **2019**, 2, 563.

[291] Y. Y. Illarionov, A. G. Banshchikov, D. K. Polyushkin, S. Wachter, T. Knobloch, M. Thesberg, L. Mennel, M. Paur, M. Stöger-Pollach, A. Steiger-Thirsfeld, M. I. Vexler, M. Waltl, N. S. Sokolov, T. Mueller, T. Grasser, *Nat. Electron.* **2019**, 2, 230.

[292] T. Li, T. Tu, Y. Sun, H. Fu, J. Yu, L. Xing, Z. Wang, H. Wang, R. Jia, J. Wu, C. Tan, Y. Liang, Y. Zhang, C. Zhang, Y. Dai, C. Qiu, M. Li, R. Huang, L. Jiao, K. Lai, B. Yan, P. Gao, H. Peng, *Nat. Electron.* **2020**, 3, 473.

[293] B. A. Holler, K. Crowley, M.-H. Berger, X. P. A. Gao, *Adv. Electron. Mater.* **2020**, 6, 2000635.

[294] G. Iannaccone, F. Bonaccorso, L. Colombo, G. Fiori, *Nat. Nanotechnol.* **2018**, 13, 183.

[295] G. Migliato Marega, Y. Zhao, A. Avsar, Z. Wang, M. Tripathi, A. Radenovic, A. Kis, *Nature* **2020**, 587, 72.

He Tian received the Ph.D. degree from the Institute of Microelectronics, Tsinghua University, in 2015. He is currently an Associate Professor at School of Integrated Circuits in Tsinghua University. He has co-authored over 150 papers and has over 5000 citations. He has been researching on two-dimensional materials-based nanoscale transistors, sensors/actuators and resistive memory devices.

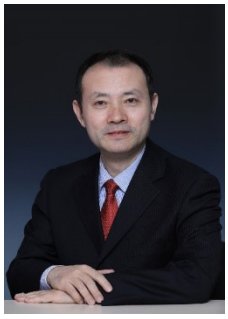
Yang Shen is currently a PhD student under the supervision of Prof. He Tian at the School of Integrated Circuits, Tsinghua University. His research focuses on devices based on 2D materials.

Zuo-Yuan Dong is currently a PhD student under the supervision of Prof. Xing Wu at the School of Communication and Electronic Engineering, East China Normal University (ECNU). His research interests focus mainly on 2D materials and their devices.

Ya-Bin Sun received the B.S. degree in electrical engineering from Jilin University, Changchun, China, in 2010, and the Ph.D. degree in electrical engineering from Tsinghua University, Beijing, China, in 2015. He is currently a associate Professor with electrical engineering of East China Normal University. His main research interests focus on design, characterization, and modeling of advanced nanoelectronic devices.

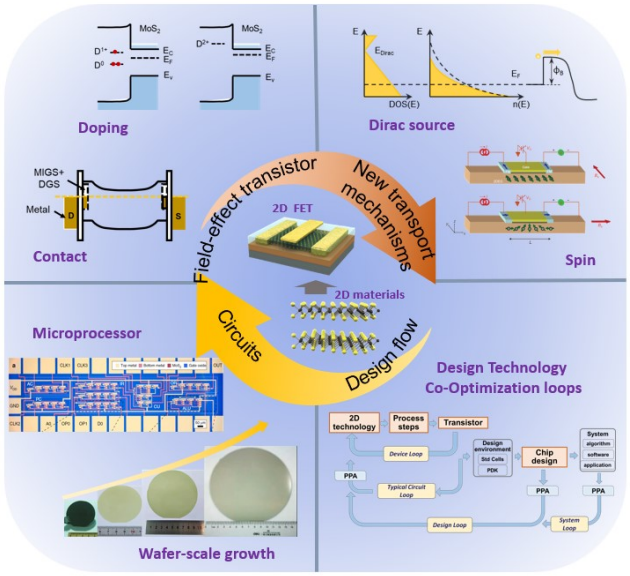
Hao Guo received his Ph.D. degree in Instrument Science and Technology from North University of China, Taiyuan, China, in 2016, where he has been a full professor with the Instrument Science and Technology since 2021. His main research interests include micro-nano optical quantum sensing and precision measurement, micro-nano manufacturing and intelligent sensors.

Xing Wu received her bachelor's degree in Electrical Engineering from Xi'an Jiaotong University (XJTU) China in 2008 and her Ph.D. degree from Nanyang Technological University (NTU) Singapore in 2012. She is currently a professor at East China Normal University (ECNU) China. Her research interests are in situ TEM characterization of advanced electronic materials, and the reliability study of electronic devices.



Tian-Ling Ren received his Ph.D. degree in solid-state physics from the Department of Modern Applied Physics, Tsinghua University, Beijing, China, in 1997, where he has been a Full Professor

with the Institute of Microelectronics since 2003. His main research interests include 2D material-based devices and novel nanoelectronic devices, intelligent sensors and integrated micro-electromechanical systems, and critical technology for advanced micro- and nanoelectronics.



Two-dimensional materials show great potential to enable the transistor scaling down below 1 nm node. This review focus on the introduction of the optimization of 2D materials-based transistor, new mechanisms, design flow and circuits, which indicate the trend of 2D transistors towards very large-scale integrated circuits.