

The Past, the Present, and the Future of Ferroelectric Memories

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(Invited Paper)

Abstract—Ferroelectric materials are characterized by two stable polarization states that can be switched from one to another by applying an electrical field. As one of the most promising effects to realize nonvolatile memories (NVMs), the application of ferroelectrics in NVMs has been studied since the 1950s. In principle, three different ways to read out the ferroelectric polarization are known: measuring the charge-related current that flows during switching of the ferroelectric, measuring the polarization-dependent tunneling current in very thin ferroelectric layers, and measuring the threshold voltage shift of a ferroelectric field effect transistor caused by the polarization change of the ferroelectric integrated into the gate stack. While early attempts used bulk ferroelectric crystals, the first commercial success was reached when the concept was integrated into a MOS process. However, all materials that were known to exhibit ferroelectricity had a very complicated structure, thus making the integration troublesome and leading to a very slow scaling and limiting its application to niche markets. With the discovery of ferroelectricity in hafnium oxide in 2011, the new impetus came into the field for all three variants described above. This article will describe the history of ferroelectric memories and its current status both with respect to the commercialization of ferroelectric memories based on traditional ferroelectric materials and the ongoing research and development activities employing the more recently discovered ferroelectricity in hafnium oxide. This finally leads us to an outlook of the future challenges for ferroelectric memories.

Index Terms—Barium titanate, CMOS, ferroelectric field effect transistor (FeFET), ferroelectric random access memory (FeRAM), ferroelectric tunnel junction (FTJ), ferroelectrics hafnium oxide, lead zirconium titanate (PZT), perovskites.

I. INTRODUCTION

FERROELECTRIC materials are characterized by two stable polarization states at zero electrical field that can be switched from one value to the other by applying an electrical field that is larger than the coercive field E_C [1], [2]. The coercive field E_C is the field at which the effective ferroelectric polarization is zero. A ferroelectric can be characterized by

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the hysteresis curve of the polarization P or the displacement field D as a function of the electrical field E , as illustrated in Fig. 1(a). The remanent polarization typically results from the displacement of certain ions from the position that is required for charge neutrality. Therefore, ferroelectricity requires that the material will not be centrosymmetric. In inorganic ferroelectrics, e.g., those having the perovskite structure such as lead zirconium titanate (PZT) or barium titanate (BTO) or a layered perovskite structure such as strontium bismuth tantalite (SBT), one central ion can switch between two stable positions [see Fig. 1(b)]. In organic ferroelectrics such as polyvinylidene fluoride (PVDF) that is typically copolymerized with tetrafluoroethylene (TRFE) to stabilize the ferroelectric β phase, the polar polymer chains constitute the dipole and are assumed to rotate during switching [see Fig. 1(c)]. Finally, in fluoride structure ferroelectrics such as the ferroelectric orthorhombic phase in hafnium oxide, the oxygen ions can switch between two stable positions [see Fig. 1(d)]. When implementing a ferroelectric material as the active material into a memory cell, different readout mechanisms are possible. First, the charge during the switching or nonswitching operation can be used [2]–[4]. For these, a capacitor having the ferroelectric material as the dielectric can be biased in a certain direction. As a result, the ferroelectric will not switch if it was previously polarized in the same direction and it will switch if it was polarized in the opposite direction. In the latter case, free charge attached on both electrodes to compensate for the polarization charge will be released by opposite switching, and this extra charge will be transferred, thus leading to a higher current flow in the outer circuit. This capacitor-based readout scheme, therefore, destroys the stored information, and a write-back is necessary. This readout scheme is used in ferroelectric random access memories (FeRAMs).

Second, the ferroelectric can be implemented as part of the gate dielectric of a ferroelectric field effect transistor (FeFET) [4]. The polarization will lead to a shift of the I – V curve of the transistor that can be used to determine the state of the ferroelectric polarization in a nondestructive way. Finally, for thin ferroelectrics [5] or a double-layer structure of a ferroelectric combined with a thin tunneling layer [6], the polarization state of the ferroelectric can be directly read out as the current flowing through the capacitor. This approach is referred to as a ferroelectric tunnel junction (FTJ). Again, this is a nondestructive readout scheme. Among these three possibilities, the first option is the one that has received the most attention and can be found in low-volume products on the market [7], [8]. The second has also received

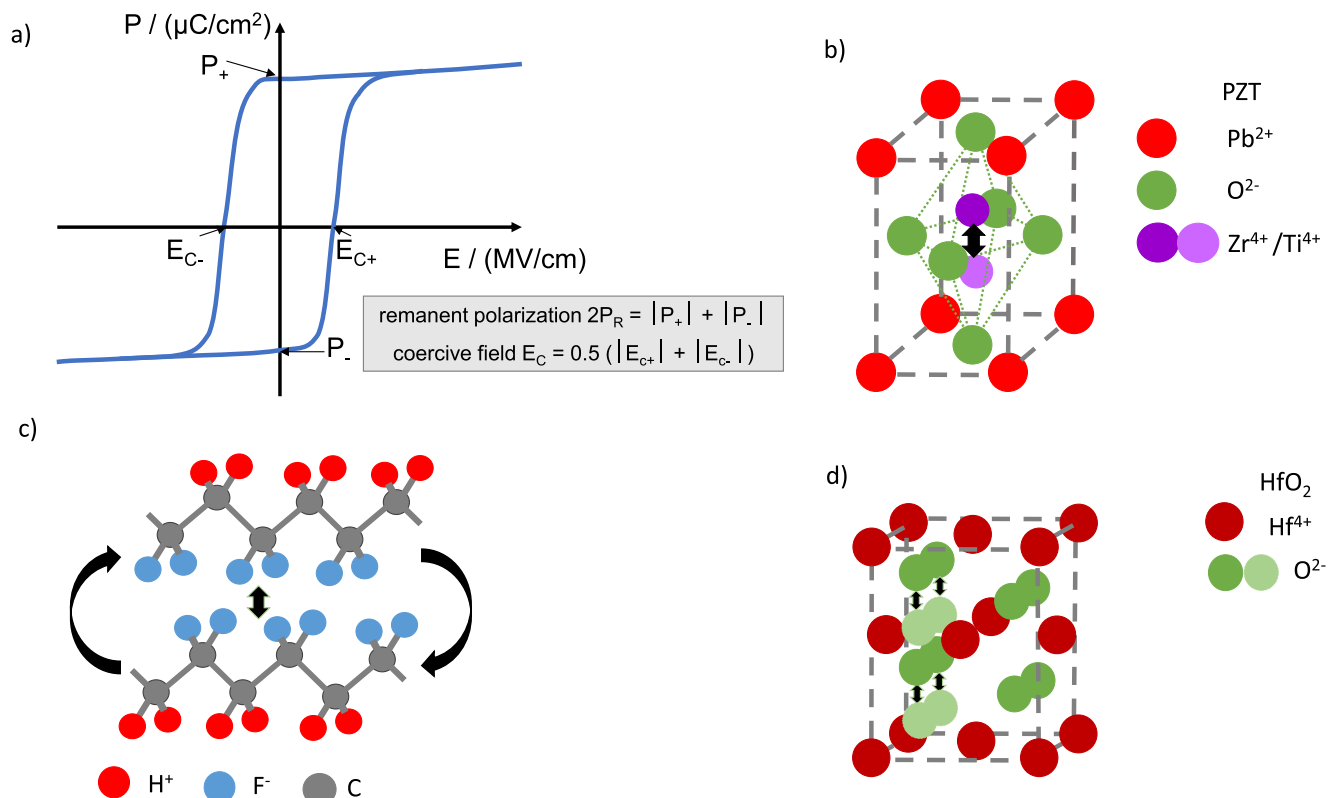


Fig. 1. Ferroelectric hysteresis and typical ferroelectric crystals. (a) Typical hysteresis curve of a ferroelectric material showing the most important properties remanent polarization and coercive field. (b) Sketch of a PZT crystal showing the two stable positions of a central Zr^{4+} or Ti^{4+} ion. (c) Sketch of a PVDF polymer chain with the two orientations that can generate the ferroelectric polarization. (d) Sketch of an orthorhombic hafnium oxide crystal indicating the switching of O_2 -oxygen ions in the crystal.

considerable attention, but recently, the unavoidable depolarization field in the FET gate stack [9] together with the low coercive field of classical ferroelectrics has hindered the commercial success of such devices. Finally, reading out the tunneling current in very thin ferroelectrics is a rather new approach that is still in the basic research phase. In the following, we will explore the history and status of all three variants.

II. CAPACITOR-BASED FERROELECTRIC MEMORIES

Looking at the hysteresis curve of Fig. 1, it becomes clear that ferroelectric materials, with their field-driven switching mechanism and two stable polarization states, will be very well-suited for nonvolatile memories (NVMs). The first attempts to realize a memory element based on a ferroelectric material therefore date back to the 1950s. The first proposal of nonvolatile ferroelectric memory goes back to Buck [10], who reported a ferroelectric memory concept in his master's thesis. This inspired some other researchers to explore these possibilities [11]–[13]. The main concept is schematically depicted in Fig. 2(a). A BTO crystal was used, and electrodes were evaporated on both sides of the crystal leading to a cross-point arrangement of memory cells that are formed at each position, where two of the electrodes cross each other with the ferroelectric in-between. However, the nonideality of the hysteresis together with the low quality of the ferroelectric materials made it impossible to avoid disturbs in the cross-point array [7]. In the 1980s, the vision of a ferroelectric memory was revived. At that time, MOS technology was available, thus making it possible to add a select transistor to avoid disturbs

and minimize the parasitic bitline capacitance in the read path. Moreover, advanced deposition techniques made material optimization feasible [14], [15]. The idea was to integrate a ferroelectric capacitor into the back end of the line of a MOS process and connect one electrode to a select transistor and the other one to the plate line. The simple version of this uses no special contact constructions and is known as the offset cell [see Fig. 2(c)]. In later versions, the bottom electrode of the capacitor was directly connected to the transistor leading to a stacked cell [16] as depicted in Fig. 2(d). Fig. 2(d) shows the so-called capacitor under bitline (CUB) approach. To save space, the capacitor over bitline (COB) approach that has replaced the CUB approach in dynamic random access memory (DRAM) can be implemented [17], [18]. This development inspired the dreams of replacing DRAM by ferroelectric memories [19], [20] or the development of a complete new class of memories that could replace both parts of the required random access memory and parts of the NVM [21]. However, although some important and exciting technologies have been developed (a nice overview can be found in [22]) and an impressive 130-nm technology reached the market [23], [24], the technology is far behind mainstream standalone memory technologies with respect to feature size and cost. With respect to reliability, however, excellent results were obtained in a 2T/2C configuration, as illustrated in Fig. 3 [25]. With a robust signal margin as the basis [Fig. 3(a)], the technology can deliver a high (essentially unlimited) cycling endurance [Fig. 3(b)] and very good retention with and without precycling (Fig. 3). These kinds of

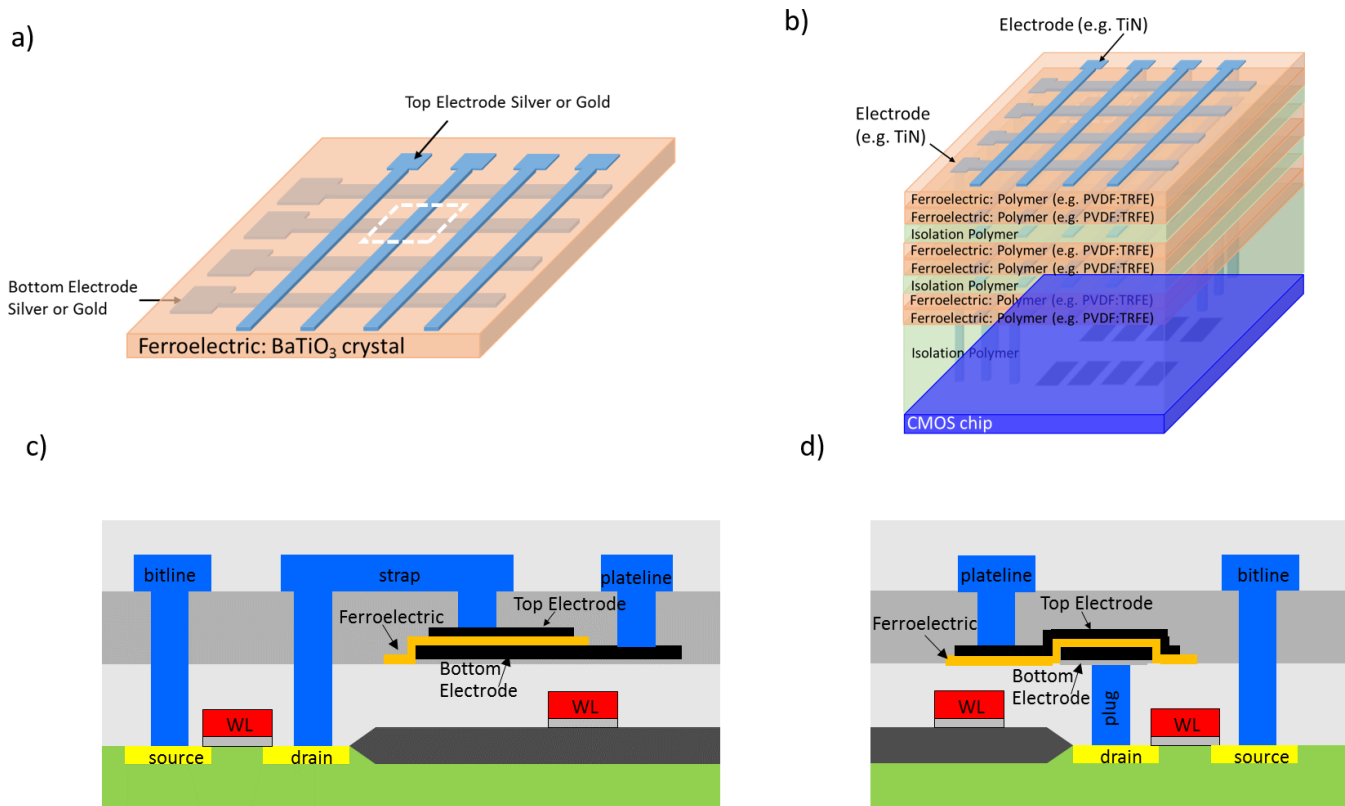


Fig. 2. Variants of capacitor-based memory cells. (a) Schematic of a small array section using cross-point cells based on BaTiO₃ crystals. This approach was explored in the 1950s. (b) Schematic of a small array section using a cross-point cell with ferroelectric polymers stacked on top of a CMOS base chip. This approach was explored in the late 1990s and the early 2000s. (c) Cross section of an offset cell using PZT or SBT ferroelectrics. This cell was the first to reach production in the 1990s. (d) Cross section of a stacked cell using PZT. This is the most advanced version commercially available today.

examples can illustrate that using ferroelectrics can result in reliable products. Both embedded and standalone memories are available combining RAM functionality with nonvolatility. However, the large technology feature sizes limit their applications to where these features are a necessary requirement. Typical applications are tasks such as data logging. For details to establish the FeRAM technology, the readers are referred to [25]–[27]. Another interesting cell variant is the chain FeRAM cell concept [22], where the select transistor and capacitor are connected in parallel and these elements are then connected in series to form a chain. Such an approach can reduce the plate-line and bitline capacitances and offers new possibilities for scaling [28]. Although an impressive 128-Mb demonstration was shown [29], this concept could not overcome the basic limitations of the integration challenges of the PZT ferroelectric used in that device. Perovskites such as the one illustrated in Fig. 1(b) and even more layered perovskites such as SBT have a rather complicated crystal structure with the oxygen being weakly bound. This causes severe integration challenges both for SBT [30] and PZT [31] on the one side from bringing the ferroelectric into the correct crystal phase and on the other side with respect to the negative influence of the annealing in reducing environments like hydrogen [32]. While these issues slowed down the development, they could still be solved. However, the charge-based sensing would require a 3-D capacitor below 100-nm ground rules [18], [22]. This problem could not be solved

in a satisfying way due to the difficulty of controlling the orientation of the PZT film on the sidewalls of the 3-D structure in small dimensions [33]. Therefore, toward the end of the first decade of the new millennium, the technology was assumed to be interesting only for niche applications.

In the late 1990s and the early 2000s, the idea of the cross-point memory was revived by a startup company from Sweden called Thin Film Electronics that was backed by INTEL at that time [34], [35]. What had changed that a ferroelectric memory based on a cross-point array seemed to be an option after it had failed back in the 1950s? First, one needs to consider that in the late 1990s and the early 2000s, NAND Flash was bringing semiconductor memories into the arena of nonvolatile mass storage rather than only addressing random access memories. This means that the targeted memory had a much lower endurance specification as well as a page architecture that would reduce the number of disturb cycles. Second, the ferroelectric material used was a polymer ferroelectric. Although the company never fully disclosed the material, it seems that the properties of the material were close to those of PVDF:TRFE [36]–[38]. As can be seen from Table I, the coercive field of this material is much higher than that of traditional inorganic ferroelectrics such as PZT and SBT. This feature and the switching dynamics allowed to precisely tune the voltage to a value that can reduce disturbs as much as possible [36]–[38]. As a result, a memory where the drivers and other periphery circuits

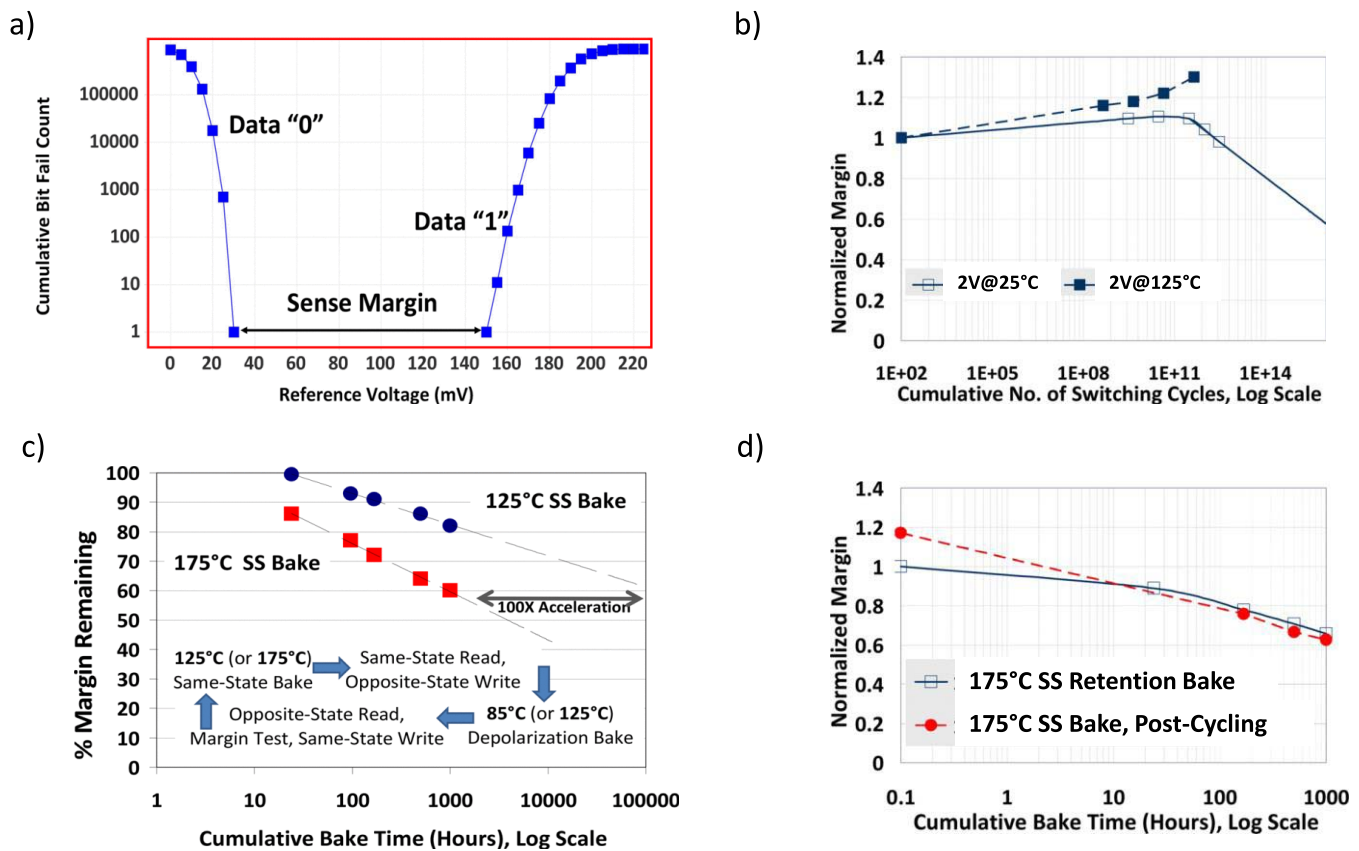


Fig. 3. Reliability data of PZT-based ferroelectric 2T-2C memory integrated into a 180-nm process reproduced from [25]. (a) Bit distribution for a 448-kb array taken at 1.65 V showing the sense margin. (b) Endurance cycling at 2 V for both room temperature (average of 100 packaged units) and 125 °C (average of 54 units). (c) Remaining window as a function of 125 °C (average of 84 packaged units) and 175 °C (average of 249 units) cumulative bake time. Inset: a compact version of the retention test flow. (d) Average signal margin as a function of same state (SS) bake time at 175 °C for 249 non cycled units and 309 cycled units (cycled up to 4.5×10^8 cycles).

TABLE I

REMANENT POLARIZATION AND COERCIVE FIELD OF FERROELECTRIC THIN FILMS

Symbol	Property	unit	PZT	SBT	PVDF: TRFE	HfO ₂
$2 \cdot P_R$	Remanent Polarization	$\mu\text{C}/\text{cm}^2$	40-90	10-20	8-10	30-60
E_C	Coercive Field,	MV/cm	0.05	0.035-0.055	0.6	0.8-2
<i>Ref.</i>			[106] [106]	[106] [106] [106]	[38] [106]	[50]

¹ Typical values were extracted from the mentioned references. Detailed values for different processing conditions may be found in the references

would be placed on a silicon chip and several layers of cross-point ferroelectric matrices would be stacked on top [see Fig. 2(b)], seemed to be very attractive. However, as with any capacitor-based ferroelectric memory, the scaling of the cell is limited. Taking the somewhat smaller polarization of ferroelectric polymers on the one hand and the possibility of implementing a more precise sensing in a storage device that would need sensing speeds in the microseconds and not in the nanoseconds range, a minimum feature size of 90 nm seemed to be feasible [39]. The stacking of several layers will increase the economic benefit up to a number of about 6–12 layers.

Above that limit, the cost per bit will increase again [39], [40]. As a result, the technology was outpaced by the rapid NAND Flash development according to Hwang's law that described the very rapid areal density increase of NAND Flash in the early 2000s [41], and finally, it was discontinued. However, the concept of a polymer ferroelectric memory is still very interesting for memories within flexible electronic devices [42], but it will not be able to challenge mainstream semiconductor memories.

Therefore, capacitor-based memories seemed to have reached their limitations. This was changed by the discovery of ferroelectricity in hafnium oxide [43]. Since hafnium oxide is a well-established material in the semiconductor industry that is used as a high-*k* material in CMOS processes since 2007 [44], this discovery promises to overcome the basic issues. Indeed, the sensitivity to hydrogen is not a severe issue [45] and deposition into 3-D structures results in almost the full expected gain in signal [46]. However, the large coercive field as indicated in Table I leads to a high electrical field stress during endurance cycling, and therefore, improving this aspect has become a major research topic [47], [48]. Continuous progress has been made in the past years, and the details are beyond the scope of this article. However, here, we would like to mention an alternative approach to master this issue. It is well-established that the field-cycling endurance of antiferroelectric materials is much higher compared to their ferroelectric

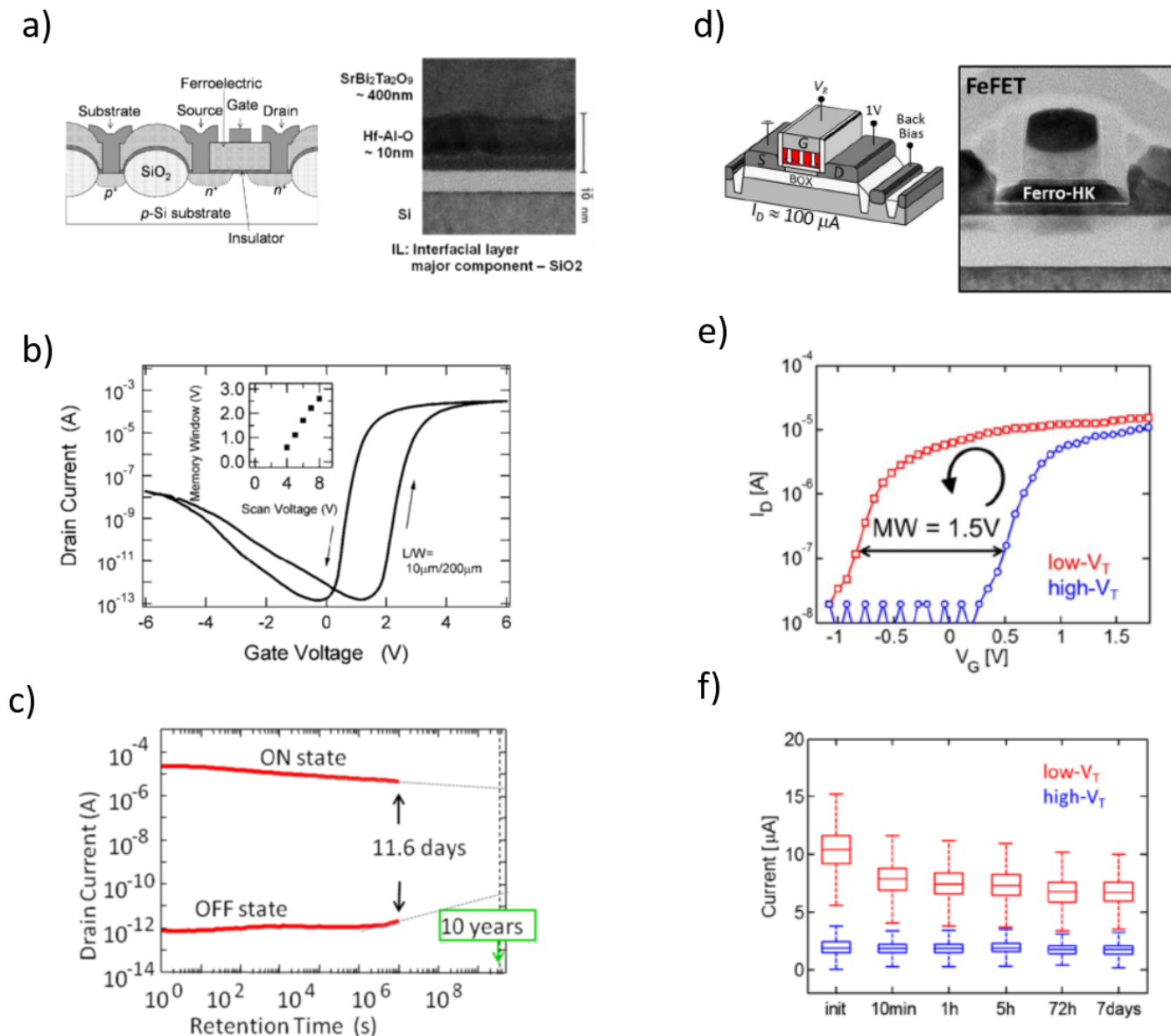


Fig. 4. FeFETs based on SBT and silicon-doped HfO₂. (a) Schematic cross section and TEM image of the gate stack of an SBT-based FeFET using HfAlO as the buffer layer. (b) *I*-*V* curves for the device shown in (a). (c) Room temperature retention measurement of the devices shown in (a). (d) Schematic cross sections and TEM cross section of a FeFET using silicon-doped HfO₂ integrated into GlobalFoundries' 22-nm fully depleted silicon on insulator (FDSOI) technology. (e) *I*-*V* curves of the device shown in the (f) retention measurement of 64-kbit array built from the device shown in (d) performed at 250 °C. Figures (a)–(c) are taken from [106]. Figures (d)–(f) are taken from [71].

counterparts [49]. For certain compositions in doped hafnium oxide or zirconium oxide, the antiferroelectric behavior can be reproducibly achieved [43], [50], [51]. In the concept of the antiferroelectric RAM (AFeRAM) [52], [53], a built-in bias field is used to shift the hysteresis, so that at 0-V applied bias, a nonvolatile state will exist that is absent in an antiferroelectric [54]. The voltage required to switch between the two states is reduced, and the switching is between one polarized state and one nonpolarized state, thus leading to lower switching voltage and better endurance [55]. This AFeRAM approach is still in its infancy, but it illustrates that there are plenty of ideas on the table to solve the remaining issues of making the new class of hafnium oxide-based ferroelectric materials ready to finally realize the dream of a nonvolatile version of a DRAM.

III. FeFETs

When the ferroelectric is integrated into the gate stack of a field effect transistor to realize a FeFET [see Fig. 4(a) and (d)], in principle, two basic limitations of the capacitor-based solution can be overcome. First, the read becomes nondestructive, and second, the device does not require a 3-D integration since the FET is sensitive to the charge per area that is maintained during scaling. The idea of building such a device dates back to the year 1957 [56], and a first realization was shown a few years after that [57]. As a result, the idea seems to be very intriguing, and consequently, many research activities were focused on the topic. A very good overview can be found in [58]. The work focused on three main challenges for about four decades:

- 1) creating a clean interface to the semiconductor in the metal–ferroelectric–semiconductor (MFS) structure;
- 2) avoiding a large depolarization field to realize ten years of data retention since the large permittivity (several 100 s for perovskite ferroelectrics) in series with the depletion layer (and a possible interface layer see below) of the semiconductor is unfavorable;
- 3) realizing a high (practically unlimited) endurance in a one-transistor-based memory array.

The last issue number three can be treated very generally here. For a long time, it was the sole goal of semiconductor memories to realize the random access memory application; unlimited endurance was required. With the establishment of Flash memories as NVMs with much lower write endurance requirements in the range of 10^5 , this boundary condition—as in Flash memory—seems to be achievable although little experimental data are available here due to the dominating issue number two.

Many different material options have been tried out. While issue one can be overcome by adding an interface layer between the semiconductor channel [59] and the ferroelectric or even splitting up the complete capacitor stack into a MOS capacitor and an MFS capacitor connected in series [60], this exacerbates issue two. Considerable work was then focused on using different materials for the interface oxide. Therefore, this issue was the dominant research topic for many years, and it seemed almost unsolvable in the early 2000s [9]. From the analysis in [9], we can learn that two aspects will help. First, the dielectric constant of the ferroelectric needs to be as low as possible and the dielectric constant of the interface layer should be high to achieve a favorable voltage divider. Second, a high coercive field helps to stabilize the stored state. Several alternative material options for the ferroelectric have been tried over the years. Barium magnesium fluoride (BaMgF_4) and bismuth titanate ($\text{Bi}_4\text{Ti}_3\text{O}_{12}$) [61] were used to overcome the issue number one in a time where GaAs-based devices were considered a very interesting option for the future and GaAs was also considered as possible semiconductor platform to realize memories. Polymer ferroelectrics have a very low permittivity on the order of 2, and a rather high coercive field (see Table I) seems to be very well suited to tackle both issues one and two. Promising devices have been fabricated only ten years ago [62] since it took quite a while to optimize the material properties (see the chapter on capacitor-based memories). However, integrating a polymer into the gate stack of FeFET is not possible due to the limited thermal budget; the material can withstand after deposition. Therefore, this is again a path available to organic electronics only. The attempt of utilizing rare Earth-based ferroelectrics such as CeMnO_3 with permittivity values below ten was proposed by Cova Inc., Miami, FL, USA, in the early 2000 s [63] and never produced notable results. Therefore, the attention went back to the classical materials such as PZT and SBT. For the interface oxide, CeO_2 [64] was a very popular option, but many other materials with higher k values were tried as well. Another possibility to reduce the depolarization field is to decouple the area of the ferroelectric capacitor from that of the gate capacitor in the FET by adding an additional metal electrode [65]. However,

to get a good effect, the ferroelectric capacitor needs to be made much smaller than the FET gate capacitor, and therefore, the cell size will be limited by the lithographic capability of forming the second electrode [66]. Moreover, the charging of the internal floating node will pose an unknown problem for the endurance of such a device. It seemed that all the research was not showing a lot of progress. But in 2004, finally, the first FeFET with ten years of nonvolatile retention was shown by Sakai and Ilangoan [67] by using a HfAlO buffer layer together with an optimized and rather thick SBT film. [see Fig. 4(a)–(c)]. Although being a major achievement, again the device was trapped in a scalability dilemma. To scale down the channel length, the thickness of the ferroelectric would also have to be scaled down. However, the memory window of the FeFET is dictated by the coercive voltage of the ferroelectric that, in turn, is proportional to the thickness of the ferroelectric [68]. Therefore, besides better CMOS compatibility, a higher coercive field is highly desirable for the ferroelectric material used in a FeFET. Since ferroelectric HfO_2 has both properties already, some of the articles dealt with FeFETs [69], [70] immediately showed data that could outperform earlier FeFETs based on traditional ferroelectrics and at the same time using a scaled-down gate stack. This led to a very strong interest both from academia and industry. In 2016, first data on a fully integrated test array showing both ferroelectric and standard devices using GlobalFoundries' 28-nm FeFET process could be shown [71], and one year later, the technology was also demonstrated using GlobalFoundries' 22-nm FDSOI technology [71], [72] [Fig. 4(d)–(f)].

However, the large coercive field is not strictly beneficial. As in the case of capacitor-based devices, it leads to rather high rewriting voltages of 3–4 V and imposes high stress to the ferroelectric during cycling. Moreover, the inherent dielectric layer at the interface to the silicon channel is subject to very strong field stress during the write operation [73]. This, in turn, leads to strong charge trapping that will eventually degrade the interface oxide and limit the cycling endurance [74], [75]. However, a typical NVM endurance of about 10^5 write cycles is shown at the array level [71], [76]. In addition, the cycling behavior of the memory cell can be further improved by tuning the electrostatics with slightly thicker ferroelectrics [77] or use self-heating to periodically heal the cycling damage [78]. When FeFET devices scaled down to a few 10-nm both in channel length and channel width direction become available, new phenomena can be explored as well. While larger devices show a gradual switching and can be operated in a subloop condition to either allow a very high cycling endurance [79] or adjust a large number of polarization values that can be used for analog storage like in neuromorphic computing [80], scaled-down devices show a limited number of threshold voltage (V_T) levels that can be related to switching of individual domains [81]. This new feature can not only be used to study such effects in nanoscale ferroelectrics but also enable new applications like realizing a random number generator [82] or even greatly simplify the construction of artificial CMOS compatible neurons [83]. The ability to directly integrate memory cells very close to standard transistors [84] and the reprogramming the memory

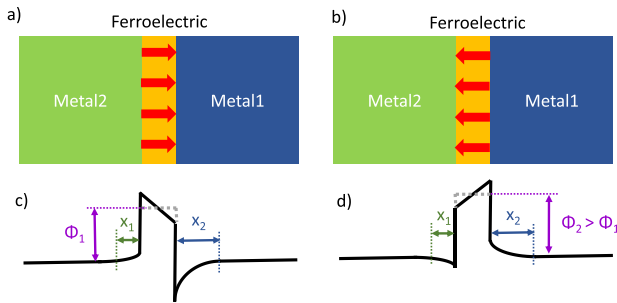


Fig. 5. Classical FTJ using very thin ferroelectric. (a) and (b) Schematic of the tunnel junction in both polarization directions. (c) and (d) Schematic of the conduction band for both polarization directions. The asymmetry of the screening length x on both electrodes leading to a different effective tunneling barrier height Φ can be seen from (c) and (d).

cell at reasonably low voltages together with the unique features of scaled ferroelectric FETs allow for applications that go beyond memories such as logic-in-memory [85] or relaxation oscillators [86]. Moreover, the ferroelectricity in the gate stack of a FeFET can also be exploited in a totally different way. If the region between the two stable polarization states can be stabilized, a negative differential capacitance region could be achieved that allows voltage amplification [87] and reduces the subthreshold swing and can increase the drive current [88]. This interesting application is beyond the scope of this article. Returning to memories, it has been shown that HfO₂-based FeFETs can be integrated into a silicon-ferroelectric-silicon (SFS)-based 3-D NAND architecture [89], [90], which provides another interesting path toward a storage class memory. Note that two interface layers to doped Si electrodes enhance the required switching voltages, which, in turn, reduces the lifetime of the devices.

IV. FTJs

The third variant of reading out the polarization of a ferroelectric is an FTJ. The basic idea is quite old and was proposed by Esaki *et al.* [91] in 1971. However, its realization required the ability to fabricate very thin high-quality ferroelectrics, which was not possible for many years. The concept started to materialize in the first decade of the new millennium [5], and received even more interest in the next decade [92], [93]. Therefore, the concept is by far less advanced compared to FeRAM and FeFET, and all available demonstrations are still using very simple test structures making performance predictions difficult at this point.

Fig. 5 illustrates the dominant mechanism in an FTJ using very thin ferroelectric layers to allow direct tunneling [94]. Different screening lengths in the two metal electrodes give rise to a tunneling barrier that is dependent on the polarization direction. Also, the piezo effect can play a role since it will modulate the tunneling distance [5] but is often neglected if small read voltages are used [94]. These and other basic studies show impressive results. However, they had in common that they were conducted on epitaxial ferroelectrics grown on lattice-matched substrates. This is not a useful integration path for memories integrated with CMOS. However, when very thin polycrystalline layers are used, the conduction via grain boundaries will cause an unwanted current component that will

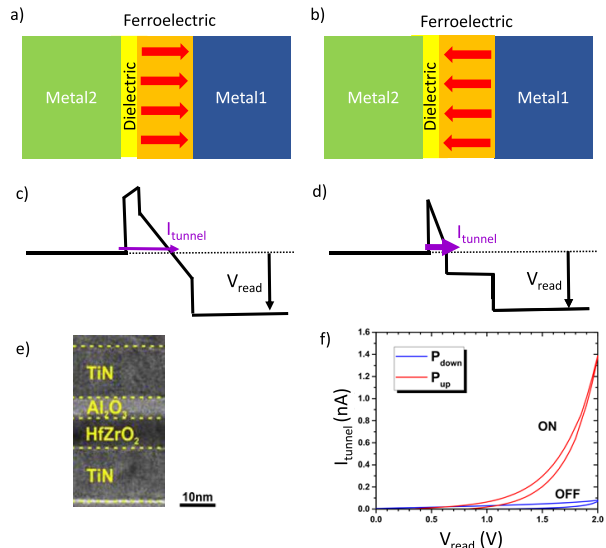


Fig. 6. Two-layer FTJ using a very thin tunneling barrier together with a ferroelectric. (a) and (b) Schematic of the tunnel junction in both polarization directions. (c) and (d) Schematic of the conduction band for both polarization directions. (e) TEM cross section of a double-layer tunnel junction stack [98]. (f) I - V curve of the stack of (e) using 12-nm HZO as the ferroelectric and 2-nm Al₂O₃ as the tunneling barrier [98].

significantly reduce the memory window. Moreover, it is very hard to achieve stable ferroelectricity in polycrystalline layers of only 2–3 nm of thickness even if ferroelectric hafnium oxide is used [95]. The double-layer tunnel junction illustrated in Fig. 6 can be a useful alternative. Here, the ferroelectric is combined with a very thin tunneling layer such as SiO₂ [96] or Al₂O₃ [6].

The thicknesses of both layers need to be carefully adjusted to get an optimum memory window [97]. In such a double-layer tunneling junction, the tunneling current is switched between the direct tunneling through the tunneling barrier [Fig. 6(d)] and the modified Fowler–Nordheim tunneling through both the tunneling barrier and parts of the ferroelectric [Fig. 6(c)]. This stack also has some shortcomings. First, the depolarization field is similar to a FeFET, and therefore, retention needs careful consideration of the stack composition and internal bias fields [98]. Second, the current density will be rather low. The latter problem can be overcome by using a 2T-1 FTJ cell proposed in [99] but at the price of a higher complexity and the necessity of connecting every FTJ directly to the CMOS circuit. However, for neuromorphic applications, small currents may even be beneficial to allow for massive parallel operation [100]. Therefore, FTJs could be a very good fit for fabricating reliable synapses for neuromorphic systems.

V. CONCLUSION

Ferroelectricity is a very interesting material property to realize NVMs. However, the complexity of the materials and their integration into CMOS has hindered rapid development and has kept ferroelectric memories from challenging classical charge-based memories. The discovery of ferroelectricity in hafnium oxide has solved this issue to a large extent. However, this new class of materials holds challenges of its own. In particular, the large coercive field has positive and

negative aspects. In capacitor-based FeRAM, the high coercive field limits the endurance and requires higher operating voltages. A material breakthrough is still required here. Possibly, the concept of the AFeRAM could be a viable alternative, but more work is required.

The material seems to be an ideal fit for FeFETs since HfO_2 is a well-established gate dielectric in the modern CMOS, and here, the large coercive field is a big plus. Both embedded NVM and possibly a NAND type of vertical memory can be imagined. Again, work is required to make highly reproducible devices with a small footprint. Recently, FTJs were a basic research vehicle based on epitaxial layers. The two-layer FTJ using doped hafnium oxide could be a possible path for synapses in neuromorphic computing systems.

Comparing ferroelectric memories with competing emerging memory concepts such as magnetoresistive memories (MRAM), phase-change memories (PCM), or resistive switching memories based on ion migration (resistive random access memory, RRAM), they are currently behind because of the low level of industry and research activities in the last 15 years. However, they show a number of unique advantages compared to each of the competing technologies. The fact that the writing process is field-driven that gives them the lowest write energy of all NVM mechanisms. This is an advantage compared to all other concepts. Compared to MRAM, the ferroelectric effect persists even at very small structures down to a few unit cells while magnetism always requires many spins to act collectively and radical new innovations with every scaling step. Once ferroelectric memories would get enough traction in the mainstream arena, they could be implemented in new scaled technologies with fewer new specific innovations taking advantage of the full-scaling benefit. This is, in particular, a big plus for the implementation in FeFET and FTJ, where aggressively scaled structures are essential. In comparison to PCM, again, the low write energy in both transitions is a big plus while PCM requires the melting of the material in the reset process that always results in high currents. In contrast to RRAM based on either ion vacancy migration (also called valence change memories, VCM) or cation migration [also called electrochemical metallization cell or conductive bridging RAM (CBRAM)], the switching mechanism is well-defined and does not require the formation of a filament leading to much more predictable switching behavior. Finally, the aspect of being able to use the same basic switching mechanism for a capacitor-based cell, a transistor-based cell, and a resistive switching cell is unique and can lead to synergies.

On the downside, the critical issues of cycling stability and imprint as well as statistical variations of the ferroelectric properties on sub-50-nm length scales still need further improvement to make reliable products. The stability issue will be relevant for all three concepts and most important to capacitor-based FeRAM, where a very high-cycling endurance is essential. The statistical variations of the ferroelectric properties are in particular important for FeFET and FTJ, where very small structures are required, while capacitor-based FeRAM needs a larger area due to the sensing requirements anyhow. The currently observed strong rise in a critical mass

of research both in the academic and industrial world could lead to ferroelectric memories being a dominant mainstream technology in 5–10 years. In summary, ferroelectric hafnium oxide has brought ferroelectric memories back from a niche to a very interesting alternative technology with many possible application extensions such as in-memory computing and neuromorphic computing.

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