Effect of Curie Temperature on Ferroelectric Tunnel FET and Its RF/Analog Performance

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***Abstract*— In this article, a numerical simulation study for the ferroelectric gate oxide tunnel field-effect transistor (Ferro-TFET) has been presented. The performance of the device is analyzed following Landau's theory and its behavior in the temperature range of 200–300 K. A minimum subthreshold swing and maximum transconductance is obtained around the Curie temperature (T_C) of 580 ± 10 K for the simulated device. The simulation result is supported by the simple analytical model. The temperature sensitivity analysis is studied on different analog and RF figure of merits for Ferro-TFET. In this study, the Ferro-TFET shows the remarkable result in reducing the detrimental effect of mobility degradation at high gate voltage and performance degradation at high temperatures as compared to conventional TFETs and MOSFET. Therefore, at Curie temperature, the operation of the Ferro-TFET shows the remarkable results for analog and RF applications.**

***Index Terms*— Ferroelectric gate oxide tunnel field-effect transistor (Ferro-TFET), memory window, negative capacitance, temperature.**

I. Introduction

THE thrust of putting an end to the age-old long issue of high subthreshold swing (SS) lead us to explore many new devices. ITRS'2015 [1] mentioned FET as one of the promising devices for reduced SS. In general, SS depends on two factors, charge transport mechanism and total capacitance from silicon body to gate oxide capacitances (body factor). Researchers have presented various works on reaching SS below the Boltzmann limit of 60 mV/dec, addressing the charge transport mechanism by introducing the band-to-band tunneling (BTBT) as dominant current conduction mechanism [2]–[9]. The introduction of negative capacitance paved the way for lowering the body factor. Ferroelectric oxides in series with conventional oxides result in internal voltage amplification proportional to the charge in the ferroelectric oxide, thereby we get an increase of the drain current resulting in lowering of SS [10]–[19]. Therefore, if we combine the effect of both BTBT and ferroelectric oxide, we can get remarkable results for the lowering of SS. Lattanzio *et al*. [12] first proposed the ferroelectric gate oxide tunnel field-effect transistor (Ferro-TFET), observed SS of about 880 mV/dec using the principles of P(VDE-TrFE), and thus widely investigated over the years [20]–[29].

In nanoscale geometries, the investigation of temperature effect becomes a crucial factor in determining the reliability of the device. Also, Landau–Ginzburg (LG) theory shows that temperature plays a key role in understanding the behavior of ferroelectric transistors, as ferroelectric changes its properties from ferroelectric to paraelectric at Curie temperature (T_C) [30], [31]. In our work, we explored for the first time in detail the effect of temperature on characteristics of Ferro-TFET. We studied the effect of temperature on the threshold, memory window, OFF-current, transconductance, SS, and RF parameters. Ferro-TFET shows unique characteristics behavior with temperature, where the performance of the device degrades when devices are subjected to phase transition from ferroelectric to paraelectric.

This article is organized as follows. In Section II, device structure and simulation setup are discussed. In Section III, simple analytical model for current and transconductance of Ferro-TFET is described. Section IV presents the effect of temperature variation, varied from 200 to 700 K, on various electric and RF characteristics. Section V provides the conclusion.

II. Device Structure and Simulation Setup

An SOI device structure is shown in Fig. 1, and the parameter for simulation is given in Table I. The simulation has been performed on Sentaurus TCAD [32]. Fermi–Dirac Statistics and effect of bandgap narrowing are applied to consider heavy doping at source and drain. Doping-dependent mobility model is used to include the effect of doping concentration and the ENormal mobility model to consider the effect of polarization in ferroelectric oxides. To consider the effect of interband tunneling in TFETs efficiently, nonlocal BTBT model along with Shockley–Read–Hall (SRH) recombination model is enabled and it uses Wetzel–Kramer–Brillouin (WKB) approximation.

III. Current and Transconductance Model for Ferrotunnel FET

LG theory [30], [31] describes the thermodynamic properties of ferroelectric material and from LG theory.

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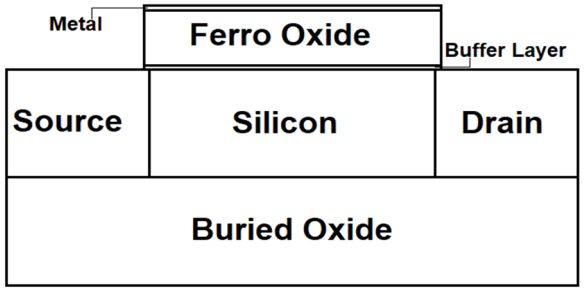

Fig. 1. Structure of the simulated device.

TABLE I
SIMULATION PARAMETER VALUE

.Parameter	Value	.Parameter	Value
Source Doping(p^+)	1×10^{20}/cm^3	Drain Doping (n^+)	5×10^{18}/cm^3
Gate Thickness	40nm	Channel Doping	1×10^{16}/cm^3
Buffer Layer	1nm	Buried Oxide Thickness	20nm
Source and Drain Thickness	30nm	Ferro Thickness(Si:HfO_2)	10nm
P_s(μC/cm^2)	9.25	P_r(μC/cm^2)	9.1
$\mathcal{E}_r$ of Si:HfO_2	32.5	E_C(MV/cm)	1.1

TABLE II
PARAMETERS USED IN MODEL

Symbol	Quantity	Symbol	Quantity
ε_0	Permittivity of free space	ε_{Fe}	Dielectric permittivity of ferroelectric material
C_{ox}	Oxide capacitance	C_{Fe}	Ferroelectric capacitance
C_s	Surface Capacitance	K_B	Boltzmann Constant
q	Charge of an electron	ϕ_F	Pseudo-Fermi level
ε_{si}	Silicon permittivity	V_{FB}	Flatband voltage
N_A	Doping concentration	E_g	Band gap energy
W	Gate Width	$E_g(0)$	1.1557eV
L	Gate Length	ψ	Electrostatic potential
A, B	Kane's tunneling parameters	V_{onset}	Onset voltage of BTBT
α	7.021×10^{-4}	β	1108

Salvatore *et al.* [33], [34] introduced basic model of capacitance, SS, and threshold voltage. The parallel plate capacitance of the ferroelectric material in gate dielectric stack can be written as

$$C_{\text{Fe}} = \frac{\varepsilon_0 \varepsilon_{\text{Fe}}}{d} \tag{1}$$

$$\varepsilon_{\text{Fe}} = \frac{1}{\varepsilon_0 \alpha} = \lambda \frac{C_{\text{CW}}}{T - T_c} \begin{cases} \lambda = \frac{1}{2}, & T < T_c \\ \lambda = 1, & T > T_c \end{cases} \tag{2}$$

where d is the thickness of the ferroelectric oxide, $\alpha = (1/\varepsilon_a)((T - T_c)/C_{\text{CW}})$, and C_{CW} is the Curie–Weiss constant. The ferroelectric oxide is in series with conventional oxide capacitance of the stack is given as

$$C_{\text{Fe-stack}}(T) = \frac{C_{\text{Fe}} C_{\text{ox}}}{C_{\text{Fe}} + C_{\text{ox}}}. \tag{3}$$

The SS of gate stack of ferroelectric layer and conventional oxide is in parabolic dependence with temperature.

$$\text{SS}_{\text{Fe-stack}}(T) = \left[1 + \frac{C_s}{C_{\text{ox}}} - \frac{dC_s T_c}{\varepsilon_o \lambda C_{\text{CW}}}\right] \frac{K_B \ln 10}{q} T + \frac{dC_s}{\varepsilon_o \lambda C_{\text{CW}}} \frac{K_B \ln 10}{q} T^2. \tag{4}$$

The threshold voltage (including the coercive field dependence on temperature) is

$$V_{\text{th}} = V_{\text{FB}} + 2\phi_F + \sqrt{4q\varepsilon_{si} N_a \phi_F} \frac{1}{C_{\text{Fe-stack}}(T)} + \begin{cases} dE_{v\text{th}}, & \text{for } T < T_c \\ 0, & \text{for } T > T_c \end{cases} \tag{5}$$

The expression of the current of a standard tunnel FET [35] is

$$I \approx \frac{\text{WLA}\sqrt{q}}{\text{BE}_g^{3/2}} \left(\frac{E_g N_a}{2\varepsilon_s}\right)^{\frac{D}{2}} e^{B\sqrt{2\varepsilon_s E_g q}/\sqrt{N_a}(\sqrt{\delta\psi} - \sqrt{E_g/q})} \sqrt{\delta\psi} \tag{6}$$

$$\delta\psi = (V_{\text{GS}} - V_{\text{onset}})/\gamma \tag{7}$$

$$\gamma = 1 + \frac{\varepsilon_s}{C_{\text{ox}}} \sqrt{\frac{q^2 N_a}{2E_g \varepsilon_s}}. \tag{8}$$

The expression of drain current is modified with the replacement of C_{ox} in (8) with $C_{\text{Fe-stack}}$ (t) from (3) to consider the dominant effect of variation of capacitance with temperature, which degrades the drain current above T_C in comparison with effect of temperature on bandgap $[E_g(T) = E_g(0) + (\alpha T^2/(T + \beta))]$.

$$\gamma = 1 + \frac{\varepsilon_s \varepsilon_0 \lambda C_{\text{CW}} + (T - T_c) dC_{\text{ox}}}{\varepsilon_0 \lambda C_{\text{CW}} C_{\text{ox}}} \sqrt{\frac{q^2 N_a}{2E_g \varepsilon_s}}. \tag{9}$$

Also, we can now write the expression of the transconductance as

$$g_{m,\text{Fe-TFET}}(T) = \frac{\partial I_D}{\partial V_{\text{GS}}} = \frac{\text{WLA}\sqrt{q}}{2BE_g^{3/2}} \left(\frac{E_g N_a}{2\varepsilon_s}\right)^{\frac{D}{2}} \times e^{B\sqrt{2\varepsilon_s E_g q}/\sqrt{N_a}(\sqrt{\delta\psi} - \sqrt{E_g/q})} \times \left(B\sqrt{2\varepsilon_s E_g q}/\sqrt{N_a} + \frac{1}{\sqrt{\delta\psi}}\right). \tag{10}$$

The mathematical model presented here is modification of the model presented in [33]–[35]. In [33] and [34], they have presented mathematical model for FE-FET which we have included in tunnel FET current model presented in [35] for analyzing our Ferro-TFET characteristics. The model helps us to analyze the effect of temperature variation on capacitance for drain current, transconductance, and SS of the device. The description of parameter used in Section III is given in Table II.

IV. RESULTS AND DISCUSSION

In our work, the ferroelectric oxide Si:HfO_2 is introduced in series with conventional gate oxide. The effect of temperature variation is investigated as it plays a pivotal role in determining the phase of the ferroelectric material. The phase changes

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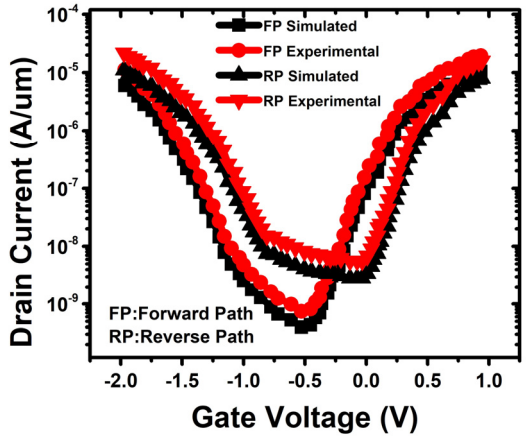

Fig. 2. I_D–V_G graph for experimental and simulated Fe-TFET (gate length = 350 nm, work function = 5 eV, ferrothickness = 46 nm, and drain voltage = 0.5 V) [29].

from ferroelectric to paraelectric as the temperature reaches the Curie temperature point. The simulation parameter is calibrated with the experimental results [29] and shown in Fig. 2. The temperature is varied from 200 to 700 K for a drain voltage of 0.5 V, and gate voltage sweep is kept at −4 to 4 V. Fig. 3(a) shows that the drain current increases with the temperature for the whole range of gate voltage till 580 K as bandgap reduces shown in Fig. 3(b) and for above 580 K, drain current reduces after reaching V_{onset} because any value of temperature above 580 K will increase γ of (9) which is responsible for reduction of $\delta\psi$ of (7), leading to reduction of drain current of (6). For temperature below 580 K, increase of drain current due to bandgap reduction stays as the dominant factor but above 580 K, γ plays the major role in drain current behavior. When we approach T_c, ferroelectric material changes phase from ferroelectric to paraelectric leading to shrinking of the polarization loop due to decrease of coercive field, remanent polarization, and increase of its permittivity. Hence, the device no longer exhibits ferroelectric properties of providing negative capacitance when included as oxide in the device for reduction of SS. The effect can be observed from Fig. 3(c) and (d), where forward path threshold voltage reduces linearly but reverse-path threshold voltage increases till it reaches the transition point and then it reduces again like in (5); thus, the memory window reduces with an increase of temperature. The ferrodevice reaches a transition point close to 580 ± 10 K and, hence, this is the Curie temperature for ferrodevice.

When we increase the temperature, OFF-state current increases due to a large number of carrier generation in the reversed biased junction. In comparison with OFF-state current, the increase of ON-state current is lower; this is basically because OFF-state current consists of two major temperature-dependent trap-assisted tunneling (TAT) and SRH recombination current, whereas ON-state current depends on the BTBT current which owing to less effective bandgap narrowing effect as with increased temperature in (6) and it is shown in Fig. 4(a). In (4), SS does not follow linear relation with temperature as in the case of MOSFET but follows a parabolic relation with temperature in case of the

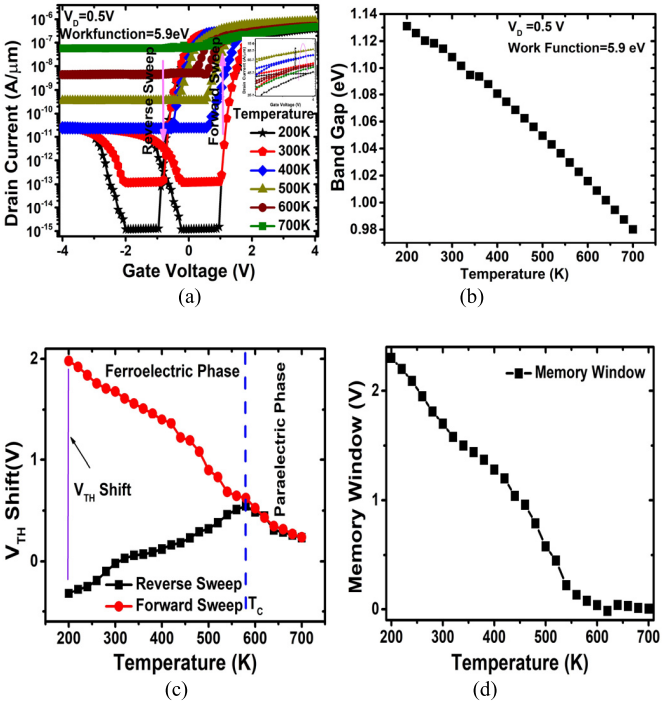

Fig. 3. I_D–V_G, bandgap, V_{TH} shift, and memory window with variation of temperature.

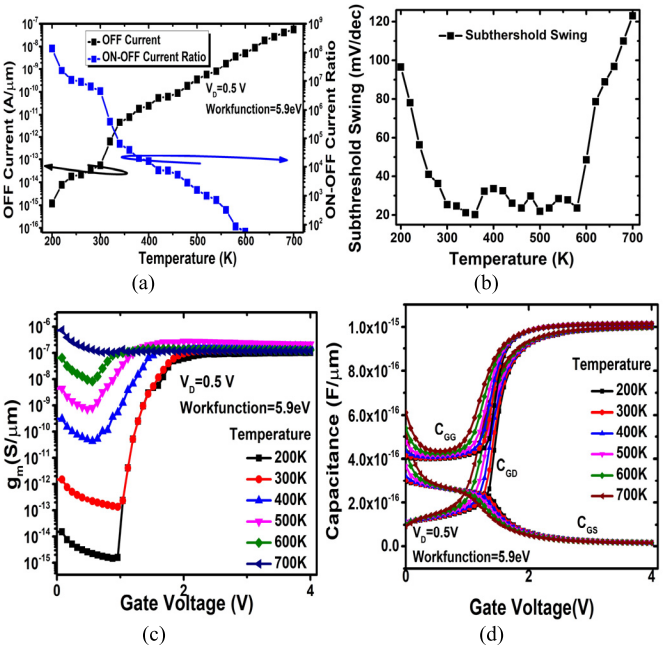

Fig. 4. OFF current, ON–OFF current ratio, SS, transconductance, and capacitance.

ferroelectric-conventional oxide gate stack. Near to Curie temperature, gate coupling, and electrostatic control over the channel increases by ferroelectric oxide. In Fig. 4(b), SS plot for both phases has been shown; we can observe that SS reaches a minimum near to 580 ± 10 K because at this point ferroelectric material permittivity is maximum, leads to exceptional improvement of gate coupling of the device and it rises sharply again beyond this point, thus satisfying the nature predicted by (4). In Fig. 4(c), transconductance variation with temperature is shown, it implies a device ability to amplify

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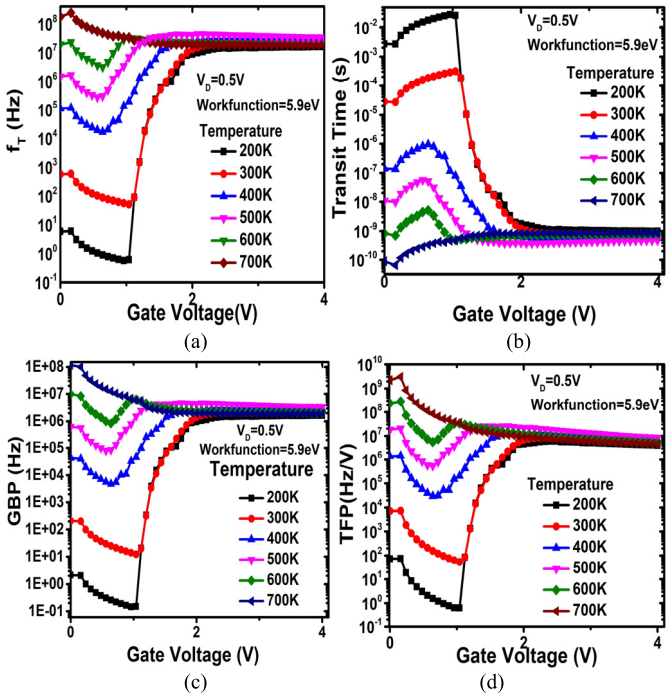

Fig. 5. Unity gain frequency, transit time, GBP, and TFP.

its input voltage to output current. A higher transconductance represents better amplification. In the subthreshold region, transconductance is smaller and gradually increases until the saturation region. In the subthreshold region, transconductance increases with the increase of temperature due to the increase of the OFF current which significantly deteriorates the device characteristics in the subthreshold region. In a strong inversion region, transconductance increases with temperature until we reach the Curie point, beyond which it reduces again. Also, significant characteristics can be observed that at higher gate voltage, transconductance does not degrade which is in contrast to the conventional MOSFET and TFET characteristics, where transconductance degrades at higher gate voltage due to mobility degradation and is predicted by (9). In TFET, the gate to drain capacitance (C_{gd}) is large due to the tunneling barrier at the source side of the TFET and thereby C_{gd} dominates over C_{gs} in contribution to the total capacitance C_{gg}. Ferroelectric oxide contributes to the better electrostatic coupling of the channel resulting in a lowering of capacitance than the conventional TFET. In Fig. 4(d), it is observed that in subthreshold region, capacitance increases with temperature until it reaches saturation, where the reduction in total capacitance is observed for temperature above 580 K that can also be related to the fact that ON current reduces for gate voltage beyond the onset voltage of BTBT.

Unity gain frequency is plotted in Fig. 5(a) and is defined as the frequency at which the short circuit current gain becomes unity and given as $f_T = (g_m/2\pi C_{gg})$. Increasing gate voltage f_T increases due to an increase in transconductance. It reaches peak value where C_{gg} is minimum and g_m is maximum. In conventional tunnel fet, f_T reduces for higher gate voltage due to the mobility degradation effect in g_m, whereas elimination of mobility degradation in Ferro-TFET, f_T, approximately remains constant. Ferro-TFET can efficiently work in the 1–100-MHz range and shows the remarkable result in higher gate voltage region. Transit time is the time taken by the device to transfer carriers from source to drain region and is represented as $\tau = (1/(2\pi 10 * f_T))$ and shown in Fig. 5(b). τ decreases with the increase of gate voltage due to increase of inversion charge density and lowering of tunneling barrier. Also, an increase in temperature shows a higher speed in the subthreshold region due to the reduction of tunneling barriers. Carrier requires a shorter time to travel from source to drain and reducing the transit time, it is in the order of 10^{-9} S. Thus, Ferro-TFET has a high switching speed. Another important figure of merit is to the gain-bandwidth product, expressed as GBP $= (g_m/20\pi(C_{gd}))$ plotted in Fig. 5(c). It shows a trend similar to unity gain frequency. It increases with gate voltage and showing a reduction in detrimental effect due to mobility degradation at higher gate voltage in conventional TFET and MOSFET. GBP represents a tradeoff between bandwidth and gain of the device. A higher value of GBP of the order of 10^6 in our device shows dominancy of gain over bandwidth. Fig. 5(d) shows plot for transistor frequency product or TFP $= (g_m/I_{ds}) \times f_T$, an important figure of merit for device applicability analysis in the high-frequency region. TFP follows characteristics dominated by g_m for lower value of gate voltage and remains approximately constant for values of gate voltage above onset voltage due to its remarkable performance in controlling the detrimental effect of mobility degradation.

V. Conclusion

In this article, the essential role of Curie temperature in designing Ferro-TFET for analog and RF applications has been explored. The simulation result based on LG theory and simple analytical model for temperature variation from 200 to 700 K closely match. Curie temperature point for our device is at 580 ± 10 K. Furthermore, in high gate voltage region of Ferro-TFET, mobility degradation is reduced as compared to MOSFET and conventional TFET. It also shows excellent analog/RF figures of merit thus implicate its efficient applicability in a wide range of temperatures for analog and RF applications.

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