Domain - VLSI Design and Verification

Course Code	Course Title	Course Nature	Credits	Pre-requisite
DEVL0401	Digital System Design using VERILOG	Theory + Practice	4	Nil
DEVL0101	FPGA Architecture and Design	Theory	3	Nil
DEVL0402	HDL Synthesis and System Architecture	Theory + Practice	4	Nil
DEVL403	System VERILOG	Theory + Practice	4	Nil
DEVL0201	VLSI Verification Methodologies	Practice	2	Nil
DEVL0102	VLSI Test Principle and Testable Design	Theory	3	Nil
DEET0300	Project	Project	6	
DEET0800	Internship	Internship	4	
			30	

Digital System Design using VERILOG

Course Title	Code	Type of course	T-P-PJ	Prerequisite
Digital System Design using VERILOG	DEVL0401	Theory & Practice	2-2-0	Nil

Objective

- To Make The Student Understand Advanced Digital System Design using Verilog Programming

Learning Outcome

- Student will be Able to Write Efficient Verilog Programme
- Student will be Able to Design Advanced Digital System Using Verilog HDL.

Evaluation Systems

Internal Examination	**Component**	**% of Marks**	**Method of Assessment**
	Internal Theory	20	Written Examination
	Internal Practice	30(20+10)	Lab Work + Learning Record
External Examination	External Theory	30	Written Examination
	External Practice	20	Lab Work
Total		100	

Course Outline

Module I: Introduction to VLSI Design (10 Hours)

Theory

VLSI Design flow: Full Custom, ASIC and FPGA. Design Tools: CAD Tool Taxonomy, Editors, Simulators, Simulation System, Simulation Aids, Applications of Simulation, Synthesis Tools, and Introduction to Hardware Description Languages (HDL)

Practice

1. Introduction to Xilinx EDA Tool.
2. Introduction With XST Tool and ISIM Tool
3. Xilinx Tool Flow: Simulation and Synthesis

Module II: Verilog HDL (12 Hours)

Introduction to Verilog HDL, Abstraction levels, basic concepts, Verilog primitives, keywords, data types, nets and registers, Verilog Modules and ports

Practice

4. Modulea and Port Declaration in Verilog Using Xilinx Tool.
5. Use of Different Data Types in Verilog Programing.

6. Design and Create Simulation Waveform for Different Digital Logic Gates Using Data Types-1
7. Design and Create Simulation Waveform for Different Digital Logic Gates Using Data Types-2

Module III: Verilog Operators (12 Hours)

Theory

Logical Operators, Bitwise and Reduction Operators, Concatenation and Conditional Operators, Relational and Arithmetic, Shift and Equality Operators, Operator Execution Order. Assignments: Types of Assignments, Continuous Assignment, Procedural Assignments, Blocking and Non-Blocking Assignments, Tasks and Functions

Practice

8. Design and Create Simulation Waveform for Different Digital Logic Gates Using Operators-1
9. Design and Create Simulation Waveform for Different Combinational Logic Circuit Using Operators-2
10. Design and Create Simulation Waveform for Different Combinational Logic Using Continuous Assignment Statements
11. Design and Create Simulation Waveform for Different Sequential Circuits Using Blocking and Non-Blocking Statements

Module IV: Verilog Modelling (12 Hours)

Theory

Gate Type, Design Hierarchy, Gate Delay, Propagation Delay, Logic Simulation Dataflow-Level Modelling: Assignments, Behavioural Modeling: Always Block, Flow Control, If-Else, Case, Cases, While Loop, For Loop, Repeat

Practice

12. Design and Create Simulation Waveform for Full Adder Using Dataflow Modelling, Behavioral Modelling(if-else, case)
13. Design and Create Simulation Waveform for Sequential Circuits Using Behavioral Modelling (case, while loop, for loop, repeat)
14. Design and Create Simulation Waveform for Decoder Using Dataflow Modelling, Behavioral Modelling(if-else, case)
15. Design and Create Simulation Waveform for Multiplexer Using Behavioral Modelling(case, while loop, for loop, repeat)
16. Design and Create Simulation Waveform for Parity Generator and Parity Checker Using Dataflow Modelling, Behavioral Modelling(if-else, case)

Module V: Verilog for Verification (14 Hours)

Theory

Design Verification and Testing, Test Bench Writing, Initial Statement, Verilog System Tasks: $finish, $stop, $display, $monitor, $time, $realtime, $random, $save, $readmemh/$writememh, $fopen, $fclose, Compiler Directives, ifdef, Array, Multi-Dimensional Array, Memory Modelling

Practice

17. Design and Create Simulation Waveform for Full Adder Using Continuous Assignment, Procedural Assignments With The Use of System Task and Functions-1
18. Design and Create Simulation Waveform for Full Subtractor Using Continuous Assignment, Procedural Assignments With the Use of System Task and Functions-2
19. Design and Create Simulation Waveform for Multiplexers Using Continuous Assignment, Procedural Assignments With the Use of System Task and Functions-3
20. Design and Create Simulation Waveform for Encoders Using Continuous Assignment, Procedural Assignments With the Use of System Task and Functions-4
21. Design And Create Simulation Waveform For Decoders Using Continuous Assignment, Procedural Assignments With the Use of System Task and Functions-5

Module VI: Combinational Logic Circuit Design (15 Hours)

Theory

Logic Synthesis, RTL Synthesis, High-Level Synthesis, Synthesis Design Flow, Design and Analysis of Combinational Circuits, Synthesis of Combinational Circuits, Arithmetic Circuits, Initial Design And Optimization, Encoder, Decoder, De-Multiplexer Circuits, Multiplexer Circuits and their Implementation Using Verilog, Design of a 4-Bit Comparator, Design of a 4-Bit ALU and a Simple Processor Using Verilog

Practice

22. Design and Create Simulation Waveform for Full Adder Using Continuous Assignment and Procedural Assignments
23. Design and Create Simulation Waveform for Encoder and Decoder Using Continuous Assignment and Procedural Assignments
24. Design and Create Simulation Waveform for De-Multiplexer Using Continuous Assignment and Procedural Assignments
25. Design and Create Simulation Waveform For 4-Bit Comparator Using Continuous Assignment and Procedural Assignments
26. Design And Create Simulation Waveform For 4-Bit ALU Using Continuous Assignment and Procedural Assignments

Module VII: Sequential Logic Circuit Design (15 Hours)

Theory

Synthesis of Sequential Circuits, Study of Synchronous and Asynchronous Sequential Circuits, Flip Flops, Shift Registers, Counters and their Design Using Verilog.

State Machine: Basic Finite State Machines (FSM) Structures, Mealy and Moore Type FSM, Mealy Vs. Moore, Common FSM Coding Style, Serial Adder Design Using FSM, FSM as an Arbiter Circuit, FIFO, Bus Interfaces.

Practice

27. Design and Create Simulation Waveform for SR-Flip Flop And D-Flip Flop Using Continuous Assignment and Procedural Assignments
28. Design and Create Simulation Waveform for JK-Flip Flop And T-Flip Flop Using Continuous Assignment and Procedural Assignments
29. Design and Create Simulation Waveform for Shift Registers(SISO,SIPO,PISO,PIPO) Using Continuous Assignment and Procedural Assignments
30. Design and Create Simulation Waveform for 2-Bit Ripple Counter Using Continuous Assignment and Procedural Assignments
31. Design and Create Simulation Waveform for 8-Bit Up/Down Synchronous Binary Counter Using Continuous Assignment and Procedural Assignments

Text Books

1. Palnitkar, Samir. "Verilog HDL: A Guide To Digital Design and Synthesis", Pearson Education India, 2003
2. Navabi, Zainalabedin, and Yuwen Xia. "Verilog Digital System Design: Register Transfer Level Synthesis, Testbench, and Verification", McGraw-Hill, 2006
3. Mishra, Kishore K. "Advanced chip design: Practical examples in Verilog", Create Space Independent Publishing Platform, 2013

Reference Books

1. Bhasker, Jayaram. "Verilog HDL Synthesis: A Practical Primer", Star Galaxy Publishing, 2008.
2. Wolf, Wayne. FPGA-Based System Design". Pearson education, 2004.
3. Ciletti, Michael D, "Advanced Digital Design with the Verilog HDL", Vol. 1. Upper Saddle River: Prentice Hall, 2003.

Session plan

Topic	No. of Sessions (in hrs.)	Activity	Assignment	Suggested Reading
Module I [4 Hrs. Lecture+6 Hrs. Practice]				
Introduction To VLSI Design	4	Lecture	Assignment-	TB-1(Ch.1)

VLSI Design Flow: Full Custom, ASIC and FPGA, Design Tools: CAD Tool Taxonomy, Editors, Simulators, Simulation System, Simulation Aids, Applications of Simulation, Synthesis Tools, Introduction to Hardware Description Languages (HDL)			1.1	
Introduction To Xilinx EDA Tool. Introduction With XST Tool And ISIM Tool Xilinx Tool Flow: Simulation And Synthesis	6	Practice		
Module II [4 Hrs. Lecture+8 Hrs. Practice]				
Verilog HDL Introduction to Verilog HDL, Abstraction Levels, Basic Concepts, Verilog Primitives, Keywords, Data Types, Nets and Registers, Verilog Modules and Ports	4	Lecture	Assignment-2.1	TB-1 (Ch.1,2,3,4)
Module and Port Declaration in Verilog Using Xilinx Tool. Use of Different Data Types in Verilog Programing. Design and Create Simulation Waveform for Different Digital Logic Gates Using Data Types-1 Design and Create Simulation Waveform For Different Digital Logic Gates Using Data Types-2	8	Practice		
Module III [4 Hrs. Lecture+8 Hrs. Practice]				
Verilog Operators Logical Operators, Bitwise and Reduction Operators, Concatenation and Conditional operators, Relational and Arithmetic, Shift and Equality Operators, Operator Execution Order. Assignments: Types Of Assignments, Continuous Assignment, Procedural Assignments, Blocking and Non-Blocking Assignments, Tasks and Functions.	4	Lecture	Assignment-3.1	TB-1(Ch. 3,6)
1. Design And Create Simulation	8	Practice		

Waveform for Different Digital Logic Gates Using Operators-1 2. Design and Create Simulation Waveform for Different Combinational Logic Circuit Using Operators-2 3. Design And Create Simulation Waveform For Different Combinational Logic Using Continuous Assignment Statements 4. Design And Create Simulation Waveform For Different Sequential Circuits Using Blocking And Non-Blocking Statements				
Module IV [4 Hrs. Lecture+8 Hrs. Practice]				
Verilog Modelling Gate Type, Design Hierarchy, Gate Delay, Propagation Delay, Logic Simulation Dataflow-Level Modelling: Assignments, Behavioural Modeling: Always Block, Flow Control, If-Else, Case, Cases, While Loop, For Loop, Repeat	4	Lecture	Assignment-4.1	TB-1(Ch.6,7)
1. Design and Create Simulation Waveform for Full Adder Using Dataflow Modelling, Behavioral Modelling (If-Else, Case) 2. Design and Create Simulation Waveform for Sequential Circuits Using Behavioral Modelling (Case, While Loop, For Loop, Repeat) 3. Design and Create Simulation Waveform for Decoder Using Dataflow Modelling, Behavioral Modelling (If-Else, Case) 4. Design and Create Simulation Waveform for Multiplexer Using Behavioral Modelling (Case, While Loop, For Loop, Repeat)	8	Practice		

5. Design and Create Simulation Waveform for Parity Generator and Parity Checker Using Dataflow Modelling, Behavioral Modelling (If-Else, Case)				
Module V [4 Hrs. Lecture+10 Hrs. Practice]				
Verilog For Verification Design Verification And Testing, Test Bench Writing, Initial Statement, Verilog system Tasks: $Finish, $Stop, $Display, $Monitor, $Time, $Realtime, $Random, $Save, $Readmemh/$Writememh, $Fopen, $Fclose, Compiler Directives, Ifdef, Array, Multi-Dimensional Array. Memory Modelling	4	Lecture	Assignment-5.1	TB-1(Ch.9)
Module VI [5 Hrs. Lecture+10 Hrs. Practice]				
Combinational Logic Circuit Design Logic Synthesis, RTL Synthesis, High-Level Synthesis, Synthesis Design Flow, Design and Analysis of Combinational Circuits, Synthesis of Combinational Circuits, Arithmetic Circuits, Initial Design and Optimization, Encoder, Decoder, De-Multiplexer Circuits, Multiplexer Circuits and their Implementation Using Verilog, Design of a 4-Bit Comparator, Design of a 4-Bit ALU and a Simple Processor Using Verilog.	5	Lecture	Assignment-6.1	TB-1(Ch.14)

1. Design and Create Simulation Waveform for Full Adder Using Continuous Assignment and Procedural Assignments 2. Design and Create Simulation Waveform for Encoder and Decoder Using Continuous Assignment and Procedural Assignments 3. Design and Create Simulation Waveform for De-Multiplexer Using Continuous Assignment and Procedural Assignments 4. Design and Create Simulation Waveform for 4-Bit Comparator Using Continuous Assignment and Procedural Assignments **5.** Design and Create Simulation Waveform for 4-Bit ALU Using Continuous Assignment and Procedural Assignments	10	Practice		
Module VII [5 Hrs. Lecture+10 Hrs. Practice]				
Sequential Logic Circuit Design Synthesis Of Sequential Circuits, Study of Synchronous and Asynchronous Sequential Circuits, Flip Flops, Shift Registers, Counters and Their Design Using Verilog State Machine: Basic Finite State Machines (FSM) Structures, Mealy And Moore Type FSM, Mealy Vs. Moore, Common FS Coding Style, Serial Adder Design Using FSM, FSM as an Arbiter Circuit, FIFO, Bus Interfaces	5	Lecture	Assignment-7.1	TB-1(Ch.14)
1. Design And Create Simulation Waveform For SR-Flip Flop and D-Flip Flop Using Continuous Assignment And Procedural Assignments 2. Design and Create Simulation Waveform for JK-Flip Flop and T-Flip Flop Using Continuous Assignment and Procedural	10	Practice		

Assignments 3. Design and Create Simulation Waveform for Shift Registers (SISO,SIPO,PISO,PIPO) Using Continuous Assignment and Procedural Assignments 4. Design and Create Simulation Waveform for 2-Bit Ripple Counter using Continuous Assignment and Procedural Assignments **5.** Design and Create Simulation Waveform for 8-Bit Up/Down Synchronous Binary Counter Using Continuous Assignment and Procedural Assignments				
Total (In Hrs.)	**90**	**30 Hrs. lecture+60 Hrs. Practice**		

FPGA Architecture and Design

Course Title	Code	Type of course	T-P-PJ	Prerequisite
FPGA Architecture and Design	DEVL0101	Theory	3-0-0	Nil

Objective

- To Make the Student Understand of Various FPGA Architectures which Subsequently Enables them to Design and Implement Various Complex Digital Architectures Using Verilog and Subsequently Implement the Digital Architecture iyn FPGA

Learning Outcome

- Student will be Able to Design Digital Systems using Verilog.
- Student will be Able to implement Digital Design in FPGA.
- Student will be Able to Handle Different FPGA Architecture.

Evaluation Systems

	Component	% of Marks	Method of Assessment
Internal Examination	Internal Theory	30	Written examination
	Assignment	5	Report or Presentation + Learning Record
	Attendance	5	Based on class attended
External Examination	External Theory	60	Written examination
Total		**100**	

Course Outline

Module I: PLD (5 Hours)

Theory

Introduction to PLDS, General Structure and Classification: SPLD, CPLD, PAL, PLA, CPLD vs. FPGA.

Module II: FPGA (6 Hours)

Theory

Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects Programmable I/O Blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.

Module III: SRAM Programmable FPGAs (6 Hours)

Theory

Introduction, Programming Technology, Device Architecture, the Xilinx XC2000, XC3000 and XC4000 Architectures. **Anti-Fuse Programmed FPGAs:** Introduction, Programming Technology, Device Architecture.

Module IV: Design Applications (6 Hours)

Theory

General Design Issues, Counter Examples, a Fast Video Controller, a Position Tracker for a Robot Manipulator, a Fast DMA Controller, Designing Counters with ACT Devices, Designing Adders and Accumulators with the ACT Architecture.

Module V: Xilinx FPGA Architecture (6 Hours)

Theory

Features and Architectures, Configurable Logic Blocks (CLBs), Input Output Blocks (I/OB), Block RAM, Programming Interconnects, Digital Clock Manager (DCM), Power Distribution and Configuration.

Module VI: ACTEL FPGA Architecture (8 Hours)

Theory

ACTEL Family, ACTEL Features and Logic Modules, C Modules and S Modules, I/O Modules, I/O Pad Drivers, Clock Networks. Intel and ALTERA FPGA Architecture.

Module VII: Embedded Processor Based Design (8 Hours)

Theory

IP Cores, Hard Cores, Firm Core, Soft Cores, Advantages and Disadvantages of Hard, Firm, Soft Cores, FPGA Embedded Processor Types, Picking the Right Core Processor, Implementing a Design, DSP Based Design Flow.

Text Books

1. S.M. Trimberger, "Field-Programmable Gate Array Technology," Springer Science & Business Media,2012
2. W.Wolf, "FPGA-Based System Design," Pearson education, 2004
3. I Grout, "Digital Systems Design with FPGAS and CPLDS," Elsevier, 2011

Reference Books

1. J.V. Oldfield andR.C. Dorf, "Field-Programmable Gate Arrays" , John Wiley & Sons, 1995
2. P.K. Chan and S.Mourad, "Digital System Design Using Field Programmable Gate Arrays," PTR Prentice Hall, 1994
3. R.C. Cofer and B.F.Harding, "Rapid System Prototyping with FPGAs: Accelerating the Design Process". Elsevier2006

Session Plan:

Topics	No. of Sessions (in hrs.)	Activity	Assignment	Suggested Reading
Module I[5 Hrs. Lecture]				
PLD PLD: Introduction to PLDS, General Structure and Classification: SPLD, CPLD	2	**Lecture**	Assignment-1.1	Text book-3 (Ch.1)
PAL	1	**Lecture**	Assignment-1.2	Text book-3 (Ch.1)
PLA	1	**Lecture**	Assignment-1.3	Text book-3 (Ch.1)
CPLD vs. FPGA	1	**Lecture**	Assignment-1.4	Text book-3 (Ch.1)
Module II[6 Hrs. Lecture]				
FPGA Organization of FPGAs, FPGA Programming Technologies	1	**Lecture**	Assignment-2.1	Text book-1 (Ch.2)
Programmable Logic Block Architectures	1	**Lecture**	Assignment-2.2	Text book-1 (Ch.2)
Programmable Interconnects	1	**Lecture**	Assignment-2.3	Text book-1 (Ch.2)
Programmable I/O blocks in FPGAs	1	**Lecture**	Assignment-2.4	Text book-1 (Ch.2)
Dedicated Specialized Components of FPGAs	1	**Lecture**	Assignment-2.5	Text book-1 (Ch.2)
Applications of FPGAs	1	**Lecture**	Assignment-2.6	Text book-1 (Ch.2)
Module III[6 Hrs. Lecture]				
SRAM Programmable FPGAs Introduction, Programming Technology	1	**Lecture**	Assignment-3.1	Text book-1 (Ch.2)
Device Architecture, The Xilinx XC2000	1	**Lecture**	Assignment-3.2	Text book-1 (Ch.2)

XC3000 Architecture	1	**Lecture**	Assignment-3.3	Text book-1 (Ch.2)
XC4000 Architecture	1	**Lecture**	Assignment-3.4	Text book-1 (Ch.2)
Anti-Fuse Programmed FPGAs: Introduction	1	**Lecture**	Assignment-3.5	Text book-1 (Ch.2)
Programming Technology, Device Architecture	1	**Lecture**	Assignment-3.6	Text book-1 (Ch.2)
Module IV[6 Hrs. Lecture]				
Design Applications General Design Issues, Counter Examples	1	**Lecture**	Assignment-4.1	Text book-1 (Ch.2)
A Fast Video Controller	1	**Lecture**	Assignment-4.2	Text book-1 (Ch.2)
A Position Tracker for a Robot Manipulator	1	**Lecture**	Assignment-4.3	Text book-1 (Ch.2)
A Fast DMA Controller	1	**Lecture**	Assignment-4.4	Text book-1 (Ch.2)
Designing Counters with ACT Devices	1	**Lecture**	Assignment-4.5	Text book-1 (Ch.3)
Designing Adders and Accumulators with the ACT Architecture	1	**Lecture**	Assignment-4.6	Text book-1 (Ch.3)
Module V[6 Hrs. Lecture]				
Xilinx FPGA Architecture Features and Architectures, Configurable Logic Blocks (CLBs)	1	**Lecture**	Assignment-5.1	Text book-1 (Ch.2)
Input Output Blocks (I/OB)	2	**Lecture**	Assignment-5.2	Text book-1 (Ch.2)
Programming Interconnects	1	**Lecture**	Assignment-5.3	Text book-1(Ch.2)
Digital Clock Manager (DCM)	1	**Lecture**	Assignment-5.4	Text book-1 (Ch.2)

Power Distribution and Configuration	1	**Lecture**	Assignment-5.5	Text book-1 (Ch.2)
Module VI[8 Hrs. Lecture]				
ACTEL FPGA Architecture ACTEL Family, ACTEL Features and Logic Modules	1	**Lecture**	Assignment-6.1	Text book-1 (Ch.3)
C Modules and S Modules	2	**Lecture**	Assignment-6.2	Text book-1 (Ch.3)
I/O MODULEs	1	**Lecture**	Assignment-6.3	Text book-1 (Ch.3)
Clock Networks	1	**Lecture**	Assignment-6.4	Text book-1(Ch.3)
I/O Pad Drivers	1	**Lecture**	Assignment-6.5	Text book-1 (Ch.3)
Intel and ALTERA FPGA Architecture	2	**Lecture**	Assignment-6.6	Text book-1 (Ch.3)
Module VII[8 Hrs. Lecture]				
Embedded Processor based Design IP Cores, Hard Cores, Firm Core, Soft cores	2	**Lecture**	Assignment-7.1	Text book-5 (Ch.2)
Advantages and Disadvantages of Hard Firm, Soft Cores	2	**Lecture**	Assignment-7.2	Text book-5 (Ch.2)
FPGA Embedded Processor Types, Picking the Right Core Processor and Implementing a Design, DSP Based Design Flow	3	**Lecture**	Assignment-7.3	Text book-5 (Ch.2)
Total (in Hrs.)	**45**	**45 Hrs. Lecture**		

HDL Synthesis and System Architecture

Course Title	Code	Type of course	T-P-PJ	Prerequisite
HDL Synthesis and System Architecture	DEVL0402	Theory & Practice	2-2-0	Nil

Objective

- To Make Students Learn the Advanced Digital System Architecture, the RTL Level Synthesis and Address the Timing Issues Associated with the Digital System Architecture

Learning Outcome

- Students Will be Able to Design and Synthesize a Complex Digital Functional Block Using Verilog HDL
- Students Will be Able to Demonstrate an Understanding of Issues Involved in Digital Design Such as Technology Choice, Timing Analysis, Tool-Flow and Testability

Evaluation Systems

Internal Examination	**Component**	**% of Marks**	**Method of Assessment**
	Internal Theory	20	Written Examination
	Internal Practice	30(20+10)	Lab Work + Learning Record
External Examination	External Theory	30	Written Examination
	External Practice	20	Lab Work
Total		100	

Course Outline

Module I: HDL Architecture Design (12 Hours)

Theory

Design of Various Subsystems by Verilog HDL in Xilinx ISE and Also They Will Check the Performance of Each Circuit in Terms of Area, Speed And Power. Sub Systebook-2, Ch.3m Design, Hardware Description Language (HDLs), Register Transfer Design, Pipeline and Data Path

Practice

1. RTL Design Of 4-Bit, 8-Bit and 16-Bit ALU and Their Performance Evaluation

Module II: HDL Architecture Design (11 Hours)

Theory

Adders, Multipliers, Memories, PLAs, Buses and Network on chips

Practice

2. RTL Design of Data Path Architecture

Module III: Static Time Analysis (12 Hours)

Theory

Basic Concepts of Static Time Analysis (STA) Used in the Design and They Will Solve Various Timing Related Issue in Their Design.], Timing and Delay and the Concept of STA, Types of Delay, Models- Distributed, Lumped Resource

Practice

3. RTL Design of Pipelined Architecture and Its Performance Evaluation

Module IV: Static Time Analysis (STA) (12 Hours)

Theory

Pin to Pin Delay Model, Path Delay Modelling, Timing Checks Delay Back Annotations

Practice

4. RTL Design of various adder topologies/architectures
5. Ripple Carry Adder
6. Carry Skip Adder
7. Carry Increment Adder
8. Carry Look Ahead Adder
9. Carry Save Adder
10. Carry Select Adder
11. Carry Bypass Adder
12. Ling adder
13. Prefix adder
14. Parallel prefix adder
15. Conditional Sum adder

Module V: Floorplaning, Routing, Placement (15 Hours)

Theory

Advanced Simulations, Coding For Synthesis, Synthesis Optimization

Practice

RTL Design of Various Multiplier Architectures

16. RTL Design of Booth Multiplier Architectures
17. RTL Design of Combinational Multiplier
18. RTL Design of wallace Tree Multiplier
19. RTL Design of Array Multiplier
20. RTL Design of Sequential Multiplier
21. RTL Design of Serial Parallel Multiplier
22. RTL Design of MAC Unit Design

Module VI: Floorplaning (15 Hours)

Theory

Floor Planning & Place and Route Optimization, Floorplaning Styles and Methodology, Global Routing

Practice

RTL Design Of Various Memory Units:

23. Single Port RAM Design in Read First Mode
24. Single Port RAM Design in Write First Mode
25. Single Port RAM Design in No Change Mode
26. Single Port RAM Design With Asynchronous Read
27. Single Port RAM Design With False Asynchronous Read
28. Single Port Block RAM Design With Enable
29. Dual Port RAM With Asynchronous Read
30. Dual Port RAM With False Synchronous Read
31. Dual Port RAM With Synchronous Read
32. ROM Design With Registered Output
33. ROM Design With Registered Address

Module VII: Floorplaning, Routing, Placement (13 Hours)

Theory

Clock Distribution, Power Distribution, Packaging and Pads

Practice

34. RTL Design of PLAs

Text Books

1. Bhasker, J., "Verilog HDL Synthesis: A Practical Primer". Star Galaxy Publishing,1998
2. Camposano, R. and Wolf, W. eds., "High-Level VLSI Synthesis" (Vol. 136). Springer Science & Business Media,2012

3. Sherwani, N.A., "Algorithms For VLSI Physical Design Automation". Springer Science & Business Media,2012

Session Plan:

Topic	**No. of Sessions** (in hrs.)	**Activity**	**Assignment**	**Suggested Reading**
Module I [4 Hrs. Lecture+8 Hrs. Practice]				
Hdl Architecture Design Sub System Design, Hardware Description Language (HDLs), Register Transfer Design, Pipeline and Data Path	4	**Lecture**	Assignment-1.1	
RTL Design of 4-Bit,8-Bit and 16-Bit ALU and Their Performance Evaluation	8	**Practice**		
Module II [3 Hrs. Lecture+8 Hrs. Practice]				
HDL Architecture Design Adders, Multipliers, Memories, PLA, Buses and Network On Chips	3	Lecture	Assignment-2.1	
RTL Design of Data Path Architecture	8	Practice		
Module III [4 Hrs. Lecture+8 Hrs. Practice]				
Static Time Analysis (STA) Timing And Delay And The Concept Of STA, Types of Delay, Models-Distributed, Lumped	4	Lecture	Assignment-3.1	
RTL Design of Any Pipelined Architecture and Its Performance Evaluation	8	Practice		
Module IV [4 Hrs. Lecture+8 Hrs. Practice]				
Static Time Analysis(STA) Pin To Pin Delay Model, Path Delay Modelling, Timing Checks Delay Back Annotations.	4	Lecture	Assignment-4.1	
RTL Design Of Various Adder: Topologies/Architectures Ripple Carry Adder, Carry Skip Adder Carry Increment Adder, Carry Look Ahead Adder, Carry Save Adder Carry Select Adder, Carry Bypass Adder Ling Adder, Prefix Adder, Parallel Prefix	8	Practice		

Adder ,Conditional Sum Adder				
Module V [5 Hrs. Lecture+10 Hrs. Practice]				
Floorplaning, Routing, Placement Advanced Simulations , Coding for Synthesis , Synthesis Optimization	5	Lecture	Assignment-5.1	TB-3 (Ch. 6,7,8)
RTL Design of Various Multiplier Architectures Booth Multiplier, Combinational Multiplier , Wallace Tree Multiplier RTL Design of Various Multiplier Architectures: Array Multiplier Sequential Multiplier , Serial Parallel Multiplier , MAC Unit Design	10	Practice		
Module VI [5 Hrs. Lecture+10 Hrs. Practice]				
Floorplaning, Routing, Placement Floor Planning & Place and Route Optimization , Floorplaning Styles and Methodology , Global Routing	5	Lecture	Assignment-6.1	TB-3 (Ch.6,7,8)
RTL Design Of Various Memory Units Single Port RAM Design In Read First Mode Single Port RAM Design in Write First Mode Single Port RAM Design in No Change Mode Single Port RAM Design With Asynchronous Read Single Port RAM Design with False Asynchronous Read Single Port Block RAM Design With Enable Dual Port RAM With Asynchronous Read , Dual Port RAM With False Synchronous Read , Dual Port RAM With Synchronous Read ROM Design With Registered Output ROM Design With Registered Address	10	Practice		
Module VII [5 Hrs. Lecture+8 Hrs. Practice]				
Floorplaning, Routing, Placement	5	Lecture	Assignment-	TB-3

Clock Distribution, Power Distribution, Packaging and Pads.			7.1	(Ch.11)
RTL Design of PLAs	8	Practice		
Total (In Hrs.)	**90**	**30 Hrs. Lecture and 60 Hrs. Practice**		

System VERILOG

Course Title	Code	Type of course	T-P-PJ	Prerequisite
System VERILOG	DEVL403	Theory & Practice	2-2-0	Nil

Objective

- To Make The Student Understand System Verilog Language And Demonstrate How To Build Verification Environment For Performing Verifications Of VLSI Circuits Using SystemVerilog

Learning Outcome

- Students will Be Able to Use Any Simulation or Synthesis Tool that Support System Verilog
- Students will Learn How to Take Advantage of The System Verilog Language to Make RTL Design ad Synthesis More Productive

Evaluation Systems

	Component	% of Marks	Method of Assessment
Internal Examination	Internal Theory	20	Written Examination
	Internal Practice	30(20+10)	Lab Work + Learning Record
External Examination	External Theory	30	Written Examination
	External Practice	20	Lab Work
Total		100	

Course Outline

Module I: Data Types, Array, Queue (16 Hrs.)

Theory

Different Data Types, User-Defined and Enumerated Types: String Data Types, Event Data Types, User-Defined Types, Enumerated Types, Nets, Reg, Logic, Type Casting, Constants, Attributes.

Array: Packed Array and Unpacked Array, Dynamic, Associate Array, Its Methods, QUEUE Operators and Expressions, Control Structure: If-Else, Switch. Loop

Practice

1. Write A Program to Find Out the Frequency of Character in a String
2. Write A Program to Remove All Characters From a String Keeping All Numbers

Module II: **Tasks and Functions (10 Hrs.)**

Theory

Tasks, functions, Enhancements to tasks and functions, Task and function argument passing, Import and export functions, System Tasks and System Functions

Practice

3. Write a Program to Convert Celsius To Fahrenheit Using Simple Task
4. Write a Program to Calculate Parity Using Function

Module III: Processes (12 Hrs.)

Theory

Combinational Logic, Latch Logic, Sequential Logic, Fork Join (Join, Join_Any, Join_None), Event Controls, Process Control

Practice

5. Write a Program to Dynamically Reverse the Bit Position in System Verilog
6. Write a Program to Write a Program Contents of Two Registers With and Without a Temporary Register

Module IV: Object Oriented Programming (16 Hrs.)

Theory

OOP Basics, Classes-Object and Handles, Polymorphism, Inheritance, Composition, Creating New Object, Object Deallocation, Static Variables Vs. Global Variables, Class Routines, Defining Routines Outside Of The Class, Using One Class Inside Another, Dynamic Objects, Public Vs. Private

Practice

7. Write a Program to Show Inheritance and Polymorphism by Creating an Object
8. Write a Program Showing The Use Of Class Properties by Creating an Object and Deleting that
9. Write a Program and Declare a Static and Global Variable and Show their Use in Subroutine
10. Write a Program of 2 Numbers by Using Class Object Concept
11. Write a Program to Show Arithmetic Operations Using Class Subroutines

Module V: Interface (14 Hrs.)

Theory

Clocking Blocks, Program Block, Interface Concepts, Interfaces: Interface Declarations, Using Interfaces as MODULE Ports, Instantiating and Connecting Interfaces, Referencing Signals Within an Interface, Interface Modports, Using Tasks and Functions in Interfaces, Parameterized Interfaces, Virtual Interfaces, Using Procedural Blocks in Interfaces, Reconfigurable Interfaces, Verification With Interfaces

Practice

12. Write a Program to Perform a Multiplication Using Function of a Class

13. Write a Program to Perform an Event At 20ns Using Task of a Class
14. Write a Program to Show the Difference Between Task and Function

Module VI: Randomization (14 Hrs.)

Theory

Randomization, Constraints: Randomization in Systemverilog, Constraint Details, Controlling Multiple Constraints, Common Randomization Problems, Iterative and Array Constraints, Random Controls, Random Generators, Random Device Configuration

Practice

15. Write a Program by using rand Variables and Randomize them using Randomization Function
16. Write a Program to Show the Difference between rand and randc Variables
17. Write a Program using Constraints within Randomization Variables

Module VII: Coverage (8 Hrs.)

Theory

Semaphores, Mailboxes, Functional Coverage: Coverage Models Cover Points and Bins, Cross Coverage, Regression Testing

Practice

18. Define 3 Bins And Also Their Coverage Points And Find Out The Coverage
19. Write Down the Script which Shows us the Regression Testing
20. Define 4 Bins Which Holds the Coverage Points and Show the Coverage as 50%

Text Books

1. Sutherland, Stuart, Simon Davidmann, and Peter Flake, "SystemVerilog for Design Second Edition: A Guide to Using System Verilog for Hardware Design and Modeling", Springer Science & Business Media, 2006
2. Spear, Chris. "SystemVerilog for Verification: a Guide to Learning the Testbench Language Features," Springer Science & Business Media, 2008

Reference Books

1. System Verilog, 3.1a, Language reference manual
2. Vijayaraghavan, Srikanth, and MeyyappanRamanathan. "A Practical Guide for SystemVerilog Assertions". Springer Science & Business Media, 2005
3. Bergeron, J. "Writing Testbenches Using SystemVerilog.—NY", Springer Science and Busir ness Media." (2006)

Session Plan:

Topic	No. of Sessions	Activity	Assignment	Suggested Reading

	(in hrs.)			
Module I [6 Hrs. Lecture+10 Hrs. Practice]				
Data Types, Array, Queue New Data Types, Tasks and Functions, Interfaces, Clocking Blocks, Different Data Types, User-Defined and Enumerated Types: String Data Types, Event Data Types, User-Defined Types, Enumerated Types, Array: Packed Array and Unpacked Array, Dynamic, Associate Array, Its Methods, QUEUE Operators and Expressions, Control Structure: If-Else, Switch. Loop	6	Lecture	Assignment-1	TB-1 (Ch.5), TB-2 (Ch.2)
Write a Program to Find Out the Frequency of Character in a String Write A Program To Remove All Characters From a String Keeping All Numbers	10	Practice		
Module II [4 Hrs. Lecture+6 Hrs. Practice]				
Tasks And Functions Tasks, Functions, Enhancements to Tasks and Functions, Task and Function, Argument Passing, Import and Export Functions, System Tasks and System Functions, VCD Data Synthesis	4	Lecture	Assignment-2	TB-1(Ch.6)
Write A Program to Convert Celsius to Fahrenheit Using Simple Task Write a Program to Calculate Parity Using Function	6	Practice		
Module III [4 Hrs. Lecture+8 Hrs. Practice]				
Combinational Logic, Latch Logic, Sequential Logic, Fork Join (Join, Join_Any, Join_None), Event Controls, Process Control	4	Lecture	Assignment-3	
Write a Program to Dynamically Reverse the Bit Position in System Verilog Write a Program Contents of Two Registers With and Without a Temporary Register	8	Practice		

Module IV [6 Hrs. Lecture+10 Hrs. Practice]				
Object Oriented Programming Object Oriented Programming: OOP Basics, Classes-Object and Handles, Polymorphism, Inheritance, Composition, Creating New Object, Object Deallocation, Static Variables vs. Global Variables, Class Routines, Defining Routines Outside of the Class, Using One Class Inside Another, Dynamic Objects, Public vs. Private	6	Lecture	Assignment-4	TB-2(Ch.4)
Write a Program to Show Inheritance and Polymorphism by Creating an Object Write A Program Showing the Use of Class Properties by Creating an Object and Deleting that Write a Program and Declare a Static and Global Variable and Show their Use in Subroutine Write A Program of 2 Numbers by Using Class Object Concept Write a Program to Show Arithmetic Operations Using Class Subroutines	10	Practice		
Module V [4 Hrs. Lecture+10 Hrs. Practice]				
Interface Clocking Blocks , Program Block , Interface Concepts, Interfaces: Interface Declarations, Using Interfaces as MODULE Ports, Instantiating and Connecting Interfaces, Referencing Signals Within an Interface, Interface Modports, Using Tasks and Functions In Interfaces, Parameterized Interfaces, Virtual Interfaces, Using Procedural Blocks in Interfaces, Reconfigurable Interfaces, Verification With Interfaces	4	Lecture	Assignment-5	TB-1(Ch.10)
Write a Program to Perform a Multiplication Using Function of a Class	10	Practice		

Write a Program to Perform an Event at 20ns Using Task of a Class Write A Program to Show the Difference Between Task and Function				
Module VI [4 Hrs. Lecture+10 Hrs. Practice]				
Randomization, Constraints: Randomization in System Verilog, Constraint Details, Controlling Multiple Constraints, Common Randomization Problems, Iterative and Array Constraints, Random Controls, Random Generators, Random Device Configuration	4	Lecture	Assignment-6	TB-2(Ch.6)
Write a Program by Using Rand Variables and Randomize them Using Randomization Function Write a Program to Show the Difference Between Rand and Randc Variables Write a Program Using Constraints Within Randomization Variables	10	Practice		
Module VII[2 Hrs. Lecture+6 Hrs. Practice]				
Coverage Semaphores, Mailboxes, Functional Coverage: Coverage Models, Cover Points and Bins, Cross Coverage, Regression Testing	2	Lecture	Assignment-7	TB-1(Ch.12)
Define 3 Bins and Also their Coverage Points and Find Out the Coverage Write Down the Script Which Shows us the Regression Testing Define 4 Bins Which Holds the Coverage Points and Show the Coverage as 50%	6	Practice		
Total (In Hrs.)	**90**	**30 Hrs. Lecture & 60 Hrs. Practice**		

VLSI Verification Methodologies

Course Title	Code	Type of course	T-P-PJ	Prerequisite
VLSI Verification Methodologies	DEVL0201	Practice	0-2-0	Nil

Objective

- The Objective of this Course ss to Involve Students in Theory and Practice of Verifications VLSI Circuits Using Methods Such as Universal Verification and Open Verification Methodology

Learning Outcome

- Student will Gain Knowledge of Various Verification Techniques Employed for Verifying VLSI Chips
- Students will Develop Skills of Performing Verification of the Complex VLSI Chips.

Evaluation Systems

Internal Examination	Component	% of Marks	Method of Assessment
	Internal Practice	50 (40+10)	Lab work + Learning Record
External Examination	External Practice	50	Lab work
Total		**100**	

Course Outline

Module I: (5 Hours)

Practice

History of Testing, Introduction to Universal Verification Methodology (UVM): Typical UVM Testbench Architecture, UVM Library Class

Module II: Introduction to UVM(10 Hours)

Practice

UVM Basics: UVM TB Architecture, Creating UVCs and Environment, Creating agent, UVM simulation phases, Test Flow

Module III: Transaction Level Modelling (TLM) (10 Hours)

Practice

Overview, TLM, TLM1, Merit, Demerit, TLM 2, Implementation

Module IV **(10 Hours)**

Practice
Creating and Using UVM Testbench: Configuring UVM Environment: UVM Sequences, UVM Sequencers, Connecting DUT-Virtual Interfaces, Virtual Sequences and Sequencers, Transaction Class

Module V **(10 Hours)**

Practice
Creating and Using UVM Testbench: Creating UVM Environment: Building a Scoreboard, Building Reusable Environments, Connecting Multiple UVCs

Module VI **(7 Hours)**

Practice
Use of Verification Components: Test Plan And Coverage: Creating Test Plan from Specification Coverage: Code Coverage and Functional Coverage

Module VII **(8 Hours)**

Practice
Assertion Based Methodology: Immediate Assertion, Simple Assertions, Sequences, Sequence composition, Assertion Coverage

Text Books

1. R. Salemi, "The UVM Primer: A Step-By-Step Introduction To The Universal Verification Methodology" Boston Light Press, 2013
2. V.R. Cooper, "Getting Started with UVM: A Beginner's Guide," Austin: Verilab Publishing, 2013
3. H. Height, "A Practical Guide To Adopting The Universal Verification Methodology (UVM)" Lulu. Com, 2010
4. C. Spear, "SystemVerilog for verification: A Guide to Learning The Testbench Language Features," Springer Science & Business Media, 2008

Session Plan:

Topic	**No. of Sessions** (in	**Activity**	**Suggested Reading**

	hrs.)		
Design of UART Protocol by using Verilog		Practice	
Design of I2C master Protocol by using Verilog		Practice	
Design of I2C slave Protocol by using Verilog		Practice	
Design of Asynchronous FIFO by using Verilog		Practice	
Designs of SPI protocol Transmitter by using Verilog		Practice	
Design of DMA by using Verilog		Practice	
Verification of UART Protocol by using UVM		Practice	
Verification of I2C master Protocol by using UVM		Practice	
Verification of I2C slave Protocol by using UVM		Practice	
Verification of Asynchronous FIFO by using UVM		Practice	
Verification of SPI Protocol by using UVM		Practice	
Verification of AMBA AXI Protocol by using UVM		Practice	
Verification of AMBA AHB protocol by using UVM		Practice	
Verification of AMBA APB protocol by using UVM		Practice	
Verification of DMA by using UVM		Practice	
Total(in hrs.)	**60**	**60 hrs. Practice**	

VLSI Test Principle and Testable Design

Course Title	Code	Type of course	T-P-PJ	Prerequisite
VLSI Test Principle and Testable Design	DEVL0102	Theory	3-0-0	Nil

Objective

- To Make the Student Understands Defects and Faults in VLSI Chips Different Test Pattern Generation Techniques and Understand Design-For-Testability.

Learning Outcome

- Students will Be Familiar with the Testing and Verification Methodology of VLSI Circuits
- Student will Develop Skill of Testing Complex Analog, Digital and Mixed Signal Chips

Evaluation Systems

	Component	% of Marks	Method of Assessment
Internal Examination	Internal Theory	30	Written examination
	Assignment	5	Report or Presentation + Learning Record
	Attendance	5	Based on class attended
External Examination	External Theory	60	Written examination
Total		**100**	

Course Outline

Module I: Introduction to VLSI testing, Fault modelling (10 Hours)

Theory

Trends, Moore's Law, Realization, Why Testing, Verification Vs Testing, Ideal Test, Real Test, Level of Testing, Cost of Testing, Role of testing, Real Defects, Faults, Errors and Failures, Overheads, Types, Basic Testing Principle, Design Flow, Characterization, Manufacturing Test, Stress Test, Bathtub Component Failure Curve, Parametric Test, Functional Test, ATPG, Test Specification and Plan, Test Program Generation, Test Data Analysis, Yield, Clustered VLSI Defects, Defect Level

Motivation of Fault Model, Why Fault Model, Some Real Defects, Fault Models, Logic Modelling, Behavioural Fault Models, Functional Level, Structural Level, Stuck at Fault Model, Bridging Fault, Switch Level Fault, Stuck Open/Short Fault, Geometric Fault, Delay Testing, Gate Delay Fault, Path Delay Fault, Redundant Fault, Operational Fault, Fault Collapsing, Fault Dropping, Fault Equivalence, Fault Dominance

Module II: Logic Simulation (5 Hours)

Theory

Basic Concept, Modelling for Simulation, Logic Model of MOS Circuit, Signal States for Simulation, Determining Gate Values, Two Valued Truth Table, True Value Simulation, Compiled Code Algorithm, Logic Levelization Algorithm, Event Driven Simulation, Parallel Simulation of Multiple Vectors

Module III: Fault Simulation (5 Hours)

Theory

Motivation, Uses of Fault Simulator, How to Simulate Fault, Fault Simulation Algorithm, Serial Algorithm, Parallel Fault Simulation, Deductive Fault Simulation, Concurrent Fault Simulation, Critical Path Tracing, Fault Sampling, Random Sampling Model, Probability Density of Sample Coverage, Sampling Error Bounds

Module IV: Testability Analysis (5 Hours)

Theory

Origin, Types of Measures in SCOAP, Range of SCOAP Measures, Controllability and Observability of Basic Gates, Error for Stems and Reconverging Fan-out, Correlation Error, Sequential Example, Combinational and Sequential Controllability and Observability, Testability Computation Algorithm

Module V: Combinational ATPG, Sequential Test Generation (8 Hours)

Theory

Test Generation, Test Pattern, Test Generation Methods, Boolean Difference, Roth's 5 Valued and Muth's 9 Valued Algebra, Deterministic ATPG, Decision Tree for Branch and Bound Search, Backtracking, Common Concepts for Structural Test Generation, Line Justification in a Fanout Free Circuit, Fault Propagation, Backtracking TG Algorithm, D Frontier, J Frontier, D Algorithm, Definition of Singular Cover, D cubes, D Intersection. D and 9V Algorithm Value Computation and Decision Tree, PODEM

Sequential Circuit, Test Generation Method, Time Frame Expansion Method, Implementation of ATPG, Cycle Free Circuits, Asynchronous Model

Module VI: Design for Testability (5 Hours)

Theory

Basic Concept, Ad hoc DFT Method, Structured Method, Scan Path Design, Scan Cell Design, Muxed D Scan FF, Clocked Scan Cell, Level Sensitive Scan Cell. LSSD- Adding Scan Structure in Circuit, Combinational test vectors, Scan Testing Time, Multiple Scan Path, Scan Overheads, Hierarchical Scan, Optimum Scan Layout, Scan Area Overhead, Automated Scan Design, Different LSSD structure, LSSD Design Rule, Advantages and Drawback. Partial Scan Design- Objective, Architecture, Partial Scan Method, MVFS Problem, Test

Generation, Flip Flop for Partial Scan, Random Access Scan(RAS), RAS Flip Flop, Scan Hold Flip Flop

Module VII: Built In Self-Test (7 Hours)

Theory

Motivation, Basic Architecture, Hierarchy, Multipurpose Register Application, Drawback and Advantages, Techniques, Pattern Generation, Exhaustive and Pseudo Exhaustive Method, Random Pattern Testing, LFSR- Types, Analysis using Polynomial Representation, Properties, LFSR as Pseudo Random Pattern Generator, Test Response Compaction- Compaction Techniques, BIST Compression Techniques, Ones Count, Transition Count, Parity Check, Syndrome Check, Signature Analysis, LFSR Response Compacter, MISR, Modular MISR, Multiple Signature Check, Aliasing Probability

BIST Architecture- Built in Logic Block Observer (BILBO), BILBO in Different Modes, STUMS, Circular Self-Test Path BIST

Text Books

1. M. Bushnelland,V.Agrawal, "Essentials of Electronic testing for Digital, Memory and Mixed-Signal VLSI circuits" (Vol. 17),Springer Science & Business Media, 2004
2. M.Abramovici, M.A. Breuer, and A.D.Friedman, "Digital Systems Testing and Testable Design" (Vol. 2). New York: Computer science press,1990

Reference Books

1. N.K. Jha, andS.Gupta,"Testing of Digital Systems", Cambridge University Press, 2003
2. L.T.Wang, C.W. Wu, and X.Wen,. "VLSI Test Principles and Architectures: Design for Testability", Elsevier,2006

Session Plan:

Topic	No. of Sessions (in hrs.)	Activity	Assignment	Suggested Reading
Module I [10 Hrs. Lecture]				
Introduction to VLSI testing, Fault Modelling Trends, Moore's Law, Realization, Why Testing, Verification Vs Testing, Ideal Test, Real Test, Level of Testing, Cost of Testing, Role of testing, Real Defects, Faults, Errors and Failures, Overheads, Types, Basic Testing Principle, Design Flow, Characterization, Manufacturing Test, Stress Test, Bathtub Component Failure Curve, Parametric Test, Functional Test, ATPG, Test Specification and Plan, Test Program Generation, Test Data Analysis, Yield, Clustered VLSI Defects, Defect Level Motivation, Why Fault Model, Some Real Defects, Fault Models, Logic modelling, Behavioural Fault models, Functional Level, Structural Level, Stuck at Fault Model, Bridging Fault, Switch Level Fault, Stuck Open/Short Fault, Geometric Fault, Delay Testing, Gate Delay Fault, Path Delay Fault, Redundant Fault, Operational Fault, Fault Collapsing, Fault Dropping, Fault Equivalence, Fault Dominance	10	Lecture	Assignment 1.1	TB-1 (Ch.4,5)
Module II [5 Hrs. Lecture]				
Logic Simulation Basic Concept, Modelling For Simulation, Logic Model of MOS Circuit, Signal States for Simulation, Determining Gate Values, Two Valued Truth Table, True Value Simulation, Compiled Code Algorithm, Logic Levelization Algorithm, Event Driven Simulation, Parallel Simulation of Multiple Vectors	5	Lecture	Assignment 2.1	TB-1 (Ch.5)
Module III [5 Hrs. Lecture]				

Fault Simulation Motivation, Uses of Fault Simulator, How to simulate fault, Fault simulation Algorithm, Serial Algorithm, Parallel Fault Simulation, Deductive Fault Simulation, Concurrent Fault Simulation, Critical Path Tracing, Fault Sampling, Random Sampling Model, Probability Density of Sample Coverage, Sampling Error Bounds	5	Lecture	Assignment 3.1	TB-1 (Ch.5)
Module IV [5 Hrs. Lecture]				
Testability Analysis Origin, Types of measures in SCOAP, Range of SCOAP measures, Controllability and Observability of Basic Gates, Error for Stems and Reconverging Fan-out, Correlation Error, Sequential Example, Combinational and Sequential Controllability and Observability, Testability Computation Algorithm	5	Lecture	Assignment 4.1	TB-1 (Ch.5,6)
Module V [8 Hrs. Lecture]				
Combinational ATPG, Sequential Test Generation Test Generation, Test Pattern, Test Generation Methods, Boolean Difference, Roth's 5 Valued and Muth's 9 Valued Algebra, Deterministic ATPG, Decision Tree for Branch and Bound Search, Backtracking, Common Concepts for Structural Test Generation, Line Justification in a Fanout free Circuit, Fault Propagation, Backtracking TG Algorithm, D Frontier, J Frontier, D Algorithm, Definition of Singular Cover, D cubes, D Intersection. D and 9V algorithm Value Computation and Decision tree, PODEM	8	Lecture	Assignment 5.1	TB-1 (Ch.7,8)
Module VI [5 Hrs. Lecture]				
Design For Testability Basic Concept, Ad hoc DFT Method, Structured Method, Scan Path Design, Scan Cell Design, Muxed D Scan FF, Clocked Scan Cell, Level Sensitive Scan Cell. LSSD-	5	Lecture	Assignment 6.1	TB-1 (Ch.14)

Adding Scan Structure in Circuit, Combinational test vectors, Scan Testing Time, Multiple Scan Path, Scan Overheads, Hierarchical Scan, Optimum Scan Layout, Scan Area Overhead, Automated Scan Design, Different LSSD structure, LSSD design rule, Advantages and Drawback. Partial Scan Design- Objective, Architecture, Partial Scan Method, MVFS problem, Test Generation, Flip Flop for Partial Scan, Random Access Scan(RAS), RAS Flip Flop, Scan Hold Flip Flop				
Module VII [7 Hrs. Lecture]				
Built In Self-Test Motivation, Basic Architecture, Hierarchy, Multipurpose Register application, Drawback and Advantages, Techniques, Pattern Generation, Exhaustive and Pseudo Exhaustive Method, Random Pattern Testing, LFSR- Types, Analysis using Polynomial Representation, Properties, LFSR as Pseudo Random Pattern Generator, Test Response Compaction- Compaction Techniques, BIST Compression Techniques, Ones Count, Transition Count, Parity Check, Syndrome Check, Signature Analysis, LFSR Response Compacter, MISR, Modular MISR, Multiple Signature Check, Aliasing Probability BIST Architecture- Built In Logic Block Observer (BILBO), BILBO in different Modes, STUMS, Circular Self-Test Path BIST	7	Lecture	Assignment 7.1	TB-1 (Ch.15)
Total (in Hrs.)	**45**	**45 Hrs. Lecture**		