Cache Coherence Protocol Design: A Report

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Abstract

[[One method of enforcing coherence is to ensure that a processor has exclusive access to a data item before it writes that item. This style of protocol is called a write invalidate protocol because it invalidates copies in other caches on a write. Exclusive access ensures that no other readable or writable copies of an item exist when the write occurs: all other cached copies of the item are invalidated.-]]–Patterson, page 468.

bus_invalidate: when a core gets a write hit in its local cache(L1) on shared block, then it broadcats a bus_invalidate requests, to inform other cores that it has updated the block, other core must invalidate their copy. If the core has the data in Modified state, then it can update the data, due to Single Write Multiple Read principle, onle one core can have data in Modified state. So, if the current core has the data in Modified state, no request should be put for invalidation.

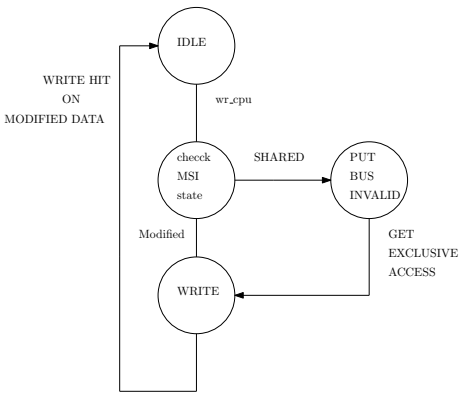

Figure 1: *Individual automatons*