Design and Comparative Analysis of a 16-bit 20 MS/s SAR-ADC Using 45nm CMOS and 32nm CNTFET Technologies for Low-Power Applications.

Jatin Saini
Dept. of Electronics & Communication Engineering
National Institute of Technology
Rourkela, Odisha, India
jatinsaini1706@gmail.com

Debmalya Mandal
Dept. of Electronics and Communication Engineering
National Institute of Technology
Rourkela, Odisha, India
debmalyamandal7434@gmail.com

Alok Kumar Sahu
Dept. of Electronics & Communication Engineering
National Institute of Technology
Rourkela, Odisha, India
aloksahu1443@gmail.com

Dr. Sumit Saha
Dept. of Electronics & Communication Engineering
National Institute of Technology
Rourkela, Odisha, India
sumitsahanitr@gmail.com

***Abstract*—This paper presents a comparative analysis of SAR-ADC circuits implemented using Carbon Nanotube Field-Effect Transistors (CNFETs) 32nm and Complementary Metal-Oxide-Semiconductor (CMOS) 90nm technology. The study aims to evaluate the performance of these technologies in terms of power consumption, size, and propagation delay. The findings offer new insights for enhancing current work by focusing on reducing power consumption and achieving high-speed ADC performance at a 16-bit resolution. Simulations were conducted using the Cadence Virtuoso simulation tool to ensure accurate and reliable results. Our findings indicate that CNFET-based SAR-ADC circuits demonstrate superior performance in terms of speed and power efficiency, particularly at smaller technology nodes. This comparative study provides valuable insights into the trade-offs between CNFET and CMOS technologies, guiding future research and development in the design of high-performance digital circuits.**

Keywords - Comparator, Control logic, DAC, SAR ADC, CNFET, CMOS, Power Consumption, Propagation Delay.

I. INTRODUCTION

In recent years, the rapid advancements in wireless communications, sensor networks, medical devices, and the Internet of Things (IoT) have significantly heightened the demand for high-speed and high-resolution Analog-to-digital converters (ADCs) that can efficiently bridge the gap between the Analog and digital domains [1]. These ADCs are critical in a diverse range of applications, from RF communication and biomedical signal processing to advanced sensor systems, where the precise conversion of Analog signals into digital formats is paramount for ensuring data integrity and system reliability [2]. Among the various ADC architectures, the successive approximation register (SAR) ADC stands out due to its ability to deliver medium-speed, low-power consumption, and high precision, making it particularly suitable for applications that require accurate and reliable digital representation of Analog signals [3].

The SAR ADC architecture is composed of several key components, including a sample and hold (S/H) circuit, a comparator, a digital-to-Analog converter (DAC), and SAR logic, each playing a crucial role in determining the overall performance of the converter [4]. The accuracy and speed of SAR ADCs are heavily dependent on the precision of the DAC and comparator, which directly influence the converter's ability to resolve fine details in the input signal [4]. Design challenges such as power dissipation, process variation, and temperature stability have driven the development of innovative techniques to enhance SAR ADC performance, including dynamic amplification, bootstrapped techniques, and advanced calibration methods [5]. Furthermore, optimizing the trade-off between speed, accuracy, and power efficiency remains a critical area of research, especially as modern applications continue to push the limits of ADC performance, demanding greater miniaturization and enhanced functionality in ever-smaller form factors. In the context of biomedical applications, where the accurate digitization of weak physiological signals is critical for patient monitoring and diagnostics, SAR ADCs have proven to be indispensable components. These applications demand ADCs that maintain high data accuracy and operate at low power to extend battery life in portable and implantable devices, ensuring long-term reliability and patient safety [6]. The ongoing miniaturization of CMOS technology, coupled with the emergence of carbon nanotube field-effect transistors (CNFETs), has further pushed the boundaries of ADC design, enabling the realization of ultra-low voltage. These power-efficient converters meet the stringent requirements of modern mixed-signal systems, addressing the challenges of power-constrained environments while maintaining high-performance standards [3]. The exploration of alternative semiconductor materials like CNFETs also opens new avenues for reducing power consumption and enhancing the speed of ADCs, providing a promising path forward in the continuous evolution of ADC technology.

This study comprehensively evaluates a 16-bit, 500 MS/s SAR ADC designed at a 45-nm CMOS technology node, with a detailed comparison against existing benchmark ADCs. Performance metrics such as signal-to-noise and distortion ratio (SNDR), figure of merit (FOM), and total harmonic distortion (THD) are used to assess the proposed ADC's superiority in power efficiency and overall performance [1]. The findings provide valuable insights that can guide future developments in the design of high-precision, low-power ADCs for a wide range of applications [2]. Moreover, the comparative analysis highlights potential areas for further optimization, especially in scaling down technology nodes and exploring alternative transistor technologies such as CNFETs, which promise to revolutionize the next generation of ADC designs. This research not only contributes to the understanding of current ADC design challenges but also lays the groundwork for future innovations in the field, particularly as the demand for more efficient, smaller, and faster ADCs continues to grow in parallel with advancements in digital technology. These insights are crucial for addressing the increasingly complex requirements of modern electronic systems, where high performance and energy efficiency are paramount.

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II. DESIGN OF SAR ADC

A 16-bit successive approximation register (SAR) ADC transforms the Analog input signal into a corresponding digital representation using a binary search technique. It works by comparing an input voltage to a series of voltage levels produced by a Digital-to-Analog Converter (DAC), starting with the Most Significant Bit (MSB) and proceeding to the Least Significant Bit (LSB) [1]. This method of successive approximation refines the digital output with each comparison, offering high resolution due to its 2^16 or 65,536 discrete levels [6].

A. SAR

- The SAR circuit is a sequential system in ADCs used to determine each bit's value based on the comparator's output.
- For an N-bit ADC, there are 2^N possible output values, requiring at least N flip-flops (FFs).
- Two SAR structures are commonly used: the Sequencer/Code register structure and the non-redundant SAR. This implementation uses the Sequencer/Code register.[7]
- Initially, the first register sets the Most Significant Bit (MSB) to '1' and compares it with the sampled input. The comparator output decides if the MSB remains '1' or resets to '0'.
- The reset input controls FF1, setting the first code register flip-flop (CF1) to output the MSB. FF1's output transitions trigger the next FF, continuing the process for all N-bits.[6]
- Positive edge-triggered D flip-flops are used to ensure proper timing and functionality of the circuit.

B. Operational Amplifier

- Operational amplifiers (op-amps) are crucial for enhancing circuit performance and gain.[12]
- A Multi-stage Amplifier configuration typically includes coupling capacitors, a tail circuit, and a common source amplifier, all contributing to increased gain and signal amplification.[1]
- Differential amplifiers focus on amplifying the difference between two input signals while rejecting noise.
- Adding a Coupling Capacitor (Cc) and resistor (R) further improves the output swing and gain.[13]

C. Comparator

- The comparator compares the DAC output with the input voltage to set the MSB.[3]
- Speed and accuracy are crucial for ADC performance.
- Our design uses a shared charge-based double tail dynamic latch comparator for better performance and lower power consumption.[4]
- It features a dynamic latch, differential transistor pair, regenerative feedback, and a Widlar current mirror for enhanced linearity and reduced current mismatch.[11]

D. Sample and Hold

- A CMOS-based sample and hold circuit uses transmission gates and a sampling capacitor to prevent charge injection errors.
- A dummy switch, controlled by an inverted clock, absorbs charge injection and eliminates glitches.[6]
- The circuit consists of a sampling switch, hold capacitor, voltage follower, and unity gain buffer.[9]
- The sampling switch, driven by a positive clock (CLK), samples a 10 MHz, 1 V P-P signal. During saturation, only the source junction is affected if connected to the hold capacitor [1].

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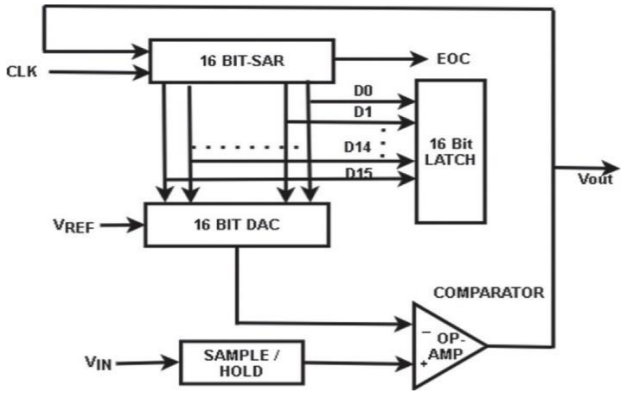

Figure 1 : Architecture of 16 Bit SAR-ADC.

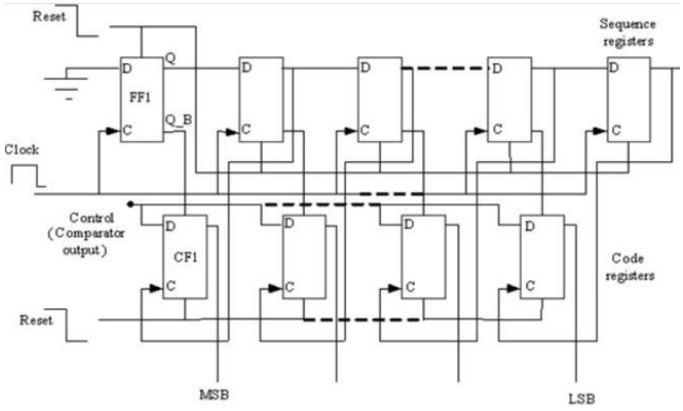

Figure 2: Schematic of SAR

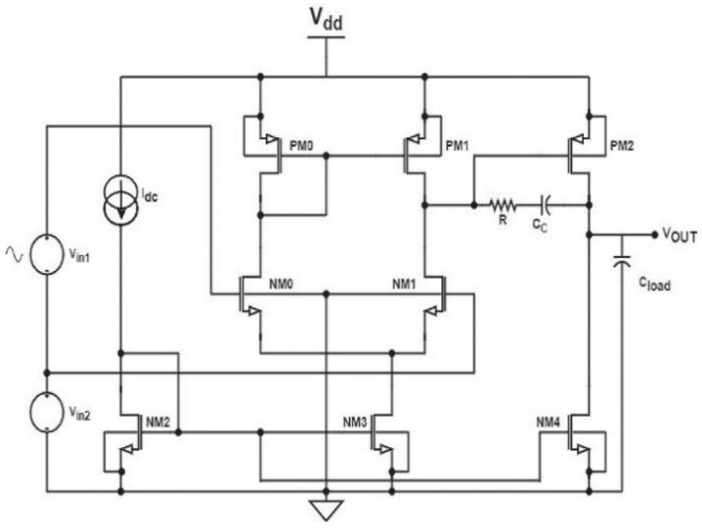

Figure 3: Multistage Operational Amplifier

- In sampling mode, the output mirrors the input, while in hold mode, the op-amp output is turned off to prevent charging errors [9].
- The hold capacitor maintains charge with the op-amp output at high impedance, and the unity gain buffer ensures voltage stability [10].

E. Digital to Analog Converter (DAC)

- A CMOS sample and hold circuit with transmission gates and a sampling capacitor minimizes charge injection errors.
- A dummy switch, driven by an inverted clock, absorbs charge injection and prevents glitches.[11]
- The circuit includes a sampling switch, hold capacitor, and unity gain buffer, sampling a 10 MHz, 1 V P-P signal.
- During saturation, only the source junction is affected if connected to the hold capacitor [8].
- The op-amp output is turned off in hold mode to prevent charge errors, with buffer maintaining voltage stability [6].

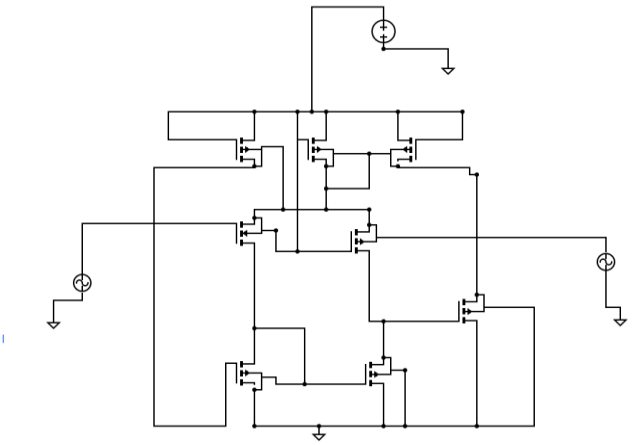

Figure 2 : Schematic of Sample and Hold circuit

III. METHODOLOGY

A. Design implementation using CADENCE VIRTUOSO

The SAR-ADC circuit was designed using two distinct technologies: 45nm CMOS and 32nm CNTFET, within the Cadence Virtuoso environment. Initially, the 16-bit SAR-ADC architecture was implemented using conventional 45nm CMOS technology to establish a baseline performance. The CNTFET models were then integrated into the Cadence environment for the 32nm node, with custom Verilog-A code to accurately represent the unique properties of CNTFETs. This integration allowed for the seamless use of these models in both schematic and layout design phases. Custom schematics and symbols were created for the CNTFET-based SAR-ADC components.[1] This involved defining critical electrical parameters, including threshold voltage, channel Width-to-Length (W/L) ratio, and other process-specific characteristics. The design process also involved organizing the circuit components into new modules and libraries, ensuring a modular and hierarchical design approach. This was crucial for maintaining clarity and facilitating future modifications or scalability in the design. For both the CMOS and CNTFET designs, key parameters such as the supply voltage, rise and fall times of the input pulse, and the pulse width were chosen to match the operating conditions of a high-speed 500MS/s SAR-ADC.

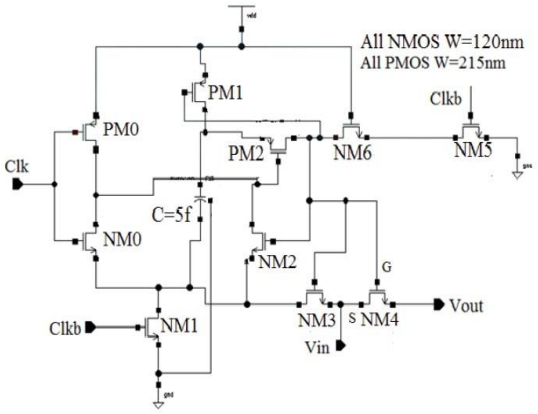

Figure 5: Comparator of 16 Bit SAR-ADC.

Transient analysis was performed on both CMOS and CNTFET-based SAR-ADC circuits to observe their time-domain behaviour. This analysis was essential for understanding the circuit's response to rapid changes in the input signals, which directly impacts the accuracy and speed of the ADC. The input and output voltage waveforms were plotted, and from these, critical performance metrics like propagation delay and power consumption were extracted. Propagation delay was calculated by analysing the timing difference between the transitions in the input and output signals, particularly focusing on when the signals crossed predefined voltage thresholds. Power consumption was assessed by examining the current drawn by the circuit throughout its operation, with specific attention to dynamic power consumption, as it plays a significant role in high-speed ADC designs. Finally, a comparative analysis was conducted between the 45nm CMOS and 32nm CNTFET technologies. This comparison highlighted the impact of technology scaling on the SAR-ADC's performance, particularly focusing on trade- offs between speed, power consumption, and overall

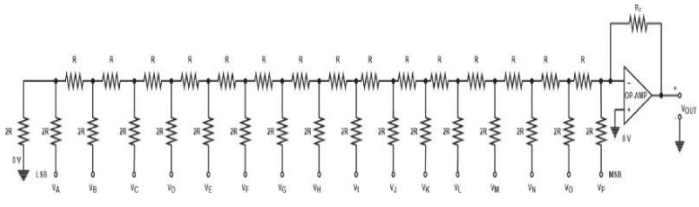

Figure 3 : Schematic of R-2R Ladder DAC.

efficiency. The results provided insights into the benefits and challenges associated with transitioning from conventional CMOS technology to CNTFETs, especially in the context of low-power, high-speed ADC applications.

IV. Simulation Results and Discussion

The following simulation results were obtained and observed with different supply voltage and pulse voltage set in all circuits using Cadence Virtuoso.

A. Comparative Analysis

In this section, we have presented a comparative analysis of the simulation results for the SAR ADC circuit implemented using Carbon Nanotube Field-Effect Transistors (CNFETs) and Complementary Metal-Oxide-Semiconductor (CMOS) technology at 45nm and 32nm technology nodes.

1. Power Consumption

From the simulation results, it is evident that the SAR-ADC's power consumption at 45nm CMOS technology is higher than at 32nm CNFET technology. Specifically, there is an 11.74% reduction in power consumption when moving from 45nm CMOS (93.57 µW) to 32nm CNFET (82.58 µW) at the same sampling rate of 20 MS/s. This comparison underscores the significant efficiency gains achievable through technology scaling.[16] The transition from 45nm CMOS to 32nm CNFET demonstrates the advantages in power reduction, making 32nm CNFET a more suitable choice for low-power, high-speed ADC applications. Detailed power consumption data are summarized in Table [1].

2. Signal-to-Noise Ratio (SNR):

Signal-to-Noise Ratio (SNR) is a measure of how much the desired signal stands out from the background noise in an ADC. It is defined as the ratio of output power and noise power in decibels(dB). A higher SNR indicates that the ADC can more effectively distinguish the signal from noise, resulting in clearer and more accurate digital output.[20] In a well-designed SAR-ADC using 45nm CMOS technology, the value of SNR above 70 dB is typically expected, ensuring good signal clarity and minimal noise interference. In our observation, the value of SNR was found to be 98.08dB.[17] For an N-Bit ADC system,

SNR (in dB) = 6.02*N +1.76;
where N is the resolution bits of ADC [17].

3. Effective Number of Bits (ENOB):

The effective Number of Bits (ENOB) represents the actual resolution of an ADC, accounting for all noise sources and imperfections in the conversion process. ENOB is crucial for understanding the real precision of the ADC beyond its nominal bit resolution.[1] For a high-quality SAR-ADC in 45nm CMOS technology, an ENOB of at least 10 bits is desirable, which translates to a high degree of accuracy in the digital representation of the analog input signal.[19] In this observation, the value of ENOB is 17.88.[17]

4. Total Harmonic Distortion (THD):

Total Harmonic Distortion (THD) measures the extent of distortion introduced by the ADC during the conversion process. It quantifies the unwanted harmonics in the output signal that are not present in the original Analog input.[1] Lower THD values indicate better fidelity and less distortion. For a good SAR-ADC design in 45nm CMOS technology, a THD below -80 dB is expected, signifying minimal

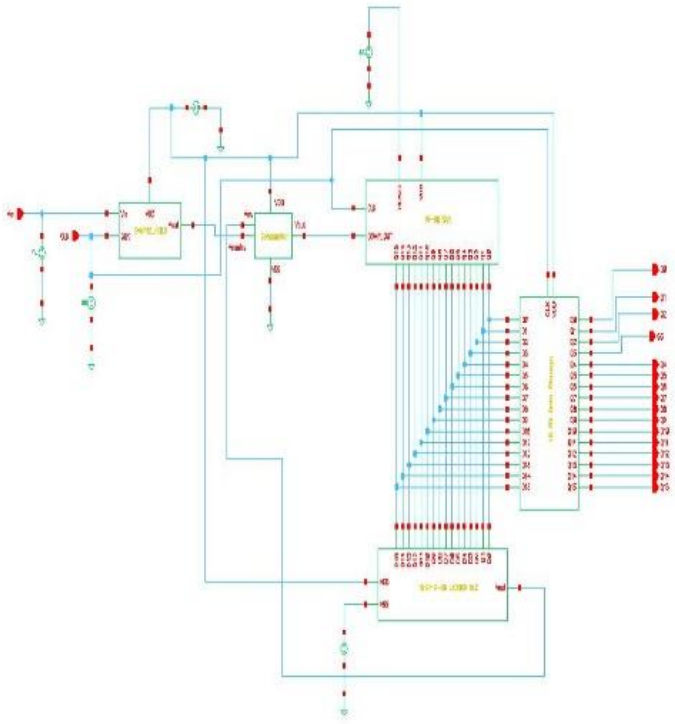

Figure 7: Schematic of SAR-ADC Block Diagram.

Source	Y Shen *et al* [18]	Y -H Chung *et al* [19]	P Zhang *et al* [20]	This Work
Architecture	Analog-detection-based input range compensation	Binary-window digital-to-analog converter (DAC) switching schemes	Monotonic and traditional switching	Low-power and High Frequency16-Bit SAR-ADC (Analog -to-Digital Converter)
Technology [nm]	65 nm	180 nm	180 nm	45nm
Supply Voltage	0.8 V	1.8 V	5 V	1.8V
Resolution (bits)	14	16	16	16
Sampling rate [mega sample/s]	128 KS s^{-1}	1 MS s^{-1}	1 MS s^{-1}	20MS/s
Power Consumption	0.65 μW	1.05 mW	40 mW	93.57uW
SNR	93 dB	100 dB	107.9 dB	98.08dB
FOM (fJ/Conv-step)	9.57	169.8	166.3	-------

Table 1: Comparison of proposed SAR-ADC with existing SAR-ADC's.

distortion and high accuracy in the digitized output.[17]

B. Simulation Result:

1. Successive Approximation Register (SAR)
   A transient analysis was performed for 16-bit SAR ADC as shown in figure (8). The supply voltage (VDD) had been taken at 1.8 V, Clock pulses were taken having 80 nS as period and pulse width of 35 nS with no delay. Preset was given a delay of 45nS and for the rest of the simulation time, it was logic high (1.8V). The simulation had been run giving comparator output as 0(active low) and it lasted for 480nS. At the output, D15 had become high initially and when it was triggered to low, D14 had triggered to high, and the other bits triggered in the same manner up to the end of the simulation.

2. Comparator
   A transient analysis was performed for the Comparator circuit for low power 16Bit SAR-ADC as shown in Figure (9). The input supply voltage of 1.8V had been given with an input sine wave of frequency 10MHz and a pulse wave of the same frequency having pulse width 65nS. The Comparator was a multistage Operational Amplifier having a Common-mode range of 0.8mV to 1.6V. The supply current was 20uA having a load capacitance of 1pF. The output waveform was a pulse wave having only high and low values in the output. The high value was for Vin > Vclock and the Low value was for Vin < Vclock. The simulation time was taken 1uS.

3. Sample and Hold
   A transient analysis was performed for the Sample and Hold circuit designed for low-power SAR-ADC using COMS as well as CNFET technology as shown in Figure (10). For the Sample and hold circuit, an input Sinusoidal waveform having amplitude of 500 mV and DC amplitude of 1 V had been taken. For sampling, clock pulses of frequency 10MHz and pulse width of 50nS were used. The output of this simulation was shown in the figure. The simulation time was taken to be 3uS with an input supply voltage of 1.8V.

4. DAC
   A transient analysis was performed for 16Bit R-2R Ladder DAC to check waveform and calculate power consumption, as shown in figure (11). 16 clock pulses were given as an input to the circuit and the staircase output was observed in this simulation. The Supply voltage and the reference voltage were given 1.8V. In the ladder circuit, the resistances were given maintaining a 2:1 ratio for vertical and horizontal elements. The vertical resistances were valued at 30kOhms and the horizontal ones were 15kOhms. The power consumption by the entire DAC circuit during the simulation time of 25uS was 10.87uWatts, which can be considered as low power for SAR-ADC design.

Device\Parameters	Resolution	Sampling Rate	Power Consumption	Supply Voltage	SNR
LTC2378–16 Analog Devices	16 bits	500 KSPS	10.5 mA	5 V	98 dB
ADS8881 Texas Instruments	16 bits	500 KSPS	12.5 mA	5 V	93 dB
LTC2380–16 Analog Devices	16 bits	1 MSPS	5.5 mW	3.3 V	96 dB
MAX11046 Maxim Integrated	16 bits	500 KSPS	1.1 mW	3.3 V	94 dB
ADS8344 Texas Instruments	16 bits	1 MSPS	2.5 mW	5 V	91 dB
LTC2368 Analog Devices	16 bits	500 KSPS	1.2 mW	5 V	96 dB
MAX11156 Maxim Integrated	16 bits	500 KSPS	140 μA	3 V	94.5 dB
Proposed SAR-ADC	16 bits	20 MSPS	93.57uW	1.8 V	98.08dB

Table 2: Comparison of proposed SAR-ADC with Used SAR-ADC in real

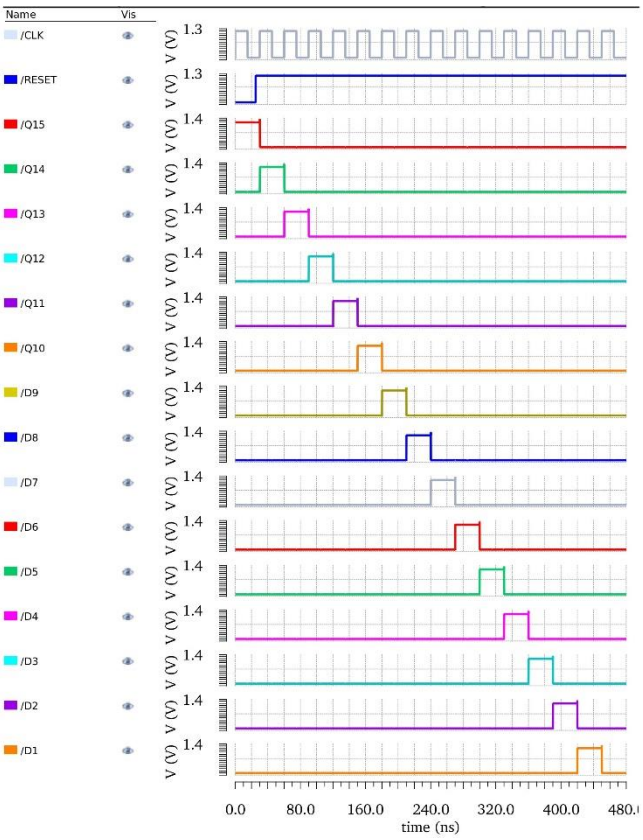

Figure 8: Output Waveform of Successive Approximation Register (SAR)(16-Bit)

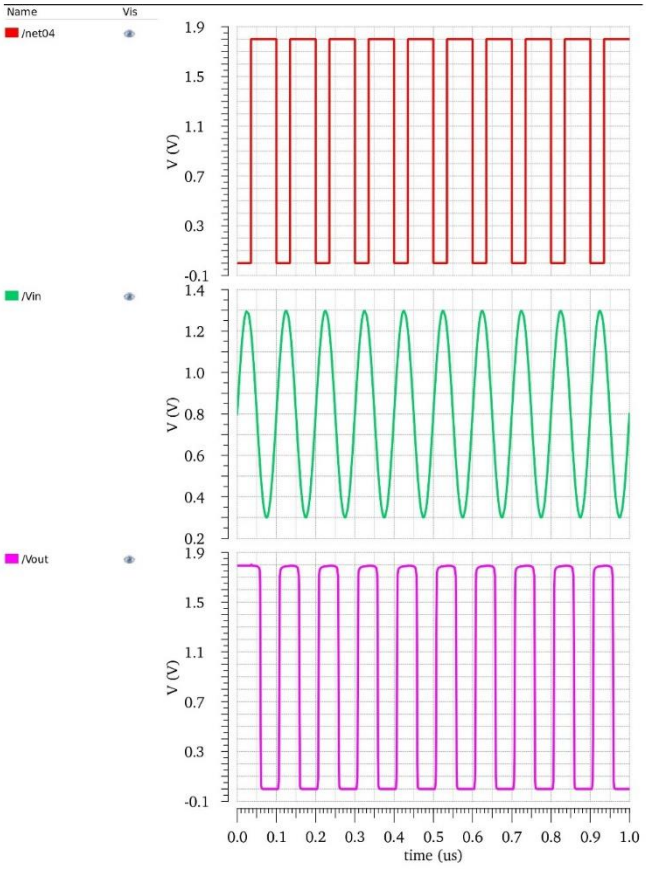

Figure 9: Comparator Output

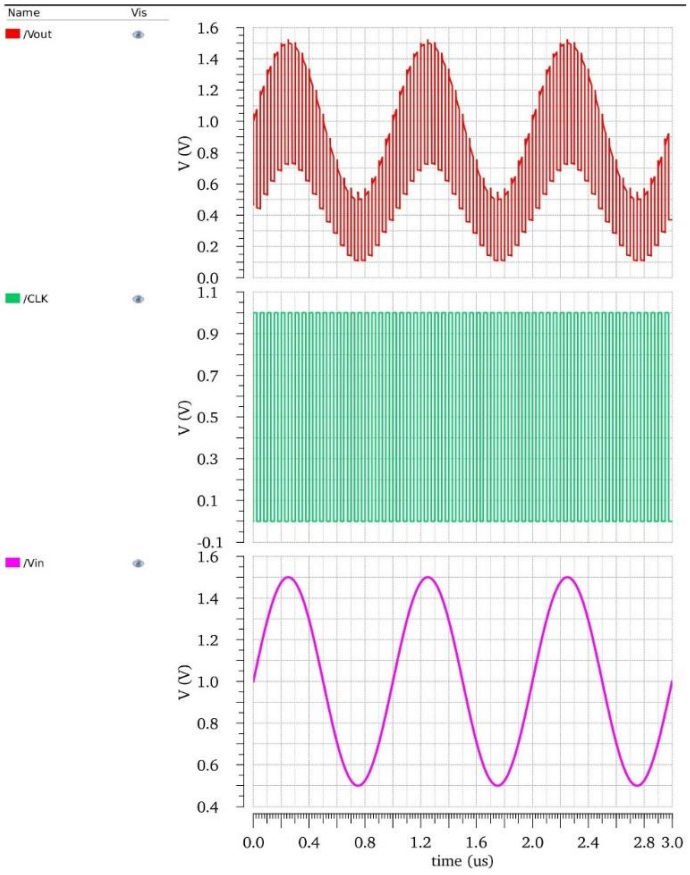

Figure 10: Transient analysis of sample and hold circuit.

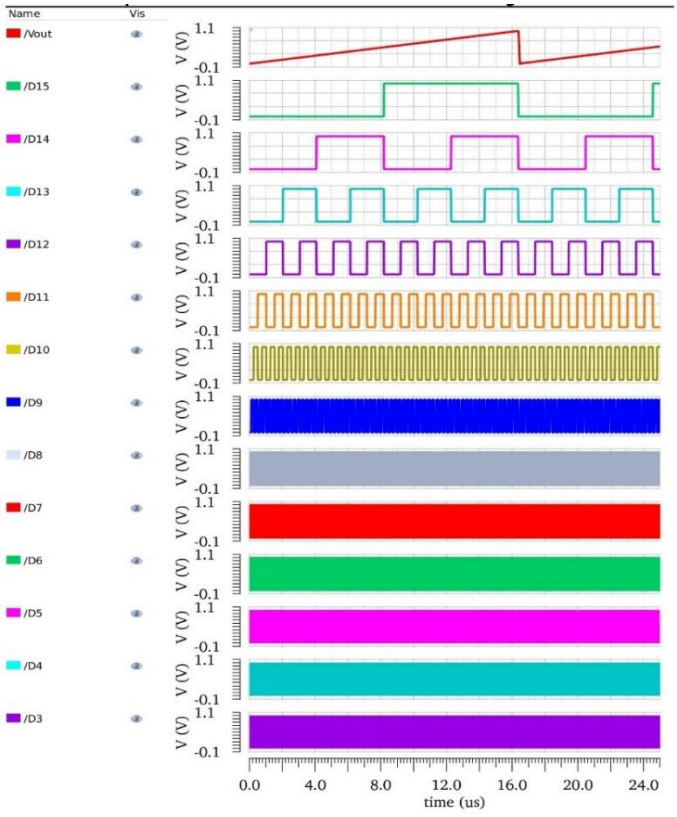

Figure 11: 16-Bit R-2R ladder DAC output waveform.

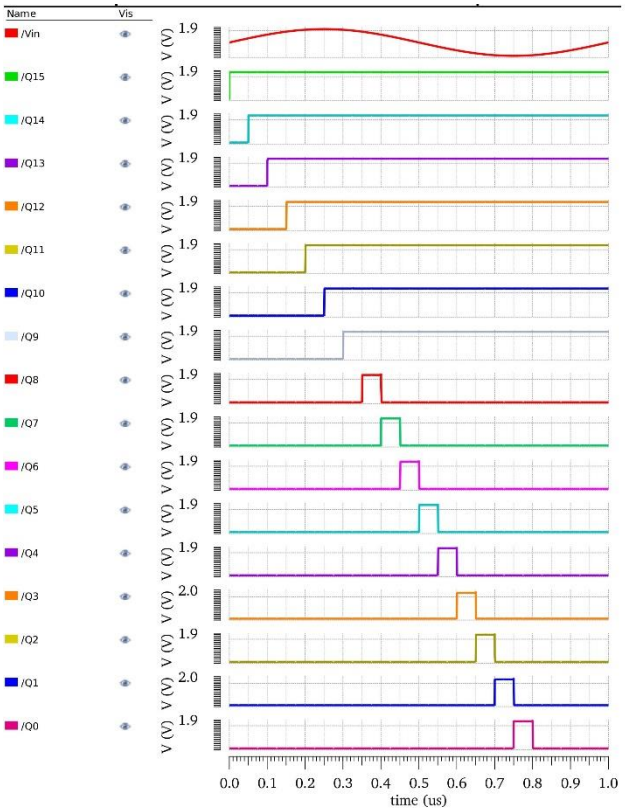

Figure 12: 16-Bit SAR ADC Output

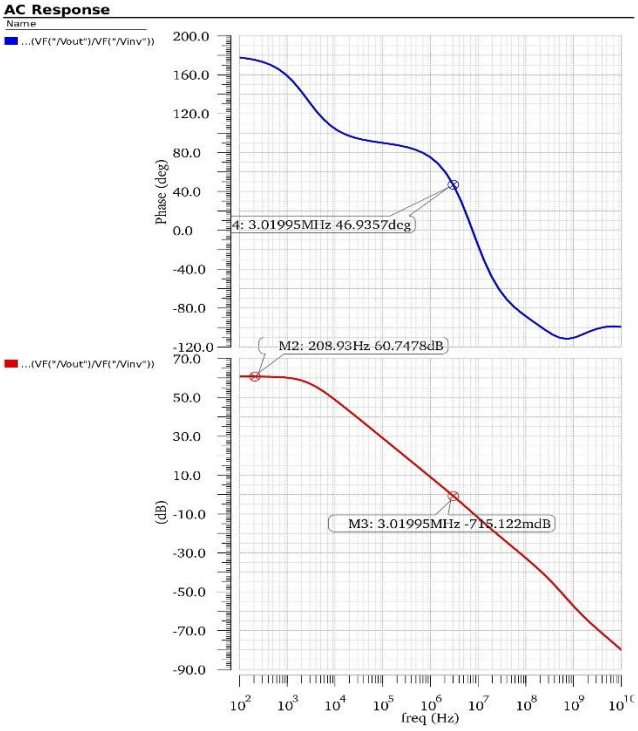

Figure 13: AC Response of Multistage OPAMP.

V. CONCLUSION

The proposed SAR ADC stands out in Analog-to-digital conversion, offering remarkable features such as a fast sampling rate of 20MS/s and low power consumption of 39.2µW. The high sampling rate allows the ADC to capture high-frequency signals accurately, making it ideal for real-time applications. Its low power consumption extends the lifespan of the integrated circuit (IC) and reduces the demand for power supply backups, which is especially beneficial for energy-efficient applications like portable devices or IoT sensors. The ADC also delivers excellent linearity, ensuring that the digital output closely matches the Analog input, providing reliable measurements. Operating at a supply voltage of 1.8 V, the ADC achieves an impressive Total Harmonic Distortion (THD) of −97.97 dB, indicating minimal signal distortion and reinforcing the accuracy of the conversion. The combination of high resolution, fast sampling rate, low power consumption, and strong linearity makes the proposed SAR ADC an accurate choice for various applications where high-quality, low-power Analog-to-digital conversion is required, such as industrial automation systems, medical devices, and audio processing.

Advancements in the uniformity and alignment of CNFETs are expected to significantly improve the reliability of CNFET circuits. This progress will enhance their resilience to environmental factors, making CNFET circuits more suitable for critical applications. Moreover, CNFETs could play a crucial role in the development of control circuits for quantum computing systems and in enhancing neuromorphic architectures, which aim to replicate brain-like functionality. Being derived from carbon nanotubes, CNFETs present a potentially eco-friendly alternative to traditional silicon-based electronics, contributing to the growth of sustainable environment technology. In summary, our comparative analysis sheds light on the performance trade-offs between CMOS and CNFET technologies in various cases for SAR-ADC circuit implementation.

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