SW6224 Register List

1. History

V1.0: initial version for IC version 3;
V1.1: modify some description of Reg0x12;
V1.2: for IC version 5;
V1.3: update company logo;
V1.4: for IC verison 6;
V1.5: update document template;
V1.6： modify some descriptions of Reg0x2D[2] and modify default values;

2. Register

Note: reserved bits should not be modified

2.1. REG 0x03: Key Config

Bit	Description	R/W	Default
7-6	Double click function definition 0: close boost 1: enter trickle current charge 2: open WLED 3: open trickle current charge piror to WLED if both modes enable	W/R	0x0
5-4	Longkey function definition 0: open trickle current charge piror to WLED if both modes enable 1: close boost 2: enter trickle current charge 3: open WLED	W/R	0x0
3-2	Short key event mapping usb plug 0/2: only open port A when short key event 1/3: nothing happen when short key event Note: Csrc(unloading) restart when short key event	W/R	0x0
1	Short key timing configuration 0: 32ms ~ 300ms low level 1: 32ms~500ms low level	W/R	0x1
0	Response to short key event enable 0: no response 1: response according to reg0x03[3:2] Note this bit is valid only when discharger port opened	W/R	0x1

2.2. REG 0x04: Short Key Event

Bit	Description	R/W	Default
7-1	/	/	/
0	I2C write short key event 0: nothing 1: short key event This bit is automatically cleared by hardware	W/R	0x0

2.3. REG 0x06: Led Status Indication

Bit	Description	R/W	Default
7-5	/	/	/
4	IRQ pin status 0: IRQ pin high 1: IRQ pin low Note this bit is 1 when led open.	R	0x0
3	Undefined bit This bit can be written and read	W/R	0x0
2	Charger status indication(debounce) 0: charger off 1: charger on	R	0x0
1	Led work status indication 0: led close 1: led open	R	0x0
0	/	R	0x0

2.4. REG 0x07: Key Event Status

Bit	Description	R/W	Default
7-3	/	/	/
2	short key pending bit This bit is cleared by writing 1	W/R	0x0
1	double click pending bit This bit is cleared by writing 1	W/R	0x0
0	long key pending bit This bit is cleared by writing 1	W/R	0x0

2.5. REG 0x08: Port Plug Out Status

Bit	Description	R/W	Default
7-6	/	/	/
5	Port Csnk plug out pending bit(SW6224 as sink) This bit is cleared by writing 1	W/R	0x0
4	/	/	/
3	Port B plug out pending bit This bit is cleared by writing 1	W/R	0x0
2	Port Csrc plug out pending bit(SW6224 as source) This bit is cleared by writing 1	W/R	0x0
1	/	/	/
0	Port A plug out pending bit This bit is cleared by writing 1	W/R	0x0

2.6. REG 0x09: Port Plug In Status

Bit	Description	R/W	Default
7-6	/	/	/
5	Port Csnk plug in pending bit This bit is cleared by writing 1	W/R	0x0
4	/	/	/
3	Port B plug in pending bit This bit is cleared by writing 1	W/R	0x0
2	Port Csrc plug in pending bit This bit is cleared by writing 1	W/R	0x0
1	/	/	/
0	Port A plug in pending bit This bit is cleared by writing 1	W/R	0x0

2.7. REG 0x0A: BAT Anormal Case

Bit	Description	R/W	Default
7-5	/	/	/
4	vbat overvoltage (more than 4.6v in low voltage protocol) pending bit This bit is cleared by writing 1	W/R	0x0
3	NTC overtempt pending bit This bit is cleared by writing 1	W/R	0x0
2	charger overtime pending bit This bit is cleared by writing 1	W/R	0x0

1	vbat overvoltage pending bit This bit is cleared by writing 1	W/R	0x0
0	charger full event pending bit This bit is cleared by writing 1	W/R	0x0

2.8. REG 0x0B: System Anormal Case0

Bit	Description	R/W	Default
7	/	/	/
6	dvdd OVP cleared bit writing 1 to this bit, reg0x21[5] will be cleared. Note reg0x21[5] is dvdd OVP pending bit	W/R	0x0
5	/	/	/
4	vbus C overvoltage pending bit This bit is cleared by writing 1	W/R	0x0
3	vbus B overvoltage pending bit This bit is cleared by writing 1	W/R	0x0
2	UVLO pending bit This bit is cleared by writing 1	W/R	0x0
1	OTP(over temperature protect) pending bit This bit is cleared by writing 1	W/R	0x0
0	SCP/OLP(short circuit protect and over load protect) pending bit This bit is cleared by writing 1	W/R	0x0

2.9. REG 0x0C: System Status

Bit	Description	R/W	Default
7	Charger on/off(realtime) 0: charger off 1: charger on	R	0x0
6	Boost on/off(realtime) 0: boost off 1: boost on	R	0x0
5-4	/	/	/
3	Port B status 0: port B off 1: port B on	R	0x0
2	Port C status 0: port C off 1: port C on	R	0x0
1	/	/	/

0	Port A status 0: port A off 1: port A on	R	0x0

2.10. REG 0x0F: Protocol Indication

Bit	Description	R/W	Default
7	PD version 0: PD2.0 1: PD3.0	R	0x0
6-4	sink protocols is valid (SW6224 as sink) 0: no fast charge valid 1: PD sink 2: / 3: HV sink 4: AFC sink 5: FCP sink 6: SCP sink 7: PE1.1 sink	R	0x0
3-0	source protocols is valid(SW6224 as source) 0: no fast charge valid 1: PD source 2: PPS source 3: QC2.0 source 4: QC3.0 source 5: FCP source 6: PE2.0/1.1 source 7: SFCP source 8: AFC source 9: SCP source 11-15: reserved	R	0x0

2.11. REG 0x12: ADC Config

Bit	Description	R/W	Default
7-3	Reserved	/	/
2-0	Adc data type 0: adc_vbat (1.2mv) 1: adc_vout (4mv)	R/W	0x0

	2: adc_dietemp (1/6.82℃) Tdie = (adc_dietemp[11:0]-1839)/6.82; 3: adc_NTC(1.1mv when reg0x48[0]=1, 2.2mv when reg0x48[0]=0) 4: adc_ichg (25/11mA) 5: adc_idischg (25/11mA) Other: reserved Note NTC resistance is computed according to adc_NTC voltage and current. current value reference reg0x48[0].		

2.12. REG 0x13: ADC Data High 8bit

Bit	Description	R/W	Default
7-0	ADC data high 8bit Adc_data[11:04]	R/W	0x0

2.13. REG 0x14: ADC Data Low 4bit

Bit	Description	R/W	Default
7-4	/	/	/
3-0	ADC data low 4bit Adc_data[03:00]	R/W	0x0

2.14. REG 0x18: Scenes Control enable

Bit	Description	R/W	Default
7-5	/	/	/
4	Downstream close operation Close boost and downstream power path gates when writing '1' to this bit and this bit is automatically cleared by hardware. Note: the operation is similar to boost anormal case, leading to scenes change.	R/W	0x0
3-1	/	/	/
0	Charger close operation Close charger when the bit is '1' and release charger when the bit is '0'. Note: only operating charger and don't close upstream power path gate.	R/W	0x0

2.15. REG 0x19: Port Event Generate

Bit	Description	R/W	Default
7-6	/	/	/
5	Port Csrc plug out event(SW6224 as source) Csrc plug out (unloading)when write '1' to this bit and the bit is automaltically cleared by hardware. Note: it is valid only when typec source is attached	R/W	0x0
4	Port Csrc plug in event Csrc plug in (when C connect) when write '1' to this bit and the bit is automatically cleared by hardware	R/W	0x0
3-2	/	/	/
1	Port A plug out event A plug out when write '1' when write '1' to this bit and the bit is automatically cleared by hardware	R/W	0x0
0	Port A plug in event A plug in when write '1' when write '1' to this bit and the bit is automatically cleared by hardware	R/W	0x0

2.16. REG 0x1A: Fast Charge Config0

Bit	Description	R/W	Default
7	C port dm detect enable 0: enable 1: disable	R/W	0x0
6-5	Reserved	R/W	0x0
4	AFC source 12v enable 0: 9v enable 1: 12v enable	R/W	0x0
3	FCP source 12v enable 0:9v 1:12v	R/W	0x1
2	sink request max high voltage (SW6224 as sink) 0: request 12v 1: request 9v	R/W	0x1
1	output max high voltage 0:12v 1:9v Note: this voltage is unvalid for FCP and PD	R/W	0x1
0	reserved	R/W	0x0

2.17. REG 0x1B: Fast Charge Config1

Bit	Description	R/W	Default
7	Port A source fast charge 0: enable 1: disable	R/W	0x0
6	Reserved	R/W	0x0
5	Port C source fast charge 0: enable 1: disable	R/W	0x0
4	Port B sink fast charge 0: enable 1: disable	R/W	0x0
3	Por C sink fast charge 0: enable 1: disable	R/W	0x0
2	Reserved	R/W	0x0
1	Port B HV protocal sink enable 0: enable 1: disable	R/W	0x0
0	Port C HV protocol sink enable 0: enable 1: disable	R/W	0x0

2.18. REG 0x1C: Fast Charge Config2

Bit	Description	R/W	Default
7	Vbus of port A pre-loading detect enable 0: disable 1: enable	R/W	0x1
6	Reserved	R/W	0x0
5	PD source enable 0: enable 1: disable	R/W	0x0
4	PD sink enable 0: enable 1: disable	R/W	0x0
3	PD high voltage close port C unloading detect 0: close port C unloading detect when PD high voltage 1: not close port C unloading detect when PD high voltage	R/W	0x0

2	High volt SCP enable 0: enable 1: disable	R/W	0x1
1	Port A QC source enable 0: enable 1: disable	R/W	0x0
0	FCP source enable 0: enable 1: disable	R/W	0x0

2.19. REG 0x1D: Fast Charge Config3

Bit	Description	R/W	Default
7	FCP sink enable 0: enable 1: disable	R/W	0x0
6	PE source enable 0: enable 1: disable	R/W	0x0
5	PE sink enable 0: enable 1: disable	R/W	0x1
4	AFC source enable 0: enable 1: disable	R/W	0x0
3	AFC sink enable 0: enable 1: disable	R/W	0x0
2	SCP source enable 0: enable 1: disable Note: reg0x1C[2] enable high volt SCP and reg0x2D[2] enable low volt SCP when reg0x1D[2] enable	R/W	0x0
1	SCP sink enable 0: enable 1: disable	R/W	0x0
0	SFCP source enable 0: enable 1: disable	R/W	0x0

2.20. REG 0x1E: Fast Charge Config4

Bit	Description	R/W	Default
7-5	/	R/W	0x0
4	charge prior to discharge 0: charging battery while discharging to downstream port 1: charger prior to downstream plug	R/W	0x0
3-2	Reserved	R/W	0x0
1	Port C QC source enable 0: enable 1: disable	R/W	0x0
0	Reserved	R/W	0x1

2.21. REG 0x1F: Fast Charge Led Status

Bit	Description	R/W	Default
7-5	/	/	/
3	Fast charge led status 0: off 1: on	R	0x0
2-0	Reserved	R	0x0

2.22. REG 0x21: System Anormal Case 1

Bit	Description	R/W	Default
7-6	Reserved	/	/
5	Vdd OVP pending bit Note this bit is cleared by writing ‘1’ to reg0x0B[6]	R	0x0
4-0	Reserved	/	/

2.23. REG 0x20: Wled Config

Bit	Description	R/W	Default
7-5	reserved	R/W	0x0
4	mcu configure wled mode enable 0: disable 1: enable	R/W	0x1
3-1	reserved	R/W	0x0

0	Wled_mode 0: disable 1: enable	R/W	0x1

2.24. REG 0x22: PD Command

Bit	Description	R/W	Default
7-4	/	/	/
3-0	PD command 1: send hardreset command other: reserved	R/W	0x0

2.25. REG 0x28: Typec Config

Bit	Description	R/W	Default
7-4	reserved	R/W	0x2
3-2	Typec role configure 0: strong drp 1: only sink 2: only source 3: reserved	R/W	0x0
1-0	Reserved	R/W	0x1

2.26. REG 0x29: Typec Indication

Bit	Description	R/W	Default
7-4	/	/	/
3-2	reserved	R	0x0
1-0	Typec power role indication 1: sink 2: source 0/3:no attach	R	0x0

2.27. REG 0x2A: PD Config0

Bit	Description	R/W	Default
7	Reserved	R/W	0x0
6	PD verison 0: PD 3.0	R/W	0x0

	1: PD 2.0		
5	PPS1 high voltage 0: 11V 1: 9V	R/W	0x0
4-0	Reserved	R/W	/

2.28. REG 0x2B: PD Config1

Bit	Description	R/W	Default
7-6	Reserved	R/W	0x0
5	PPS0 enable 0: enable 1: disable	R/W	0x1
4	PD 5V/2A PDO enable 0: disable 1: resend 5v/2A PDO after sink request 5v/3A PDO	R/W	0x0
3	PPS1 enable 0: enable 1: disable	R/W	0x1
2-0	Reserved	R/W	0x0

2.29. REG 0x2C: PD Config2

Bit	Description	R/W	Default
7-6	/	/	/
5-4	PD fixed 5V PDO current 0: 3.0A 1: 2.4A 2: 2.5A 3: 2.0A	R/W	0x0
3-2	PD fixed 9V PDO current 0: 2.0A 1: 2.22A 2: 2.33A 3: 2.4A	R/W	0x0
1-0	PD fixed 12V PDO current 0: 1.5A 1: 1.6A 2: 1.67A 3: 1.75A	R/W	0x0

2.30. REG 0x2D: PD Config4

Bit	Description	R/W	Default
7-6	Reserved	/	/
5	PD enable when multi port opened 0: enable 1: disable	R/W	0x1
4-3	Reserved	R/W	0x0
2	Low volt SCP enable 0:disable 1:enable	R/W	0x0
1	Reserved	R/W	0x1
0	Samsung 1.2V mode enable 0: enable 1: disable	R/W	0x0

2.31. REG 0x2E: Trickle Current Charge Control

Bit	Description	R/W	Default
7-6	/	/	/
4	Enter/exit trickle current charge 0: nothing 1: enter/exit trickle current charge This bit is automatically cleared by hardware	R/W	0x0
3-1	/	/	/
0	Trickle current charge status 0: normal charge 1: in trickle current charge	R	0x0

2.32. REG 0x30: Plug Out Config0

Bit	Description	R/W	Default
7-6	unloading detect time when single port open 0: 32s 1: 8s 2: 16s 3: 64s	R/W	0x0
5-4	unloading detect time when multi port open 0: 32s	R/W	0x2

	1: 8s 2: 16s 3: 64s		
3-1	unloading detect current threshold setting VOUT<7.65V or VOUT>7.65V and reg0x30[0]=0: 0: 55mA 1: 10mA 2: 25mA 3: 40mA 4: 70mA 5: 85mA 6: 100mA 7: 115mA VOUT>7.65V and reg0x30[0] =1: 0: 30mA 1: 10mA 2: 5mA 3: 25mA 4: 40mA 5: 40mA 6: 55mA 7: 70mA	R/W	0x0
0	Unloading detect current threshold change when vout > 7.65v 0: not change 1: change	R/W	0x1

2.33. REG 0x31: Plug Out Config1

Bit	Description	R/W	Default
7-6	Reserved	R/W	0x0
5	Port A dm detect enable 0: enable 1: disable	R/W	0x1
4	Cable compensate enable 0: enable 1: disable	R/W	0x0
3	Port A Load detect enable 0: enable 1: disable	R/W	0x0
2-1	Reserved	R/W	0x2
0	close power enable when port C unloading	R/W	0x0

	0: enable 1: disable		

2.34. REG 0x33: Trickle Current Charge Config

Bit	Description	R/W	Default
7-2	/	/	/
1-0	MCU configure trickle current charger mode enable 2: disable 3: enable Other: reserved	R/W	0x0

2.35. REG 0x40: Boost Config0

Bit	Description	R/W	Default
7-5	UVLO threshold 0: 2.8V 1: 2.7V 2: 2.9V 3: 3.0V 4: 3.1V 5: 3.2V 6: 3.3V 7: 3.4V	W/R	0x2
4-3	UVLO hystersis 0: 0.5V 1: 0.4V 2: 0.6V 3: 0.7V	W/R	0x0
2-1	Boost frequency 0: 400K 1: 300K 2: 500K 3: 600K	W/R	0x0
0	Max output power 0: 18W 1: 21W	R/W	0x0

2.36. REG 0x41: Boost Config1

Bit	Description	R/W	Default
7-5	Reserved	W/R	0x0
4-3	Vout offset setting 0: 100mV 1: 0mV 2: 50mV 3: 150mV	W/R	0x3
2	constant current margin 0: 5% 1: 15% For 5V output when reg0x48[2]=1, 0: 1A 2: 2A	R/W	0x0
1	Reserved	W/R	0x0
0	max output current setting when multi output port open 0: 3A 1: 4.2A	W/R	0x0

2.37. REG 0x42: Charger Config0

Bit	Description	R/W	Default
7-5	input current setting when 9v input (port current) 0: 2.0A 1: 1.6A 2: 1.7A 3: 1.8A 4: 1.9A 5: 2.1A 6: 2.2A 7: 2.3A	R/W	0x0
4-2	input current setting when 12v input (port current) 0: 1.5A 1: 1.1A 2: 1.2A 3: 1.3A 4: 1.4A 5: 1.6A 6: 1.7A 7: 1.8A	R/W	0x0

1-0	reserverd	R/W	0x0

2.38. REG 0x43: Charger Config1

Bit	Description	R/W	Default
7-4	Port C input current setting when 5v input 0: 2.0A 1: 1.8A 2: 1.9A 3: 1.7A 4: 2.1A 5: 2.2A 6: 2.3A 7: 2.4A 8: 2.5A 9: 2.6A A: 2.7A B: 2.8A C: 2.9A D: 3.0A E: 3.1A F: 3.2A	R/W	0xd
3-1	Port B input current setting when 5v input 0: 2.0A 1: 1.8A 2: 1.9A 3: 1.7A 4: 2.1A 5: 2.2A 6: 2.3A 7: 2.4A	R/W	0x0
0	/	/	/

2.39. REG 0x44: Charger Config2

Bit	Description	R/W	Default
7	/	/	/
6	charger end current threshold 0: 5v/230mA,9v/130mA,12v/100mA	R/W	0x0

	1: 5v/270mA, 9v/150mA,12v/110mA		
5-3	charger 5V input voltage threshold 0: 4.6V 1: 4.7V 2: 4.8V 3: 4.9V 4: 4.2V 5: 4.3V 6: 4.4V 7: 4.5V	R/W	0x7
2-0	charger temperature loop set 0: 100℃ 1: 105℃ 2: 110℃ 3: 115℃ 4: 80℃ 5: 85℃ 6: 90℃ 7: 95℃	R/W	0x3

2.40. REG 0x45: Charger Config3

Bit	Description	R/W	Default
7-6	/	/	/
5-3	12V input voltage threshold 4: 11.215V 5: 11.215V 6: 11.321V 7: 11.429V 0: 11.538V 1: 11.650V 2: 11.765V 3: 11.881V	R/W	0x7
2-0	9V input voltage threshold 4: 8.072V 5: 8.182V 6: 8.295V 7: 8.392V 0: 8.490V 1: 8.612V 2: 8.738V	R/W	0x0

	3: 8.867V		

2.41. REG 0x46: Charger Config5

Bit	Description	R/W	Default
7-6	Charger frequency 0: 600K 1: 400K 2: 800K 3: 500K	R/W	0x1
5-0	reserved	R/W	0x0

2.42. REG 0x47: NTC Config0

Bit	Description	R/W	Default
7-6	NTC low temperature threshold for boost 0: -20℃ 1: 5℃ 2: 5℃ 3: 5℃	R/W	0x0
5-4	NTC high temperature threshold for boost 0: 60℃ 1: 50℃ 2: 55℃ 3: 65℃	R/W	0x0
3	boost NTC protect function enable 0: enable 1: disable Note: if protect function enable, boost will close when NTC temperatue is out of threshold range.	R/W	0x0
2	boost NTC temperature adaptive enable 0: enable 1: disable Note: if adaptive enable, vout will drop 800mv/degree when NTC temperature high than adaptation threshold.	R/W	0x1
1-0	/	/	/

2.43. REG 0x48: NTC Config1

Bit	Description	R/W	Default
7	charger JEITA rule enable 0: disable 1: enable	R/W	0x1
6-5	NTC high temperature threshold for charger 0: 50℃ 1: 45℃ 2: 55℃ 3: 60℃	R/W	0x0
4-3	NTC low temperature threshold for charger 0: 0℃ 1: 15℃ 2: 15℃ 3: 15℃	R/W	0x0
2	5V output current limit set 0: 3A 1: 1A/2A	R/W	0x0
1	boost NTC temperature adaptive hysteresis 0: 5℃ 1: 10℃	R/W	0x0
0	NTC current flag 0: 80uA 1: 40uA	R	0x0

2.44. REG 0x49: Temperature Config

Bit	Description	R/W	Default
7	/	/	/
6-4	over temperature threshold for boost and charger 0: 130℃ 1: 100℃ 2: 110℃ 3: 120℃ 4: 90℃ 5: 140℃ 6: 150℃ 7: 160℃	R/W	0x6
3	boost temperature adaptive enable 0: enable 1: disable	W/R	0x0

2-0	boost adaptive temperature setting 0: 100℃ 1: 105℃ 2: 110℃ 3: 115℃ 4: 80℃ 5: 85℃ 6: 90℃ 7: 95℃	R/W	0x3

2.45. REG 0x57: Version Info

Bit	Description	R/W	Default
7-3	/	/	/
2-0	IC version	R	0x6

2.46. REG 0x73: Max Power Capacity Low 8bit

Bit	Description	R/W	Default
7-0	Battery max capacity Bat_cap[7:0] 0.1695V.A.H/bit. For typical 3.7V 10000mAH battery, the max capacity is 3.7V * 10A.H = 37V.A.H	R/W	-

2.47. REG 0x74: Max Power Capacity High 4bit

Bit	Description	R/W	Default
7-4	/	/	/
3-0	Battery max capacity Bat_cap[11:08]	R/W	-

2.48. REG 0x7A: Charge Control

Bit	Description	R/W	Default
7-6	Reserved	R/W	0x0
5	Charge battery voltage set 0: normal 1: reduce bat voltage 0.1V	R/W	0x0
4	Charge current set 0: normal current	R/W	0x0

	1: set by reg0x7A[3]		
3	Charge current 0: 5V/9V12V 0.5A 1: 5V/9V12V 1A	R/W	0x0
2-0	Reserved	R/W	0x0

2.49. REG 0x7E: Final Process Percent

Bit	Description	R/W	Default
7	/	/	/
6-0	Final process percent 1%/step	R	0x0