CL400/CLG400 Packages—XC7Z014S, XC7Z020, XA7Z020, and XQ7Z020

User I/O Pins	Dedicated Pins	Other Pins	PS MIO Pins	PS DDR Pins
○ IO_LXXY_#	CFGBVS_0	GND	◉ PS_POR_B	PS_DDR_CKP
Ⓢ IO_XX_#	D DONE_0	VCCAUX_IO_G#	PS_CLK	PS_DDR_CKN
	J DXP_0	VCCAUX	◎ PS_SRST_B	Ⓔ PS_DDR_CKE
Multi−Function Pins	L DXN_0	VCCINT	⊗ PS_MIO_VREF	Ⓢ PS_DDR_CS_B
	GNDADC_0	VCCO_#	PS_MIO	Ⓡ PS_DDR_RAS_B
B PUDC_B	Y INIT_B_0	VCCBRAM		Ⓒ PS_DDR_CAS_B
● AD0P/AD0N–AD15P/AD15N	P PROGRAM_B_0	VCCPINT		Ⓦ PS_DDR_WE_B
⊕ VRN	K TCK_0	VCCPAUX		Ⓐ PS_DDR_BA
⊖ VRP	I TDI_0	VCCO_MIO0		PS_DDR_A
⊗ VREF	O TDO_0	VCCO_MIO1		Ⓣ PS_DDR_ODT
◐ DQS	M TMS_0	VCCO_DDR		Ⓓ PS_DDR_DRST_B
◕ MRCC	VCCADC_0	◆ VCCPLL		PS_DDR_DQ
◔ SRCC	VCCBATT_0	R RSVDVCC[3:1]		Ⓜ PS_DDR_DM
	S VP_0	R RSVDGND		PS_DDR_DQS_P
	S VN_0	n NC		PS_DDR_DQS_N
	S VREFP_0			⊖ PS_DDR_VRP
	S VREFN_0			⊕ PS_DDR_VRN
				PS_DDR_VREF

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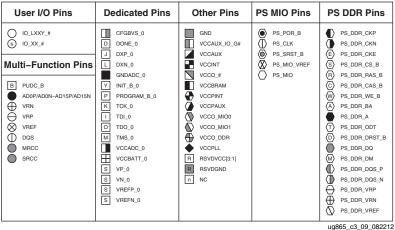*Figure 3-13:* **CL400/CLG400 Packages—XC7Z014S, XC7Z020, XA7Z020, and XQ7Z020 Pinout Diagram**