hypothermic / **lane-detection** Private

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master

Commits on Apr 1, 2022

Fix wrong register map being used in vpu driver **hypothermic** committed on Apr 1 ✓	Verified		07603cf
Remove generated output from Jupyter notebooks **hypothermic** committed on Apr 1 ✓	Verified		8837d45
Write driver code to interface with VPU core **hypothermic** committed on Apr 1 ✓	Verified		41c731d
Implement median blur filter in IP core **hypothermic** committed on Apr 1 ✓	Verified		f47145d
Add HLS test targets in makefile **hypothermic** committed on Apr 1 ✓	Verified		6ea8a2f

Commits on Mar 31, 2022

Add makefile rules for running HLS and HW builds **hypothermic** committed on Mar 31 ✓	Verified		f9dc917
Add commandline tools for synth & impl to bitstream **hypothermic** committed on Mar 31	Verified		1372587

Commits on Mar 30, 2022

Write resource utilization reports in technical design
hypothermic committed on Mar 30
Verified `d9db253`

Commits on Mar 29, 2022

Add place&route figures to technical design
hypothermic committed on Mar 29
Verified `654e2c9`

Add package and address mapping diagrams
hypothermic committed on Mar 29
Verified `62d118b`

Write paragraph Implementation Strategy
hypothermic committed on Mar 29
Verified `cd7d0e9`

Commits on Mar 28, 2022

Add enlarged version of block diagram as appendix entry
hypothermic committed on Mar 28
Verified `97d871f`

Update design document with a beautiful figure of the block design
hypothermic committed on Mar 28
Verified `080129e`

Add s_axilite interface to VPU to control it via DMA
hypothermic committed on Mar 28
Verified `bd06d79`

Fix IP core output location
hypothermic committed on Mar 28
Verified `bf07f4f`

HLS IP Core export works
hypothermic committed on Mar 28
Verified `6fdeef2`

Commits on Mar 25, 2022

Update timetable
 **hypothermic** committed on Mar 25 ✓
Verified `ee92f68`

Keep latex preamble and title/lastpage in separate files
 **hypothermic** committed on Mar 25 ✓
Verified `f68256d`

Fix workflow issue TD figure not found
 **hypothermic** committed on Mar 25 ✓
Verified `1bc0fe3`

Commits on Mar 24, 2022

Add problem domain in TD
 **hypothermic** committed on Mar 24 ✗
Verified `ff47398`

Fix design pdfs not being generated for document workflow
 **hypothermic** committed on Mar 24 ✓
Verified `994c7a6`

Commits on Mar 23, 2022

Update technical design
 **hypothermic** committed on Mar 23 ✓
Verified `1bb5ab2`

Commits on Mar 21, 2022

Update technical design
 **hypothermic** committed on Mar 21
Verified `15ec41a`

Write about PYNQ-Z2 memory options
 **hypothermic** committed on Mar 21 ✓
Verified `755273f`

Commits on Mar 18, 2022

Update timetable
 **hypothermic** committed on Mar 18 ✓
Verified `81bf6be`

Commits on Mar 17, 2022

Update timetable
 **hypothermic** committed on Mar 17 ✓
Verified `2715965`

Describe memory implementation in technical design
 **hypothermic** committed on Mar 17
Verified `222c5c1`

Fix vector graphics being ignored on git
 **hypothermic** committed on Mar 17 ✓
Verified `a0550ab`

Add dependency on tikz-uml for drawing UML diagrams
 **hypothermic** committed on Mar 17 ✗
Verified `e71ce3b`

Fix gitattributes not indexing tex files
 **hypothermic** committed on Mar 17
Verified `a2bef51`

Add functional and technical designs to pdf output
 **hypothermic** committed on Mar 17 ✗
Verified `7427b7a`

Commits on Mar 16, 2022

Update timetable
 **hypothermic** committed on Mar 16 ✓
Verified `a20ba55`

Start technical design
 **hypothermic** committed on Mar 16
Verified `ce57b39`

Use case diagram

 **hypothermic** committed on Mar 16

Verified `217b46a`

Update a7 device constraints for ov7670 and vga output

 **hypothermic** committed on Mar 16

Verified `1bd0dd8`

Newer Older