Olin College ENGR3410: Computer Architecture Fall 2022

Name:

Collaborators:

Homework 4

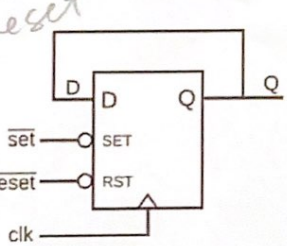
1. Reading and Review

- *Continue referring back to Ch3, Ch4, and the Verilog Cheatsheet as needed*
- Reread Ch1, 1.4.5, 1.4.6
- Chapter 5: 5.1 to 5.2.3
    - Section on Cary-Lookahead/Prefix Adders is optional

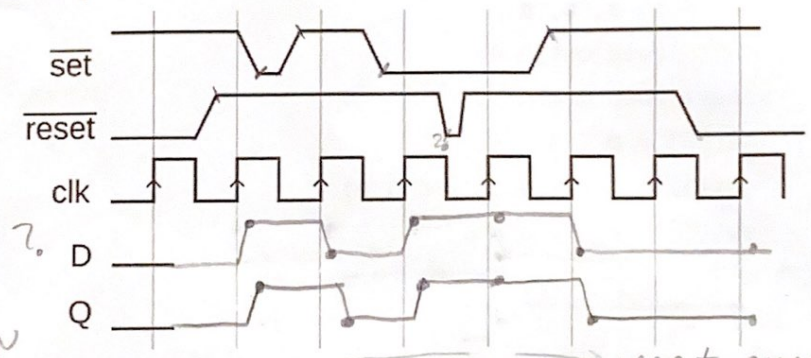
These questions are to make sure you get enough from the reading. Show your work!

a) Review: Flip Flops

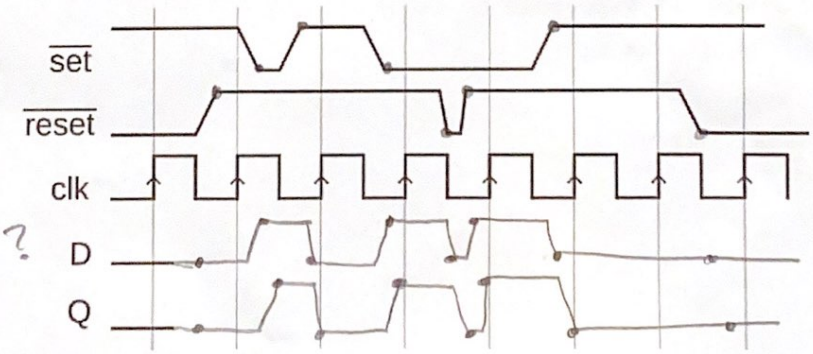
Sketch the waveforms for the following circuit under different types of set/reset. Note that for this flip flop set and reset are active low (action occurs when the voltage is zero).



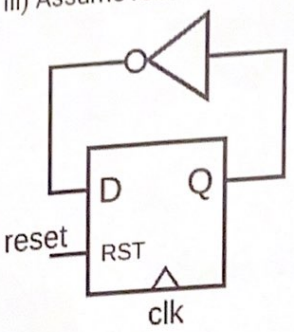
i) assume synchronous set/reset

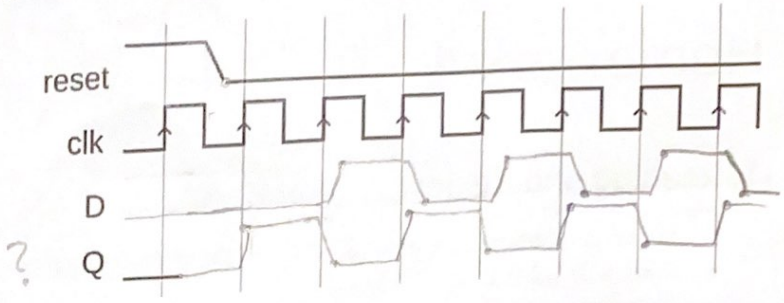


ii) assume asynchronous set/reset



iii) Assume reset is active high **and** synchronous. Sketch the waveforms for D and Q below.





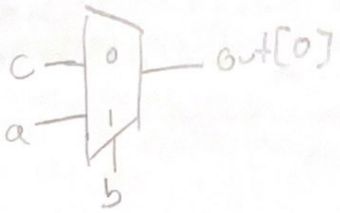
2. Verilog Skillbuilding

a) Verilog to Schematic

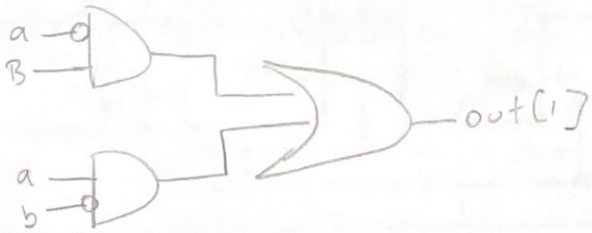
For each output, draw an equivalent gate level schematic ***and*** write a phrase or sentence describing what that output does in terms of the inputs.

```
module mystery(a,b,c, out);
 input wire a, b, c;
 output logic out[3:0];
  always_comb begin
   out[0] = b ? a : c;
   out[1] = (~a & b) | (~b & a);
   out[2] = c | ( b & c);
 end
 logic d;
 always_comb d = b ? a : 1'b0;
 always_ff @(posedge c) begin
   out[3] <= d;
 end
endmodule
```

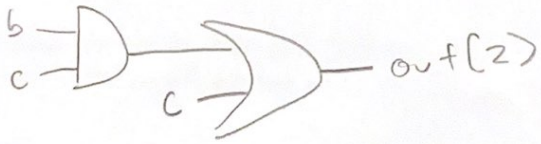
out[0]:



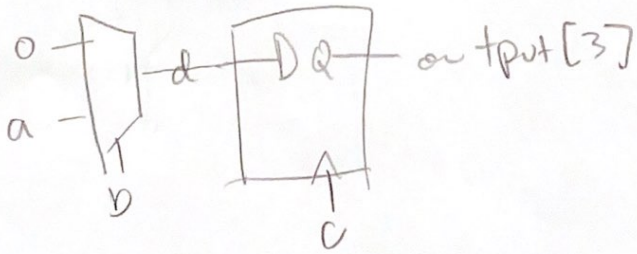
out[1]:



out[2]:



out[3]:



b) Schematic to Verilog

Create this module as part of your zipped submission. There's a testbench to go with it so you can see what it does (it's not an obviously useful circuit but it has some interesting use cases).