



# Final Year Project Title: Wireless Clock Generator for Magnetic Tracking Synchronization

Discipline of Electrical and Electronic Engineering  
Module EE4050 - Project  
Final Report



AUTHOR: DECLAN O SULLIVAN, 119341691  
SUPERVISOR: ALEX JAEGER  
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## List of Abbreviations

PCB	Printed Circuit Board
Op-amp	Operational Amplifier
TX	Transmission
RX	Reception
ISM	Industrial Scientific and Medical
RF	Radio Frequency
V	Volts
VSWR	Voltage Standing Wave Ratio
VNA	Vector Network Analyser
EMT	Electromagnetic Tracking

## List of Scientific Symbols

$\mu$	$10^{-6}$
M	$10^6$
k	$10^3$

## Abstract

This project aimed to provide a wireless clock design, suitable for implementation in an Electromagnetic Tracking (EMT) sensor node. The wireless clock's purpose is to alleviate the mobility constraints associated with a wired design, whilst maintaining synchronous clock function. Previous research has successfully implemented a theoretical wireless design. This project is distinguished by the target of creating a low power and cost optimised implementation. Simulations were conducted in the Simulink and LTspice environments, before a hardware construction was formed. Successful operation of a wireless clock was achieved, proving the efficacy of the theoretical motivation and the performance of the design.

## 1. Summary

The fundamental construct motivating the pursuit of the project resided in the increased performance delivered from wireless clock systems, as opposed to wired constructs. Wired clocks are subject to potential time delays, in a manner proportional to the length of the signal carrying wire. This feature delivers inconsistencies when operating a number of devices from the same clock. Through the mechanism of a wireless clock, however, the system clock accuracy can be ameliorated. This is achieved through the use of radio waves, signal processing and antennas.

In order to maximise design efficacy, the project was apportioned into four distinct sections. The first section was Simulink simulation and design. The Simulink environment facilitated a broad scale design approach, where signal processing filter constructions could be implemented and tested, without the presence of individual electrical components. The second stage involved a more practical implementation of the design, with the knowledge and results obtained from the previous Simulink design, informing the composition of a real component design. This was undertaken in the LTspice environment. The operating points and efficiency models of both designs were then combined, to enlighten the final stages of practical design.

The final stages of design involved the accumulation of the completed designs into a practical hardware implementation. The printed circuit board (PCB) design software Altium permitted the composition of the schematic, 2D and 3D layout formats of the PCB. The ambition of this hardware was to offer the proposed function, in a manner optimised under the conditions of both efficiency and efficacy.

## 2. Relevant Theory

The fundamental construct upon which this project is constructed, resides in the form that when two single frequency tones are transmitted, the resultant wave can be represented by the product of two cosine functions. Contained within each cosine function is both a sum and difference frequency term. This project aims to extract the difference frequency term.

Let  $x_1(t) = Ae^{j2\pi f_1 t}$  and  $x_2(t) = Ae^{j2\pi f_2 t}$  be two single tone sinusoidal signals of amplitude  $A$  at frequencies  $f_1$  and  $f_2$ , respectively. The transmitted two-tone signal is represented by Equation 1.

$$S_{tx}(t) = A \sum_{k=1}^2 A e^{j2\pi f_k t} \quad (1)$$

This superposition of waves can be written as a function of the sum and difference of the frequencies  $f_1$  and  $f_2$  [1], as demonstrated in Equation 2.

$$S_{tx}(t) = 2\cos(2\pi((\frac{f_1-f_2}{2})t)) e^{j2\pi(\frac{f_1+f_2}{2})t} \quad (2)$$

One part is a quadrature signal which oscillates with the average frequency  $f_{avg} = f_1 + f_2$ . The other part is a cosine wave which oscillates with the difference frequency  $f = f_1 - f_2$ , as if it were the modulator signal controlling the envelope of the resulting wave.

The envelope signal crosses the zero mark twice in every period and, thus, the envelope frequency is twice the difference frequency. This envelope signal is represented by the magnitude of the difference of the two frequencies,  $f_{env} = |f_1 - f_2|$ . The central goal of this project is to extract this difference frequency signal. The reference clock signal  $f_{clk}$ , or  $f_{env} = |f_1 - f_2|$ , is extracted through a suitably designed envelope detector.

## 3. Electromagnetic Tracking (EMT)

The motivation behind the construction of a wireless synchronised clock resides in its application to Electromagnetic Tracking (EMT). EMT harnesses the utility of a sensor, in conjunction with a transmitting magnetic field generator, to facilitate the real time tracking of the position and orientation of the sensor, within the patient. This is demonstrated in Figure 1. Examples of the employment of this technology include orthopaedics [2] and neurosurgery [3].

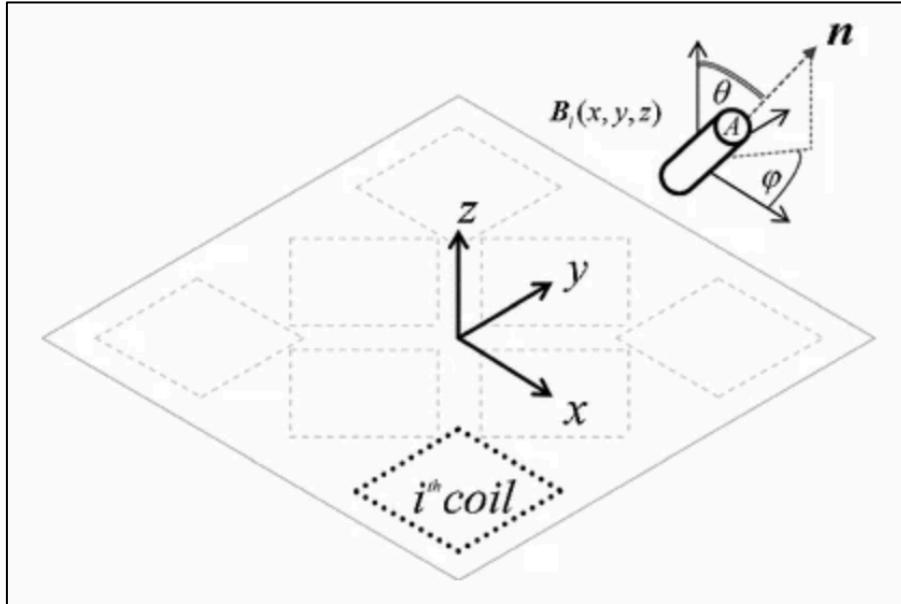


Figure 1: EMT generator and sensor conjunctive use to determine position and orientation data [4].

Electromagnetic tracking is the gold standard for instrument tracking and navigation in the clinical setting without line of sight. It can alleviate or eliminate the need for real-time radiological imaging, replacing X-ray or fluoroscopy with virtual imaging, registered to prior CT or X-ray patient images. EMT inductive magnetic sensors operate by Faraday's law, given in Equation 3.

$$V = - \frac{\partial \Phi}{\partial t} \quad (3)$$

The magnetic flux  $\Phi$  is calculated as the surface integral of the magnetic flux density  $B$  over the cross-sectional coil area  $A_c$ , demonstrated in Equation 4.

$$\Phi = B \bullet n A_c \quad (4)$$

$B$  can be approximated as constant across the loop for small-diameter coils, as employed in this project.

## 4. Introduction

The key theoretical motivation behind the undertaking resided in the format of the addition of two different frequency signals, each with a unique frequency  $f_1$  and  $f_2$  respectively. The addition of these signals results in a signal envelope with a frequency equal to the difference of the two input signals ( $f_2 - f_1$ ). Under this premise, the two signal frequency values were selected as 900 MHz and 901 MHz

respectively, resulting in a signal envelope of 1 MHz. This would provide the desired clock reference signal.

Upon transmission of the desired signal additions, the basic frequency content fundamental for clock function was established. Relevant signal processing and filtering was then required to remove the desired envelope signal and obtain the clock reference. The first iteration of this design process resided in the construction of an envelope detector circuit, necessary for the extraction of the envelope signal. In conjunction with this, subsequent low pass filter and DC blocking capacitor stages were required, in order to remove the noise present in the obtained envelope signal.

The outlined process facilitated the procurement of a signal with the required clock frequency. The presence of a Schmitt Trigger was then implemented in order to convert the sine wave into the square wave clock signal. The overall block diagram is shown in Figure 2. These series of signal processing steps culminated in the acquisition of the desired 1 MHz clock reference signal.

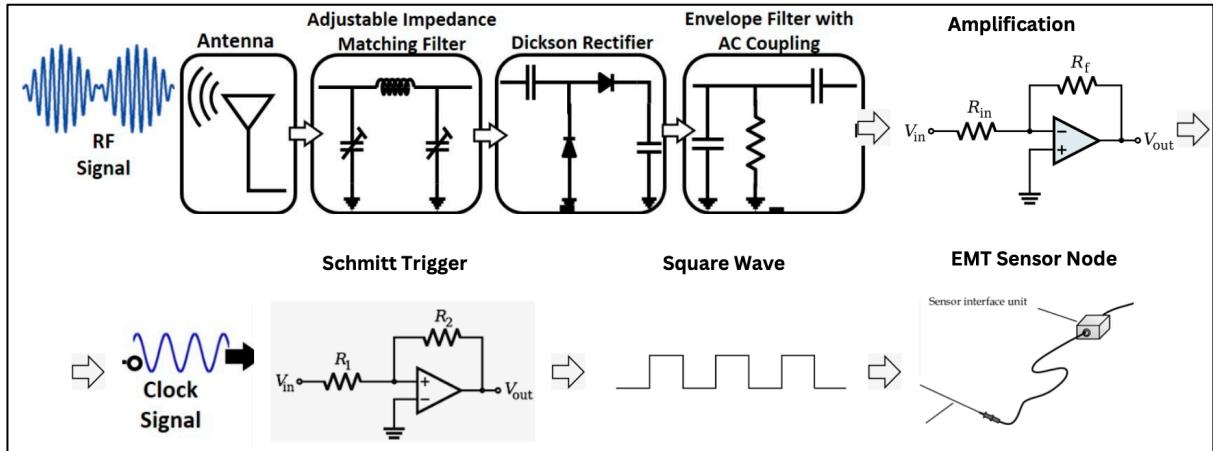


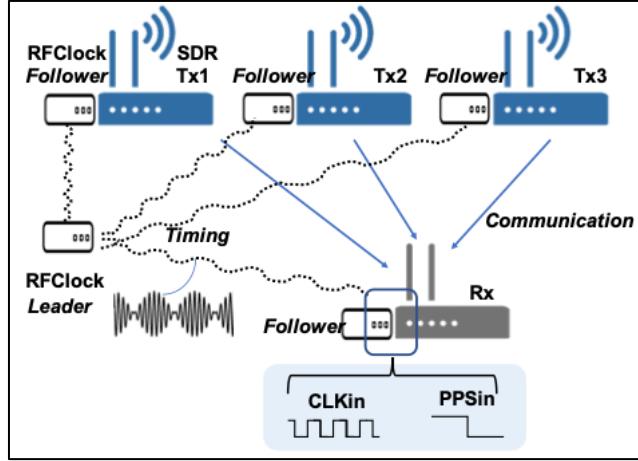
Figure 2: Project block diagram overview [1].

## 5. Literature Review

### (i) RF Clock

Innovation within the context of wireless networks has recently flourished, with the shift from system wide central control towards individual device orientated local decisions, as informed by the broader scale objective. This is demonstrated in Figure 3. An example of this exists in the form of the hundreds of thousands of small base cells composing the 5G network technology [5]. These small cells notate pivotal inclusion in 5G networks, as a consequence of the inclusion of higher frequency spectrum bands, that necessitate network densification in support of increased traffic volumes. The

deployment of small cells targets capacity enhancements, in addition to coverage amelioration, replacing coverage blackspots or inadequacies. Another example of network densification resides in the leveraging of low cost antennas, facilitating the creation of smart surfaces [6], [7].



*Figure 3: RF Clock distributed wireless network architecture [1].*

The innovation supplied by these applications, however, is offset by the requirement for wired connection to a centralised clock. The catalyst to the design of this project resided in the construction of both the transmission and reception design aspects, facilitating the creation of a wireless 1 MHz clock signal. Thus, the design and simulation of an RF clock, providing both a multi-node coherent phase and time reference, was fabricated.

## (ii) Wireless Clock Advantages

The advantages associated with wireless distributed transmission have been explored through a variety of mechanisms [8]. With the emergence of networked devices and wireless applications, the specification of air transmitted time synchronization has become a necessity. The use of independent clocks at different nodes of a system creates an overarching incoherence, triggered by the deviations in nominal frequency at each node of transmission.

Proposed solutions that facilitate a single clock reference typically use two-tone frequency transmission, where the desired clock reference signal is the difference of the two frequencies [9]. The two tones are then amplified through the mechanism of a power amplifier, with a reception chain involving a low noise amplifier and a band pass filter serving to extract the envelope of difference clock frequency. The merit of such an implementation resides in the form of the simplicity and low-cost nature of the design. The absence of any analogue to digital converters or baseband processing, provides further convenience. This utility of outlet removes deviations in the separate node operation supplied by independent clocks, through consistent performance.

### (iii) Alternative Clock Solutions

#### Wired Clock

The most simplistic implementation of a clock is constructed by connecting each system node to a shared clock, through the means of wires. The Ettus Octoclock [10] operates a wired connection between the reference source. The phase and frequency offsets present in the received clock signal are negated by the cable inputs sharing the same lengths and conductive properties. Although this format typically offers coherent time transmission at each node, its performance and practicality regresses, when operated in conjunction with mobile nodes. Under this premise, a solution that offers mobility in conjunction with synchronous clock operation, is achieved through wireless implementation.

#### GPS Clock

A wireless solution exists in the form of connecting each node in a system to a GPS clock, with each clock displaying a very low carrier frequency in comparison to each other, as enforced by the use of GPS signal and temperature-moderated crystals. GPS- disciplined oscillators [11] (GPSDO) are highly stable oscillators. Despite the high precision offered by GPS clock synchronization [12], there is an exorbitant fixed cost, hundreds of thousands of euros, associated with the implementation of such technology. In conjunction with this, GPS clock synchronization stipulates a large power demand and doesn't operate effectively in an indoor setting. This is as a consequence of the requirement for line-of-sight to satellites. Under these outlined premises, this technology is not suitable for deployment, within the context of sensor nodes.

#### (iv) Synchronised Clock

Anser EMT [4] is an open-source EMT platform for image-guided interventions, that uses the AD9833 integrated circuit (*Analog Devices, Norwood, USA*) to generate reference sinusoidal waveforms. A consequent magnetic field is produced by a set of eight planar emitter coils, each supplied by the AD9833 waveform generator chip. Each of these eight emitter coils are supplied by the same clock signal, connected through wires.

The function of this project was to construct an efficacious implementation of a wireless synchronous clock, that would remove the requirement for wiring between all eight nodes. This is achieved through the creation of a distributed generator that transmits a coherent clock signal. This solution fundamentally increases the mobility of the system, through the removal of previously existing wires.

Conducive to this objective, an inexpensive and low-power design implementation was fabricated, creating distributed coherent transmission.

## 6. Ethical Issues

Within the context of RF transmission, there are legal and, therefore, ethical implications. The key advantage of using high frequency transmission signals resides in the consequent increase in information transfer bandwidth. As such, radio frequency transmission is extremely common and heavily regulated. A large percentage of radio frequency bands are licensed and moderated by power limitations. These bands cannot be operated within [13].

The ISM radio frequency bands, however, are specific ranges of the radio spectrum internationally reserved for scientific and industrial use, in radio frequency applications. Under this premise, the transmitted signals used within this project will be maintained within the ISM radio bands. The 900 MHz band falls within the ISM bands and is, thus, free to use in this project. The 900 MHz and 901 MHz ISM bands were used to create a reference 1 MHz clock signal. These frequencies are used as the required 1 MHz clock signal resides within the licenced frequency bands. The use of these ISM band frequencies are subject to the power levels not exceeding threshold values [14]. In recent years, there has been much deliberation as to the validity and value levels of these imposed thresholds but, in the context of this project, the transmitted power is negligible in comparison to the legal limits.

## 7. Description of Main Tasks

The first stage of the design process involved high level MATLAB and Simulink simulation of the signal chain.

### (i) Simulink

#### Noise

Two sinusoidal signal generators, at 900 MHz and 901 MHz respectively, were added to simulate the transmitted signal, from which the clock reference signal was to be extracted. The addition of noise was necessary, in order to replicate the travel of the signals through air and the consequent interfering disturbances. This was initially achieved through the introduction of a random generator block.

Testing and simulation, however, emphasized that a more appropriate mechanism for noise addition existed in the form of the Band-Limited White Noise Simulink block.

The Limited White Noise block contained two central parameters, namely the noise power and the sample time. Initial adjustments to the noise power parameter yielded unsatisfactory results, with the observed output merely producing a dc shift relative to the increase in the inputted noise power value, when added to the sinusoidal summing signal generator. Closer inspection, as informed by conducted research, revealed that the noise power parameter was not a pure value of the noise in Watts, but instead a power spectral density.

The power spectral density of a signal describes the power present in the noise per unit frequency. Under this premise, it was established that the noise power and sample time parameters were not mutually exclusive but, instead, dependent. Through this outlet, the default sample time of 0.1s was modified to a value of  $1\mu\text{s}$ , with time equal to the inverse of frequency and the clock reference having a value of 1 MHz. With this modification in sample time and conjunctive power manipulation, the observed noise obtained the desired format.

## Signal Processing

With the noise format determined, it was established that the appropriate filter for implementation existed in the form of a Chebyshev Low Pass Filter. The purpose of the filter was to create an envelope detection mechanism that would facilitate the capture of the 1 MHz clock reference signal. In order to achieve this, the addition of a magnitude block before the filter processing, was necessary.

The prerequisite of the creation of an appropriate clock reference signal compelled the addition of a Schmitt Trigger device, that would facilitate the construction of a square wave signal. This square wave signal was to retain a frequency value equal to that of the filtered sinusoidal input signal, at 1 MHz. This effect was achieved through the addition of a relay block.

## Operating Conditions

The operational specifications of the system were subsequently investigated. In order to achieve this task, the Signal-to-Noise Ratio (SNR) was calculated. The first step existed in the form of creating Fast Fourier Transforms (FFTs) of the signal, composed of the addition of the input sinusoids with and without noise. To achieve this, an identical signal processing system was composed for the signal but this time without the addition of the band-limited white noise. The purpose of this was to establish a method of comparison between the FFTs taken at each process stage, with and without noise.

Conducive to successfully creating an FFT of a signal in the continuous time domain, the signal must be digitally sampled to ascertain the appropriate format for entry into the FFT block. To achieve this digital sampling, a Zero-Order Hold (ZOH) block was implemented. Upon simulation of the ZOH, with the sample time parameter set at the default -1 inherited value, it became evident that the frequency of the input signals (900 MHz and 901 MHz) were too large. Conducive to the ZOH accurately reflecting the input signals, a sufficiently small sample time was evaluated, with the period being the inverse of frequency.

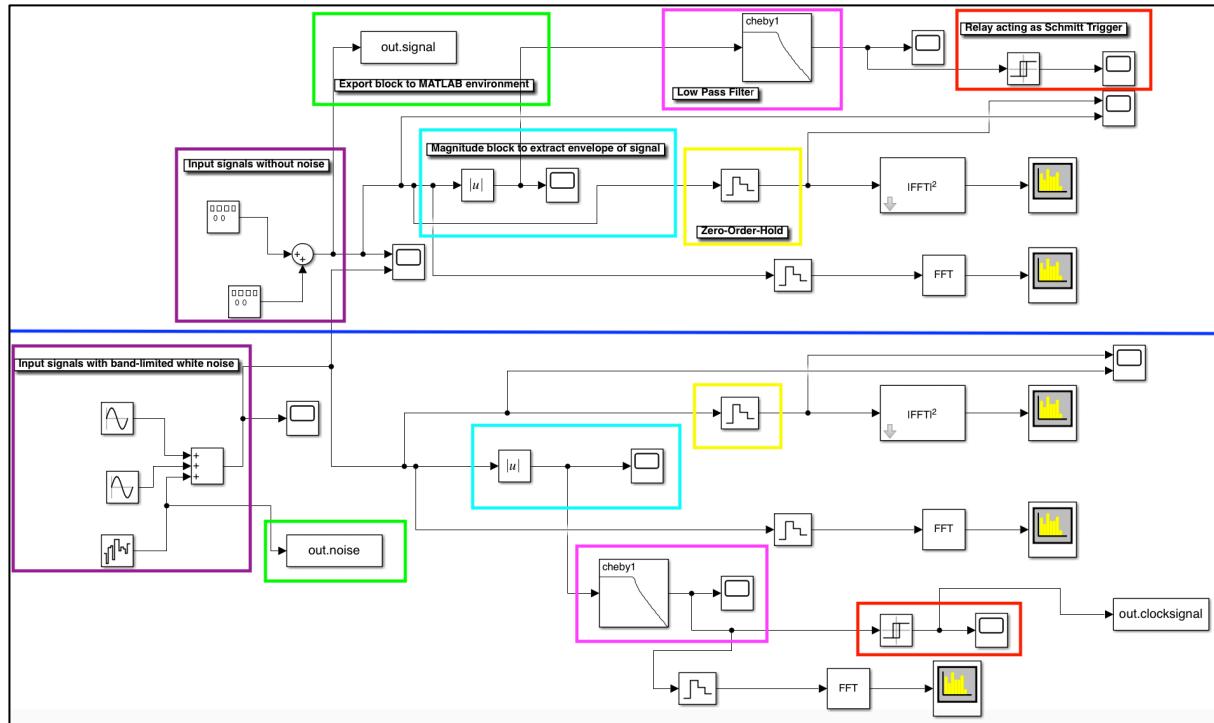


Figure 4: The final Simulink design.

The final Simulink design is visible in Figure 4. The purple boxes represent the input frequency tones, the green represent the MATLAB exports facilitating SNR calculations and the turquoise signifies the magnitude block necessary for envelope extraction. The pink and red boxes indicate the Low Pass filter and the relay acting as the Schmitt Trigger, respectively. The yellow box contains the ZOH necessary for FFT capture. As evident from examination, the design is almost completely symmetrical about the horizontal axis, centred about the middle of the construction. This feature is present as an ideal model of the design was simultaneously executed (top-half of design), containing no added noise, in concurrence with the non-ideal model (bottom half of design).

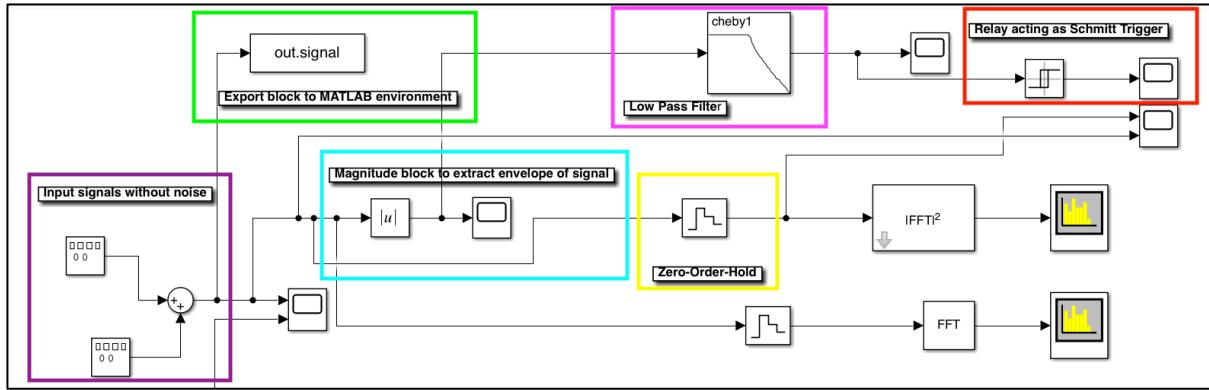


Figure 5: Simulink schematic without noise

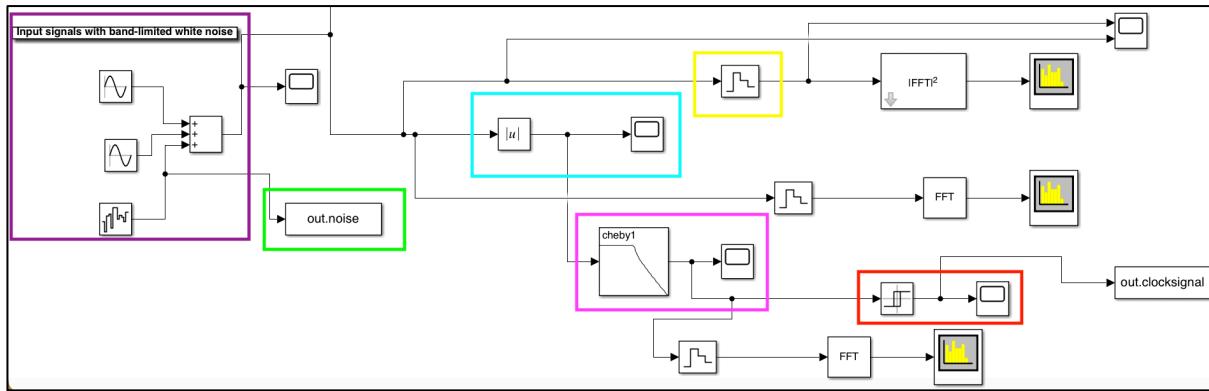


Figure 6: Simulink schematic with noise.

The Simulink schematics without noise and with noise added are demonstrated in Figure 5 and Figure 6 respectively. This implementation was conducted to provide a means of reference of the system, with respect to both noise presence and power. Under this fundamental pillar of construction, the system performance and efficacy can be examined in an objective and unequivocal manner.

## (ii) LTspice

The next step in the simulation and design of the wireless clock generator was to construct a simulation in the LTspice environment. The purpose of this would be to create a simulation with real components and circuit elements, informed by the fundamental construction provided by the broader scale Simulink design. The first step was composed of the construction of two voltage sources in series that produced 900 MHz and 901 MHz sine waves respectively.

### Difference Frequency Extraction

An envelope detector circuit was subsequently composed, consisting of a diode, capacitor and resistor. The capacitor collects and stores charge on the rising edge, slowly discharging through the resistor during the falling edge. The diode acts as a rectifier, only permitting current flow when the

voltage at the positive input terminal is higher in value than the negative input terminal. This envelope detector circuit extracted the resultant 1 MHz desired clock frequency wave, from the output of the combined voltage sources. In order to remove the presence of higher frequencies and improve the clarity of the signal, a low pass filter was then added. The lowpass filter cut-off frequency was calculated as shown in Equation 5.

$$f_c = \frac{1}{2\pi RC} \quad (5)$$

## Signal Processing

It was observed that the output of the low pass filter resulted in a waveform with the desired frequency, but with a DC offset. In order to remove the DC offset present, a DC blocking capacitor was added to the schematic. The resultant output was a sine wave of the desired 1 MHz frequency, with an average value of 0V.

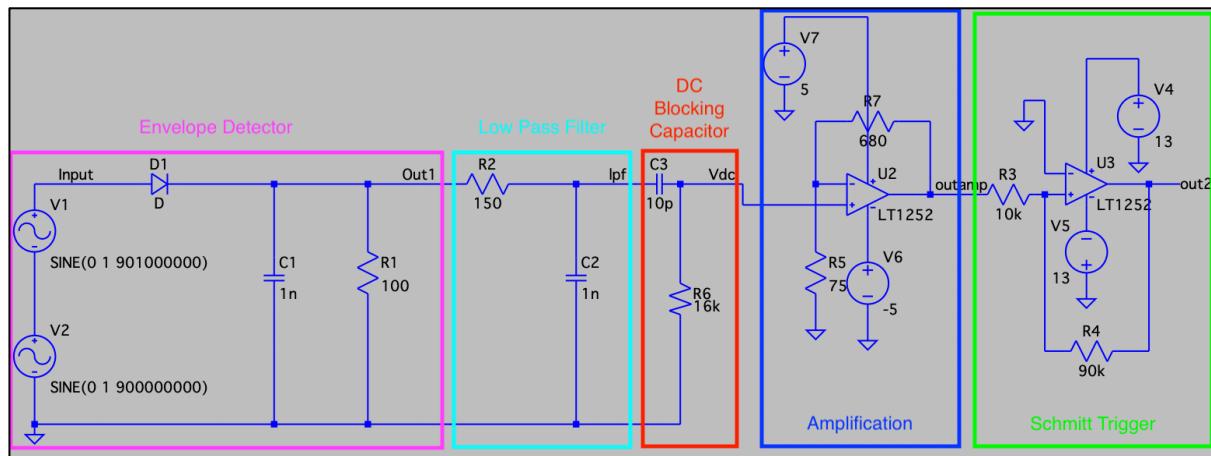


Figure 7: LTspice schematic of final design.

To convert the output signal to a suitable square wave clock signal, the implementation of a Schmitt Trigger was required. Through iterative investigation, it became clear that an additional amplification stage was required before the Schmitt Trigger. This amplification stage was achieved through the implementation of an operational amplifier (op-amp). Integration of the op-amp into the design revealed the importance of using an op-amp with a wide enough frequency bandwidth, to support the amplification of the input signal. The final design is visible in Figure 7.

### (iii) ADALM Pluto Kit

Future progression within the project was moulded by the pursuit of the distillation of the design properties, tested and simulated in both the Simulink and LTspice environments, into a functional

system of hardware. This pursuit was facilitated through the use of the ADALM Pluto kit, which offers an extensive range of features to be utilised on both the transmission and reception sides of antenna technology. The kit interfaced with a desktop application that was used to transmit and receive radio waves, with varying noise powers. These features were utilised to transmit the required 900 MHz and 901 MHz signals at different SNR values. The Pluto kit also has a Simulink package that was used to interface with the hardware in order to export data to MATLAB, facilitating operating point conditions and efficiency of function calculations.

The ADALM Pluto kit was used to generate the required 900 MHz and 901 MHz frequency signals on the transmission side of the system. The LTspice and Simulink simulations informed the construction of the signal processing topology, with the designed filters, amplifiers and Schmitt Trigger used to extract the frequency difference clock reference signal. Initialisation of the utilities of the ADALM Pluto kit and exploration of its functionalities was conducted in several environments. The IIO Oscilloscope app was installed in addition to the relevant supplementary drive software, to support the transmit and receive functionality of the Pluto kit

### ADALM Pluto Simulink

Upon testing of the ADALM Pluto kit in the IIO Oscilloscope environment, the inbuilt corresponding MATLAB Simulink software package was investigated. The relevant package required for execution within the environment was downloaded and installed, in order to facilitate efficacious implementation. Once successful connection and operation of the device had been achieved, the functionality and operational parameters of both the transmit and receive ADALM Pluto Simulink block were researched.

Initial simulation revealed the prerequisite of the input to the transmit block to be complex in nature. This necessity was met through the introduction of two DSP sine waves of frequency values 900 MHz and 901 MHz, respectively. With the parameters of the receive block set to match that of the transmission block, this implementation resulted in the transmission and reception of both frequency tones. Further investigation, informed by undesirable simulation results, however, denoted that a more effective solution existed.

The absence of a block input to the Pluto transmission block in combination with the DSP feature activation would facilitate an improved implementation of the transmission of the two desired frequency tones. As the output of the reception block was also complex in nature, the signal had to be converted into a format that was suitable for entry into the signal processing necessary for clock

signal extraction. This was achieved by dividing the output into both real and imaginary arrays and then reformatting the signal. The complex signal  $x(t)$  is represented by Equation 6.

$$x(t) = a + bj \quad (6)$$

The magnitude of the complex signal is then given by Equation 7.

$$|x(t)| = \sqrt{a^2 + b^2} \quad (7)$$

This fundamental expression permits the manipulation of the signal for suitable entry into the Schmitt Trigger, thus providing the square wave output. This is demonstrated in Figure 8.

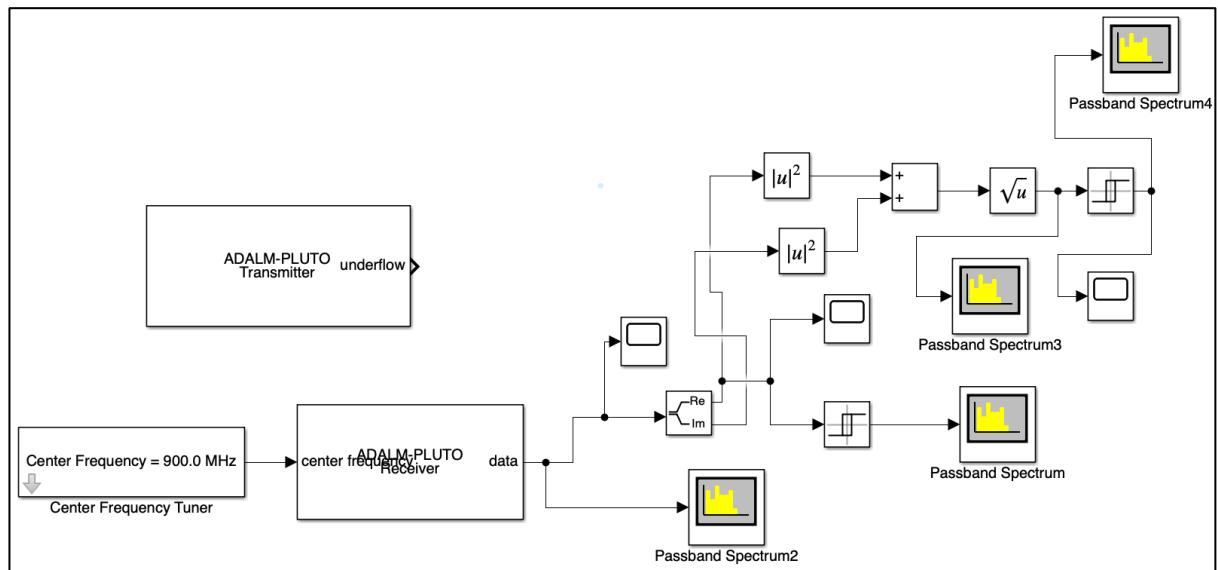
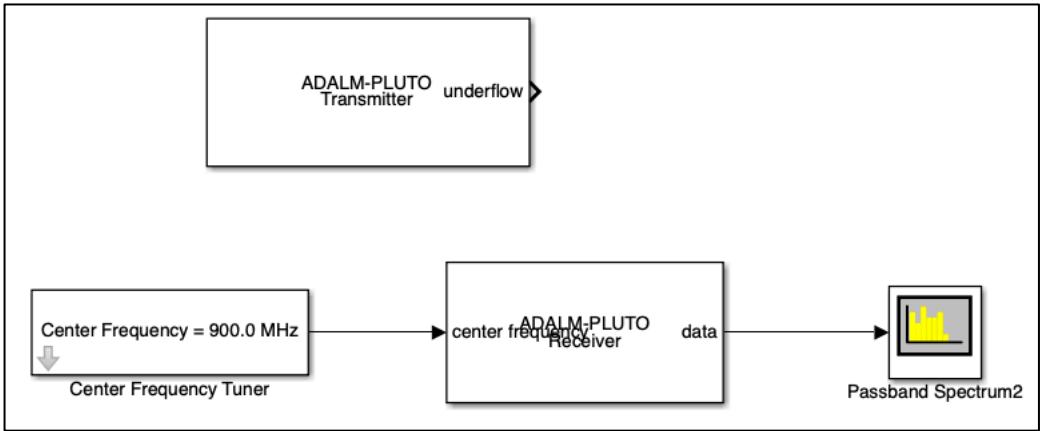


Figure 8: Pluto transmission Simulink schematic with signal processing.

The transmission and reception capabilities of the ADALM Pluto kit have been demonstrated to ensure the correct transmission of the desired frequency tones. In this project, however, the kit is only utilised for its transmission function, as demonstrated in Figure 9. The receiver is still present in the Simulink schematic, to ensure the integrity of the transmitted frequency content, through the outlet of a formatted passband spectrum.



*Figure 9: Pluto transmission Simulink schematic without signal processing.*

#### (iv) Reception Amplification Stage

The Pluto kit producing the transmitted frequency tones will, however, required an additional amplification stage prior to the already designed envelope extraction circuit. This was necessitated by the potential of the transmitted signal to have an amplitude less than the turn on voltage of the diode, in the frequency difference detector circuit. The typical turn on voltage of a Silicon diode or a Schottky diode is approximately 0.65V or 0.3V, respectively. Conducive to the efficacious operation of the diode, an amplification stage was required, to ensure that the amplitude of the signal arriving at the envelope detector circuit exceeded the chosen diode turn on voltage.

During the course of LTspice simulations of a potential amplification stage of the input signal, a variety of op-amps were trialled. The high frequency of the 900 MHz signal, combined with the requirement for an amplification stage in the order of a factor of ten, resulted in the prerequisite of a gain bandwidth product (GBW) of approximately 9 GHz. The unavailability of op-amps with a large enough gain bandwidth product in the LTspice environment meant that an effective implementation could not be simulated. For practical hardware implementation, however, there are several options for radio frequency low noise amplifiers.

#### Radio Frequency Amplifier

The unavailability of op-amps with a large enough gain bandwidth product in the LTspice environment meant that an effective op-amp amplification implementation could not be simulated at the 900 MHz input frequency. For practical hardware implementation, however, there were several options for radio frequency low noise amplifiers. The SKY66420-11 is a high-performance, highly integrated RF front-end module designed for high-power industrial, scientific and medical (ISM) band applications operating in the 860 to 930 MHz frequency range. The SKY66420-11 is designed for

ease of use and maximum flexibility with fully matched 50 TX (or TX\_ALT), RX inputs, antenna outputs and digital controls compatible with 1.6 to 3.6 V CMOS levels. The amplification radio frequency board is shown in Figure 10.

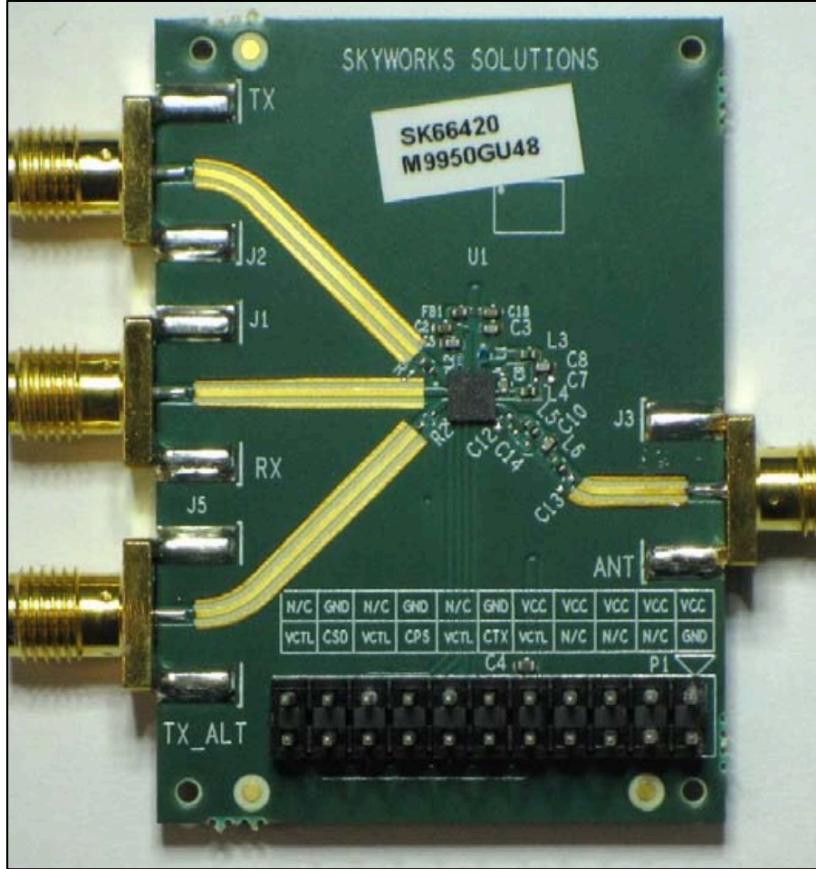


Figure 10: SKY66420-11 RF front-end amplification module [15].

### Dickson Rectifier

A conjunctive solution to the amplification requirement exists in the format of connecting a Dickson Rectifier circuit in series with the amplification stage, to further amplify the input signal [16]. The Dickson Rectifier circuit is commonly implemented within energy harvesting applications [17] and is used to facilitate voltage multiplication. The circuit uses a number of Schottky diodes, in combination with capacitors, to achieve a voltage boosting effect. An example of the implementation of the Dickson Rectifier circuit, in conjunction with an impedance matching circuit, is shown in Figure 11.

The designed LTspice Dickson Rectifier is shown in Figure 12. The voltage boosting effect achieved is visible in Figure 13, with the peak-to-peak voltage increased from an input value of 4 V to an output value of 6V.

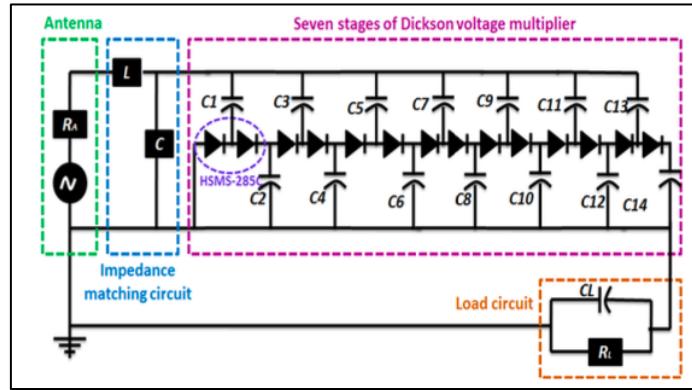


Figure 11: Dickson voltage multiplier circuit connected to an impedance matching circuit and antenna [17].

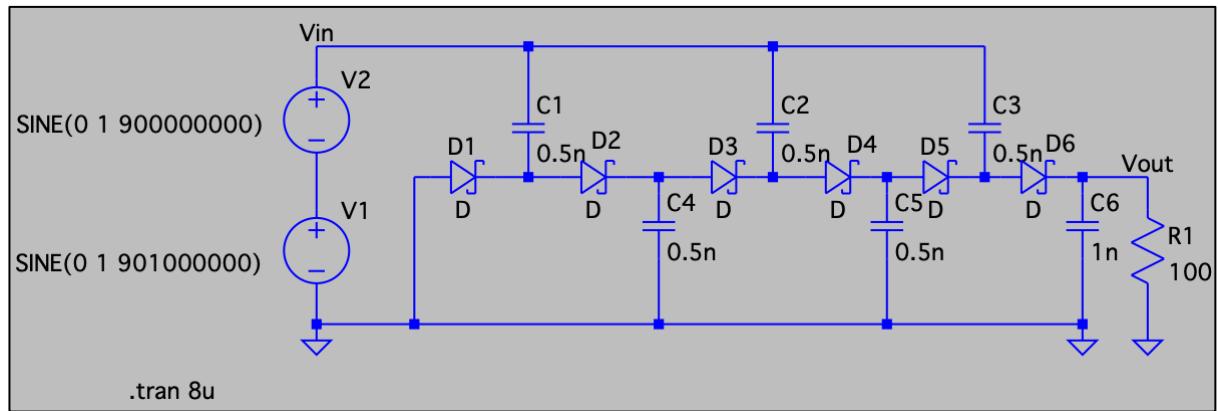


Figure 12: LTspice schematic of Dickson Rectifier.

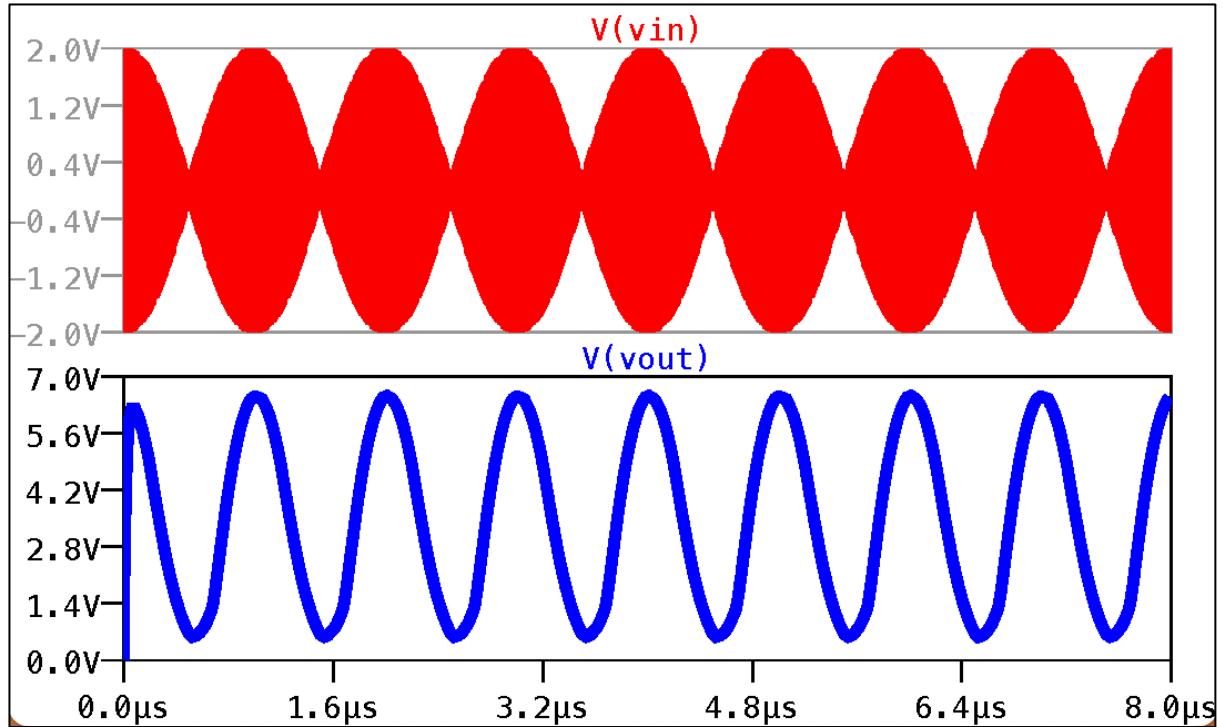


Figure 13: Simulated Dickson Rectifier input and output voltage against time.

### (v) Reception Antenna and Impedance Matching

On the reception side, in addition to the amplification stages prior to the signal filtering and processing, a suitable antenna and an accompanying impedance matching circuit was required. Impedance matching between an antenna and a transmission line is required to make the voltage reflection coefficient ( $\Gamma$ ) as close to zero as possible. This is necessary to maximize the efficiency of the transmission line.

The impedance of an antenna is frequency dependent, with the input impedance of an antenna varying with the frequency of the signal being received. This is demonstrated in Figure 14. If a single frequency signal or small frequency range of input signals are being used, then a fixed impedance matching circuit can be designed, with set inductor and capacitor values. An impedance matching system must be constructed, in order to minimize the Voltage Standing Wave Ratio (VSWR). Alternatively, an antenna tuned to have a  $50\ \Omega$  output impedance at the operating frequency can be selected. On account of this, a 900 MHz tuned, half-wave dipole antenna was used.

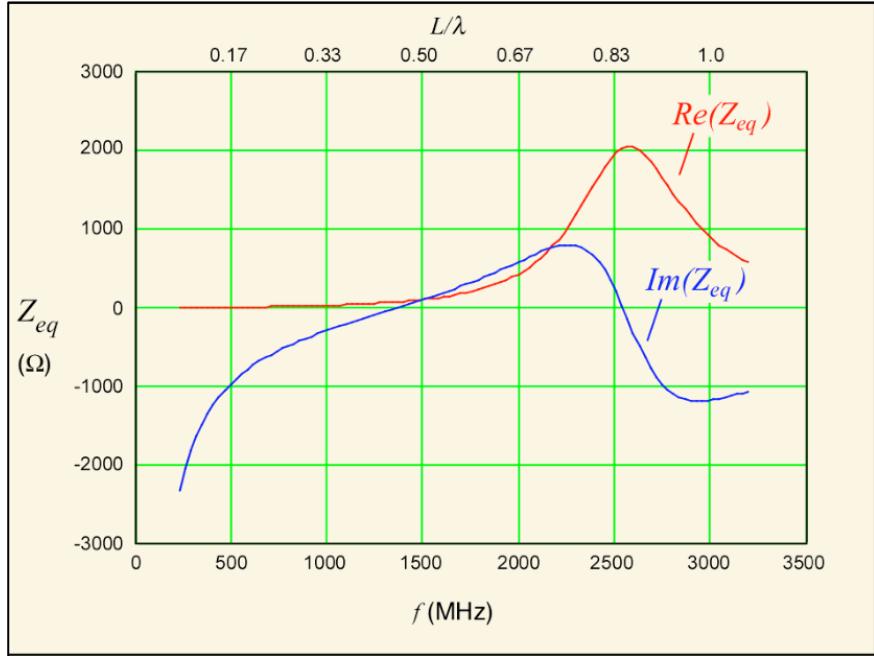


Figure 14: Graph of input impedance of dipole antenna vs. frequency, for  $a = 0.0005\lambda$  [18].

### 900 MHz Tuned Antenna



Figure 15: Standard ADALM Pluto antennae [19].

The standard ADALM Pluto antennae are not electrically resonant at 900 MHz. The wavelength of a 900 MHz signal is 33.3cm and thus the Pluto antennae are insufficient in length. This is demonstrated in Figure 15. The NanoVNA kit, a network vector analyser, was used to generate the Smith chart of

the output impedance of the Pluto antenna, under a frequency sweep. The Return Loss plot is visible in Figure 16.

As evident from Table 1, the output impedance is complex in nature and not close to the desired  $50 \Omega$  output impedance. The obtained output impedance value at 900 MHz is approximately  $100 \Omega$ . The Return Loss plot of the Pluto antenna demonstrates that it is electrically short at the 900 MHz frequency. From the frequency sweep, it is evident that the antenna is electrically resonant and demonstrates an approximate  $50 \Omega$  output impedance at a frequency of approximately 880 MHz. The Pluto antenna output impedance moves away from the desired  $50 \Omega$  output impedance and is electrically short at frequencies, above and below the 880 MHz frequency at which it is resonant.

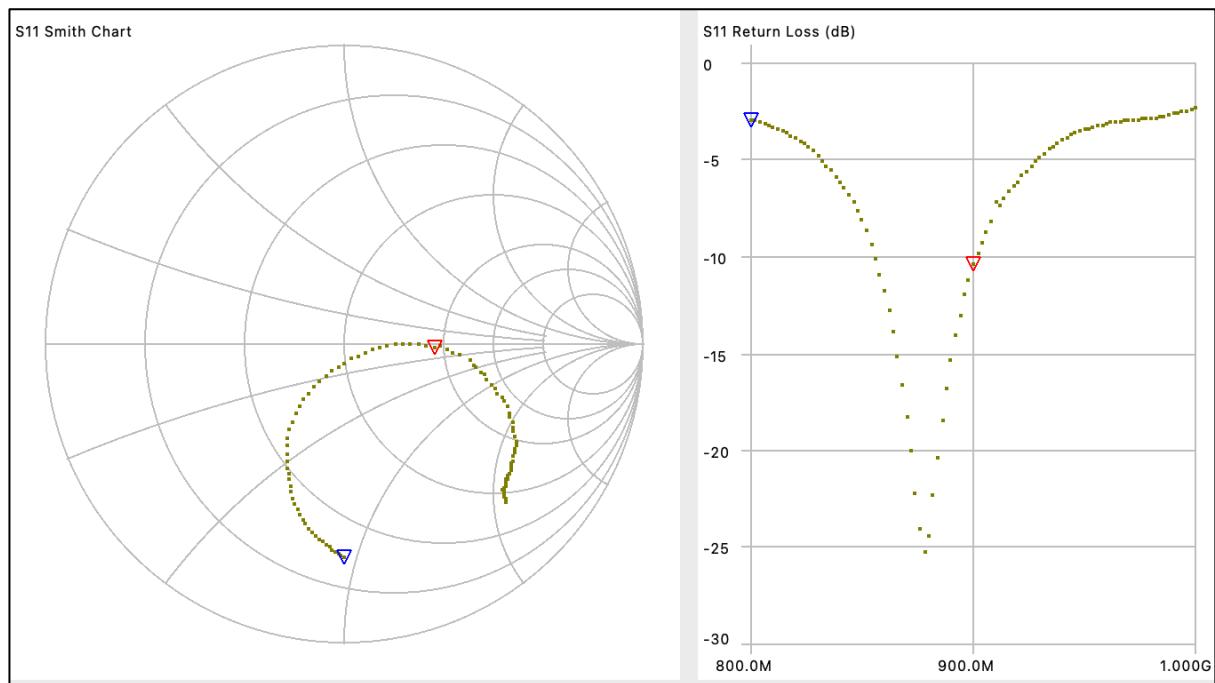


Figure 16: Smith chart and Return Loss of 890 MHz to 1 GHz frequency sweep for standard ADALM Pluto antenna.

Marker 1	
Frequency: 900.000 MHz Impedance: 92.8-j1.89 $\Omega$ Series L: -334.8 pH Series C: 93.406 pF Parallel R: 92.857 $\Omega$ Parallel X: 38.845 fF	VSWR: 1.857 Return loss: -10.455 dB Quality factor: 0.02 S11 Phase: -1.77° S21 Gain: -59.641 dB S21 Phase: 169.16°

Table 1: Output impedance of standard ADALM Pluto antenna at 900MHz.

In order to maximize the power transmitted, a half-wave dipole antenna tuned to 900 MHz was used. The Pulse Electronics W1063M antenna is shown in Figure 17. The radiating length of the half-wave antenna is 15.4 cm, as seen in Figure 18. This value is slightly shorter than half the wavelength of a

900 MHz signal, a value of 16.6 cm. The antenna is designed to have 50-ohm output impedance at the 900 MHz input frequency. The output impedance of the antenna at 900 MHz, as shown in Table 2, is very close to the desired  $50 \Omega$  output impedance. This is also reflected in the results of the frequency sweep shown in Figure 19. Discontinuities in the Smith chart and Return Loss plots are observed in the 900 MHz to 910 MHz frequency range. The discontinuity is caused by the disturbance in the NanoVNA at the 900 MHz antenna resonance. Inaccuracies in the NanoVNA interface and software may have represented the antenna output impedance as further from the desired  $50 \Omega$  output impedance, than the actual value is. The NanoVNA measurements are highly sensitive to the surrounding environment and proximity to other objects, presenting potential inaccuracies.



Figure 17: 900 MHz tuned half-wave dipole antenna [20].

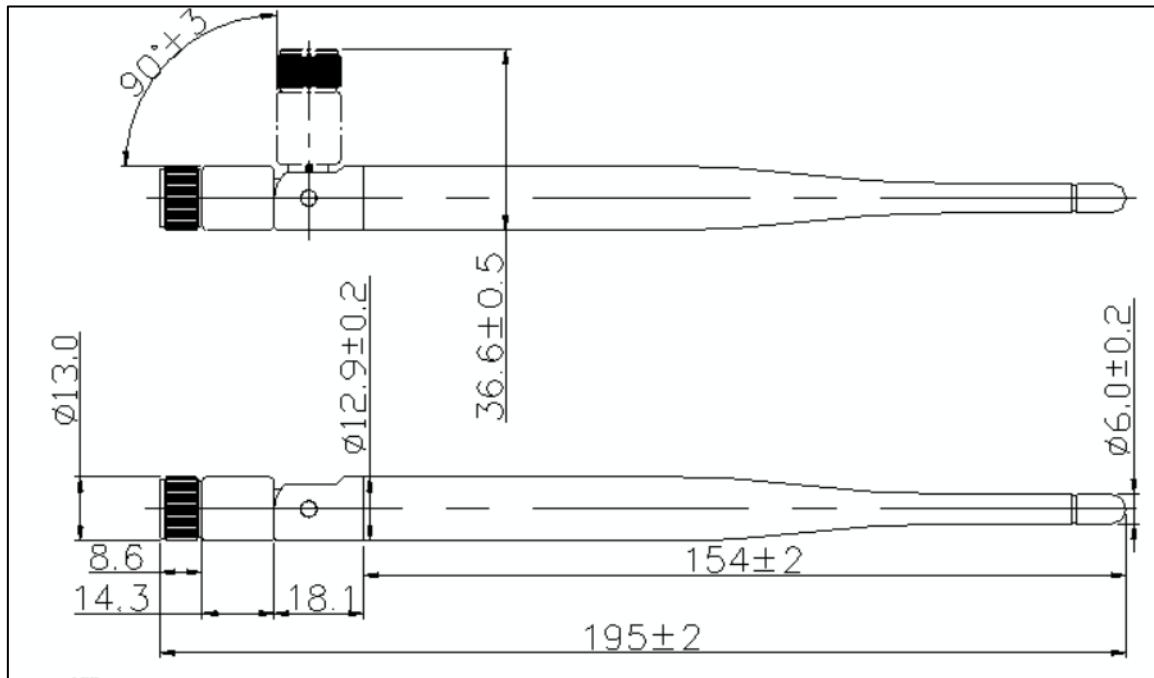


Figure 18: The Pulse Electronics W1063M antenna dimensions.

Impedance matching circuit is located within the antenna to provide  $50 \Omega$  output impedance. The output impedance of the antenna at 900 MHz is  $45.9 + j9.71 \Omega$ . This is approximately the desired  $50 \Omega$  output impedance.

Marker 1	
Frequency: 900.000 MHz Impedance: $45.9 + j9.71 \Omega$ Series L: 1.7173 nH Series C: -18.209 pF Parallel R: 47.944 $\Omega$ Parallel X: 40.062 nH	VSWR: 1.246 Return loss: -19.218 dB Quality factor: 0.212 S11 Phase: 107.16° S21 Gain: -72.117 dB S21 Phase: -26.35°

Table 2: Output impedance of 900 MHz tuned half-wave dipole antenna at 900MHz.

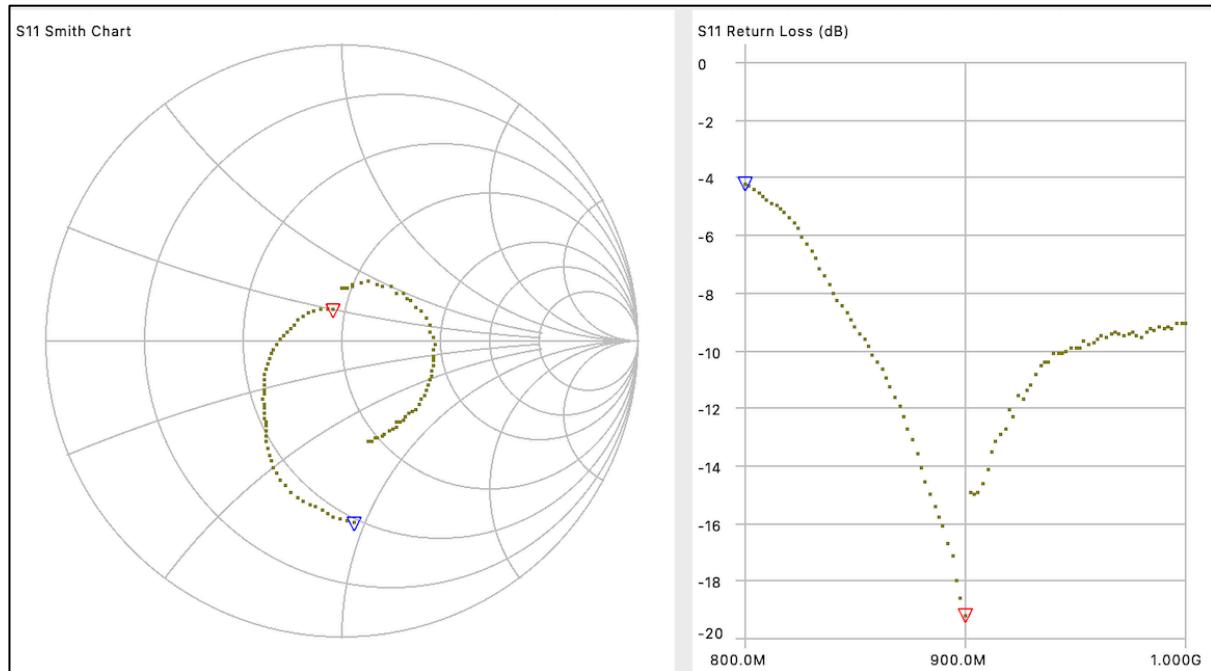


Figure 19: Smith chart and Return Loss of 890 MHz to 1 GHz frequency sweep for 900 MHz tuned half-wave dipole antenna.

## (vi) Altium

### Altium Schematic

The next step of the project saw the implementation of the system on a printed circuit board (PCB). The Altium design environment provided the appropriate software, facilitating the design. YouTube tutorials were viewed and concurrently trialled, informing the requirements for schematic construction.

To facilitate circuit construction, specific part numbers and manufacturer details were obtained, corresponding to the previously simulated component values. The importance of selecting parts currently in stock and available from the same manufacturer, enforced a clear method of comparison. The price, voltage range and functionality of each component offered additional key performance metrics. Once the relevant component details and identifier key were obtained, the value was imported into the Altium environment.

A manufacturer part search of the unique identifier key thus facilitated the capacity of download and implementation of each separate individualised footprint and component design. Through this fundamental mechanism, a schematic was designed including each component and its associated footprint. Accurate annotation of each schematic label net, facilitating connection of one or more ports, proved a pivotal construction, particularly when progressing to subsequent PCB design stages.

## Challenges

Using learnings taking form various tutorials, construction of the Altium schematic was undertaken. Each subsection of the Simulink and subsequent LTspice designs were input in the Altium environment, with effort made to obtain the cheapest parts available. Each part was obtained from the same manufacturer, in order to assist ease of procurement and potential manufacture.

Issues that arose during the formatting of the design resided in the inclusion of the appropriate headers and connections, in order to facilitate efficacious design. An example of this exists in the format of the establishment of suitable means of signal transmission, such as placing SMA connectors at the signal input to enable RF connection. The first attempt at header design was incorrectly formatted as a connector but subsequent re-design elicited the inclusion of a corrected male header.

## (vii) PCB Construction

Once the Altium schematic design had been completed, with the inclusion of corresponding footprints and models, the PCB layout and design commenced. The op-amps were initially included on the bottom layer of the PCB, to facilitate cleaner routing. Further investigation, however, alluded to the improved implementation offered by the placement of all components on the top layer of the PCB. This format would facilitate the pouring of a polygon ground on the bottom layer, with vias implemented on the top layer, to provide effective access to ground and eradicate the requirement for surplus trace routing. Breaks in the mould would then be used to facilitate routing on the bottom layer, for short lengths, avoiding trace intersection.

## Dickson Rectifier Switch

A switch facilitating the potential inclusion of a supplementary amplification stage, in the form of a Dickson Rectifier, was subsequently added. The switch was designed with the placement of two additional resistor footprints in the schematic, whose components would not be placed in the final design. This was achieved through the addition of a custom note to the manufacturer. The remaining pads can then be soldered together, if the additional amplification stage inclusion proved necessary.

## PCB Layout Formatting

The number of headers and associated pins was an aspect of the design that altered progressively, in conjunction with the design stage. Evaluation informed that an improved header format existed in the division of the power supplies and signal input and outputs into separate header boards. This facilitated a cleaner design and ameliorated user interface. Test points were also added at points after each signal filtering process. The points corresponded to the label nets used in the LTspice simulations, establishing a mechanism of comparison between the results.

The width of the power carrying PCB traces were increased in order to decrease the resistance and, thus, decrease the consequent voltage drop across the traces. This would ensure constant voltage supply. Decoupling capacitors were also placed as close to the op-amp voltage input ports as possible, in parallel to the voltage supply. This was implemented as the power carrying wire has an associated inductance and, during periods of high current demand, a consequent voltage drop is observed. This voltage drop is given by Equation 8.

$$V = L \frac{di}{dt} \quad (8)$$

The placement of a decoupling capacitor of value 10nF would offset this effect, as it would charge up during periods of low current demand and discharge at high current demand periods. This addition provides a voltage supply smoothing effect.

Hexagonal standoffs were also fitted to each corner of the PCB design, facilitating mounting of the board during testing, aiding ease of access. Effort was also made to minimise the length and number of bottom layer traces. This was to ensure that the presence of breaks in the polygon ground pour was kept to a minimum, ensuring that the ground plane was not compromised. In addition to this, a unity gain buffer was also designed for implementation. The buffer would be placed after the Dickson Rectifier to convert the high input impedance to a low output impedance, ensuring circuit performance was not compromised by the inclusion of the supplementary amplification stage.

## Completion of Design

The final design alterations in the Altium were subsequently executed. A second SMA connector was added to the schematic and PCB layout, in order to facilitate a second RF means of access to the output pin. Through this mechanism, the output square wave was now available from a male header pin, an SMA connector and through means of a test point. This variety in output format would facilitate the ease of testing and access to the output clock signal.

An additional header pin was also added to the design, to permit the separation of the voltage supplies and ground to individual header pins. The output and input pins were then moved to separate headers. This would facilitate ease of testing and a cleaner design format. The final Altium schematic is demonstrated in Figure 20.

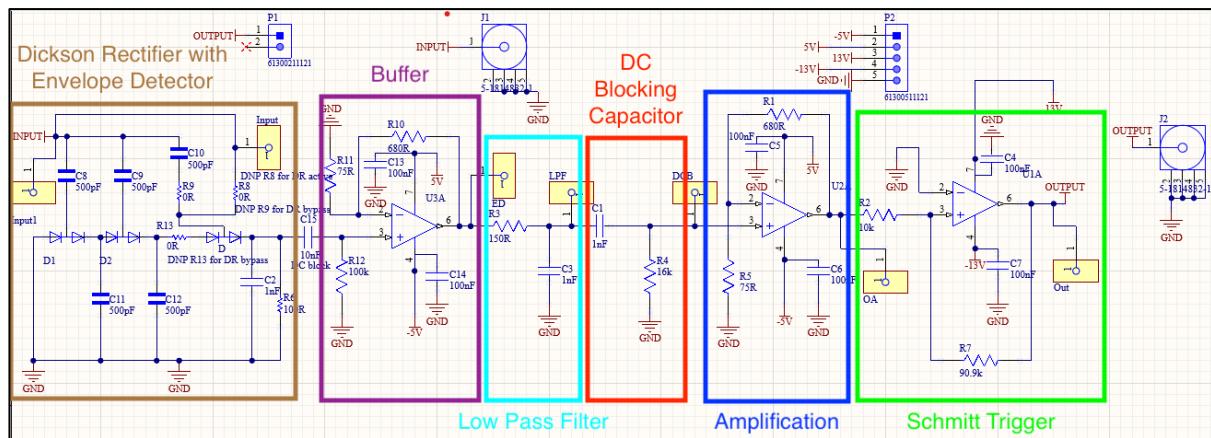


Figure 20: Final Altium schematic.

Once the headers had been formatted, the design was systematically evaluated to ensure that the smallest size component included in the design would be the 0805 module. As the PCB board design only was to be manufactured, the components would have to be attached manually, through the means of soldering. The verification process would ensure that the components were of requisite size, to enable successful implementation. Some capacitor values, however, were unavailable in the desired sizes and, as such, compromises were made. The PCB design was then sent off for production. The 2D and 3D PCB design models are displayed in Figure 21 and Figure 22, respectively.

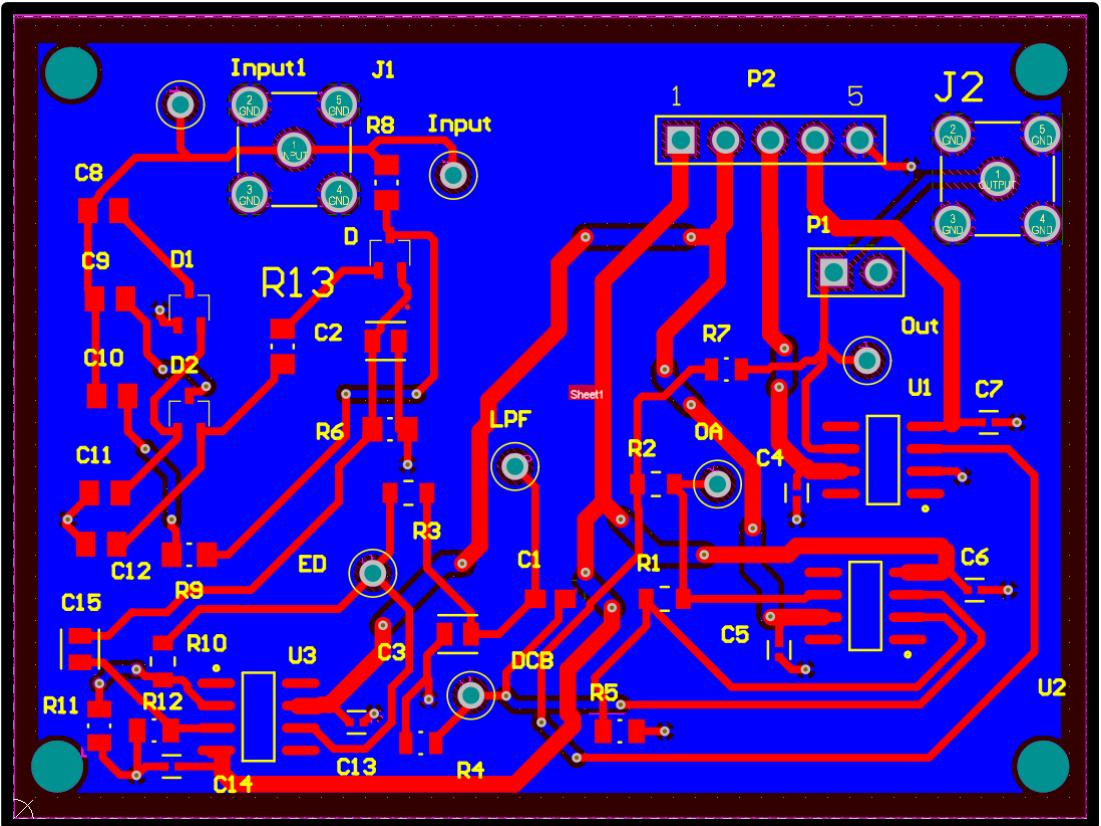


Figure 21: Altium 2D design layout

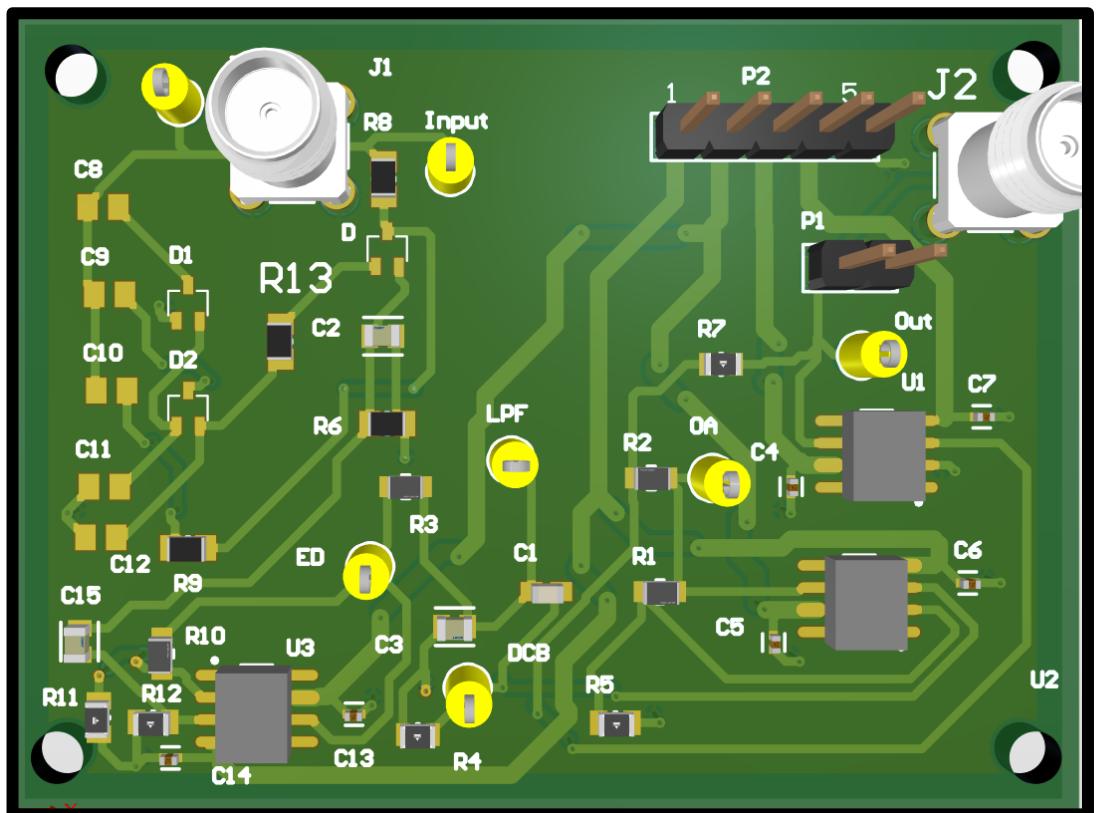


Figure 22: Altium 3D design model.

## Component Selection

Once the PCB manufacturing had been arranged, constituent component parts were then ordered. Upon analysis of the available stock options, compromises had to be made in the selection of parts, with the deadline of the open day approaching. The largest of these was in the format of the unavailability of the op-amp with the 100 MHz gain-product bandwidth op-amp. The lack of available stock of op-amps with a frequency bandwidth in this order, resulted in the selection of an op-amp with a 4MHz gain-product bandwidth. 0R resistors were also ordered in order to permit the inclusion or removal of the additional Dickson Rectifier amplification stage. A compilation of the final component order was organised and a corresponding bill of materials was generated.

A large printout of the Altium schematic and the generated 2D layout was made and labelled. A plan of execution was then formatted with the components to be attached in order of smallest component area to the largest.

## (viii) PCB Assembly

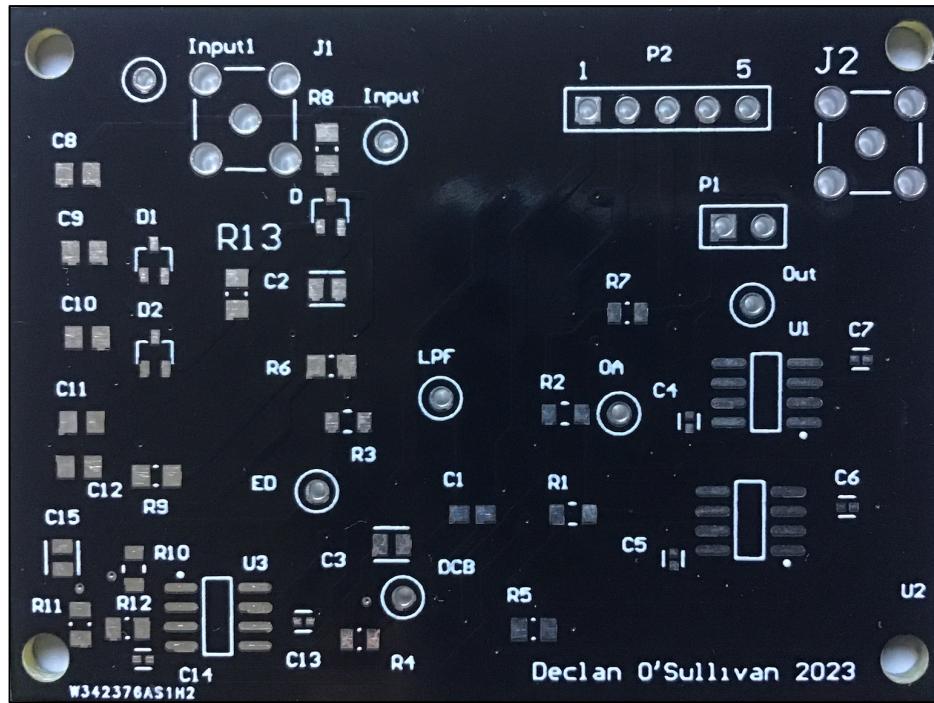


Figure 23: Unpopulated PCB design.

Upon the arrival of the PCB boards and components, the compilation of the boards was executed. The designed PCB is shown in Figure 23 . The minimum number of boards that could be ordered was five and this facilitated the population of several boards. Under this premise, two identical boards were

constructed without the Dickson Rectifier amplification stage included (Figure 24) and an additional board was constructed with the Dickson Rectifier (Figure 25). This optional inclusion was facilitated by the forementioned OR resistor values that could be included or not, acting as a switch for the Dickson Rectifier.

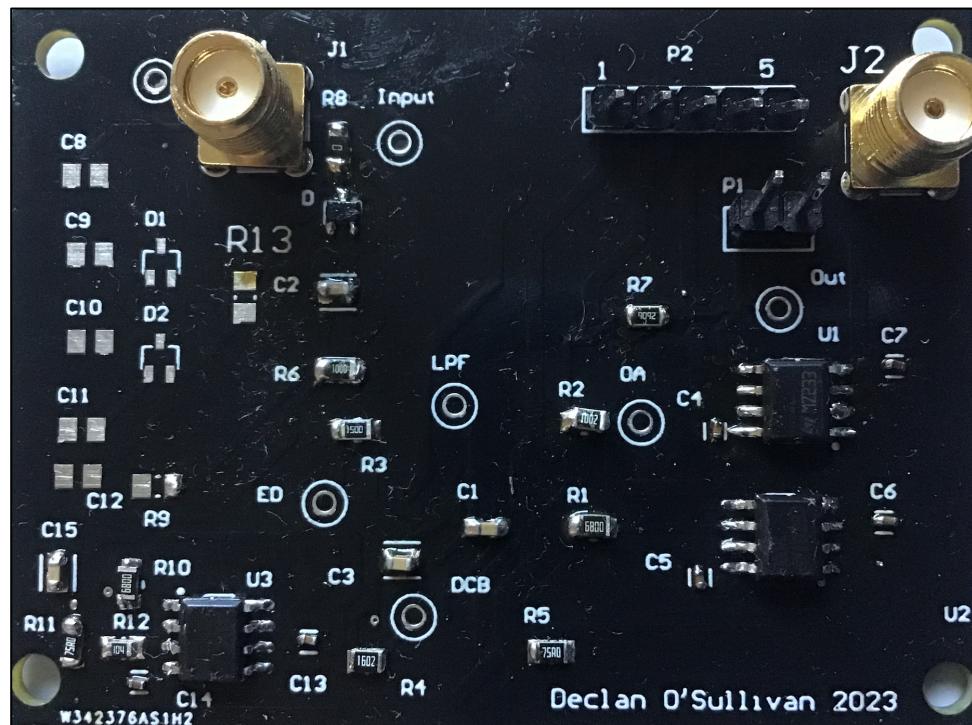


Figure 24: PCB design without Dickson Rectifier.

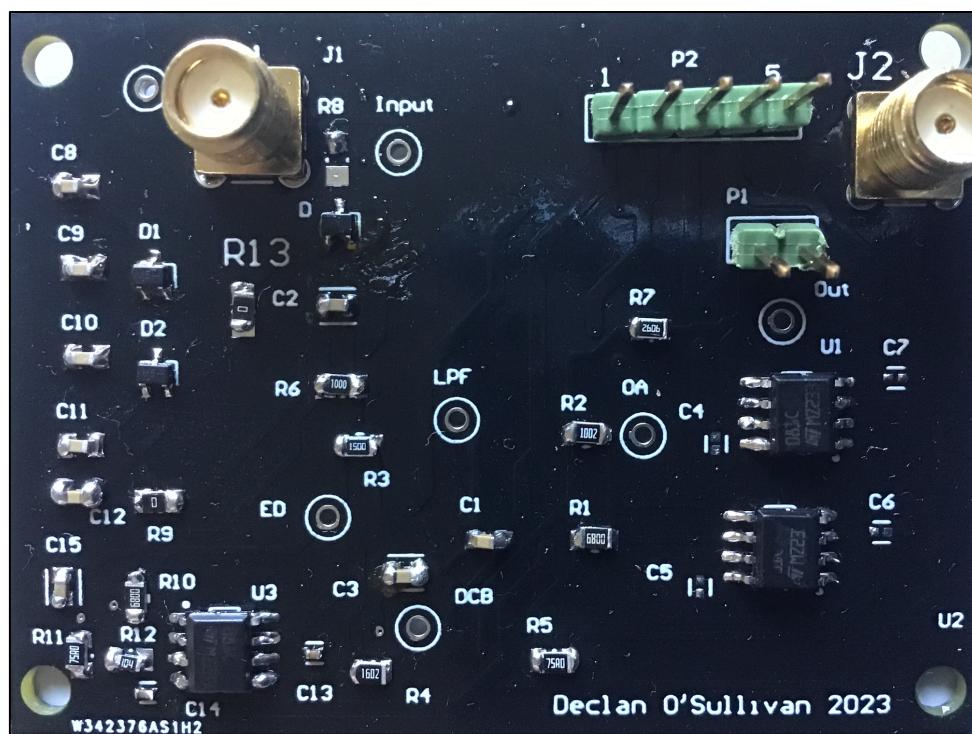


Figure 25: PCB design with Dickson Rectifier.

## PCB Design

The process of soldering was an intricate and time-consuming process, requiring constant and careful attention to detail. Initially, it was planned that the smallest component sizes would be soldered on first, as these would be the most challenging to attach. A more effective solution, however, consisted of the attachment of the larger 0805 module components first. This method would permit the practice of repetitive component soldering, improving technique and skill, before the smallest capacitor values were attached.

## Soldering

Problems encountered during the soldering process were mainly focused in the area surrounding the op-amps. The first difficulty arose in the format of establishing the correct orientation of the op-amps. The first pin of an op-amp is typically indicated by the inclusion of a white dot on one side of the op-amp. The ordered op-amp included white dots on both sides of the op-amp and consultation of the corresponding component datasheet failed to offer clarity on the matter. Further research, however, revealed that the first pin was marked by a 45 degree slope present on the first op-amp pin.

The decoupling capacitors located as close to the op-amp power supply pins as possible, proved to be the most difficult component inclusion in each board. This was partially as a consequence of the proximity to the op-amp pins but mostly as a result of the miniature component size. A decoupling capacitor is shown in Figure 26. With the presence of two power supply pins on each op-amp, three op-amps per board and one capacitor per power supply pin, six decoupling capacitors were to be attached per board.

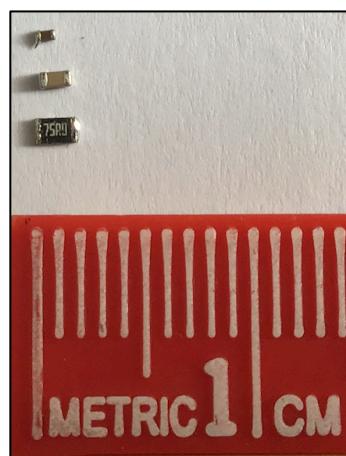


Figure 26: Comparison of component sizes with decoupling capacitor on top, 0805 module sized capacitor below and 0805 module sized resistor on the bottom.

The difficulty of the attachment of the miniature decoupling capacitors would have been partially negated in the presence of an increased pad size. The combination of minimal contact area and the millimetre scale upon which the soldering was conducted, concluded in a challenging undertaking. In addition to this, the op-amp pin proximity frequently caused the connection of overlapping solder, melting away previously secured connections. The op-amp component was also difficult to solder, with the proximity of the pins often resulting in the undesired shorting of pins.

The removal of undesired solder was facilitated by the use of flux wire, which absorbed surplus solder, upon the application of heat. This tool, in combination with the flux pen, was leveraged to create tidier connections and improve the final visual display of the design. PCB clean was then carefully applied, in order to remove staining and provide an overall clean of the design.

## (ix) PCB Testing

Prior to the application of voltage to the PCB and the testing of the populated board, safety checks had to be executed. This was to ensure the presence of no shorts or faulty connections, that could potentially result in smoking or component failure. This was conducted using the continuity function in a multimeter, where the presence of a connection between the two multimeter probes results in the production of a buzzing sound. This ensured that no power or ground pins were shorted.

### Voltage Supply Pins

The voltage supply of the Schmitt Trigger was initially established as +13V. During the course of simulations of the operating conditions of the trigger, however, it became evident successful operation could be achieved with the same voltage supply of +5V as used in the buffer and amplification op-amp stages. The purpose of labelling the supply as +13V was to distinguish the supply from the other op-amp stages. Under this premise, the +13V supply pin was shorted to the +5V supply and, conversely, the -13V supply was connected to the -5V supply. This was achieved by soldering a wire between both sets of pins.

Once the voltage supply pins were formatted and all connections were validated, the board was supplied with power. The current did not exceed the set rating on the dual voltage supply, thus indicating the absence of shorted connections. In order to effectively execute debugging of the board, the test points present at each design stage were used to ensure correct operation of each design stage. This was achieved by soldering a wire at the test point to each design stage, thus allowing an appropriate input signal to be applied to the input of the selected design stage.

## PCB Debugging

The first stage to be tested was the buffer op-amp stage. Upon the application of the input signal, it became apparent, through the mechanism of the oscilloscope probe pins, that there was no signal present on the output pin of the op-amp. Under this premise, the signal was followed through each component present in the stage, revealing the presence of an incomplete connection. The buffer stage had been formatted with the option for an additional amplification stage that could be omitted or included based on the required amplification. The stage had been negated by shorting the gain resistor's pins together but testing revealed that this connection was not properly executed. The PCB was thus reformatted by the removal of the soldered short and insertion of another 0R resistor. This zero resistance component would perform the same function as the soldered short. Testing revealed the output of the buffer stage was now formatting correctly.

The low pass filter stage and DC blocking capacitor stage were subsequently verified by testing but an additional inconsistency arose in the final op-amp amplification stage. Through a similar debugging process, however, several faulty connections were identified. One of these issues was caused by a resistor holding an area too large in value for the pad, on which it was to be placed, preventing secure connection. This issue was rectified by the use of a smaller resistor size, of the same resistance value. Additional re-soldering touch ups of other design stage components, ensuring pad connections, concluded with the successful implementation of all design stages.

## 8. Discussion of Key Results Achieved

### (i) Simulink

To assess the validity of the Simulink design and the operational capacity of the system, the operating conditions of the system were evaluated. The SNR in dB is defined in Equation 9.

$$SNR \text{ (dB)} = 20\log_{10} \frac{\text{Signal Power in Watts}}{\text{Noise Power in Watts}} \quad (9)$$

In order to accurately assess the performance metrics of the system, the range of SNR values for which the output clock maintains sufficient performance was evaluated. Sufficient clock performance is defined as the clock signal maintaining a 50% duty cycle. This is demonstrated by the output shown in Figure 27, as obtained from one of the simulations. To calculate the SNR for each adjustment in noise power, both the summed sinusoidal signals without the noise and the noise itself, were exported

from Simulink into the MATLAB workspace. This was achieved by converting both exports into three dimensional arrays, concatenated along the third dimension.

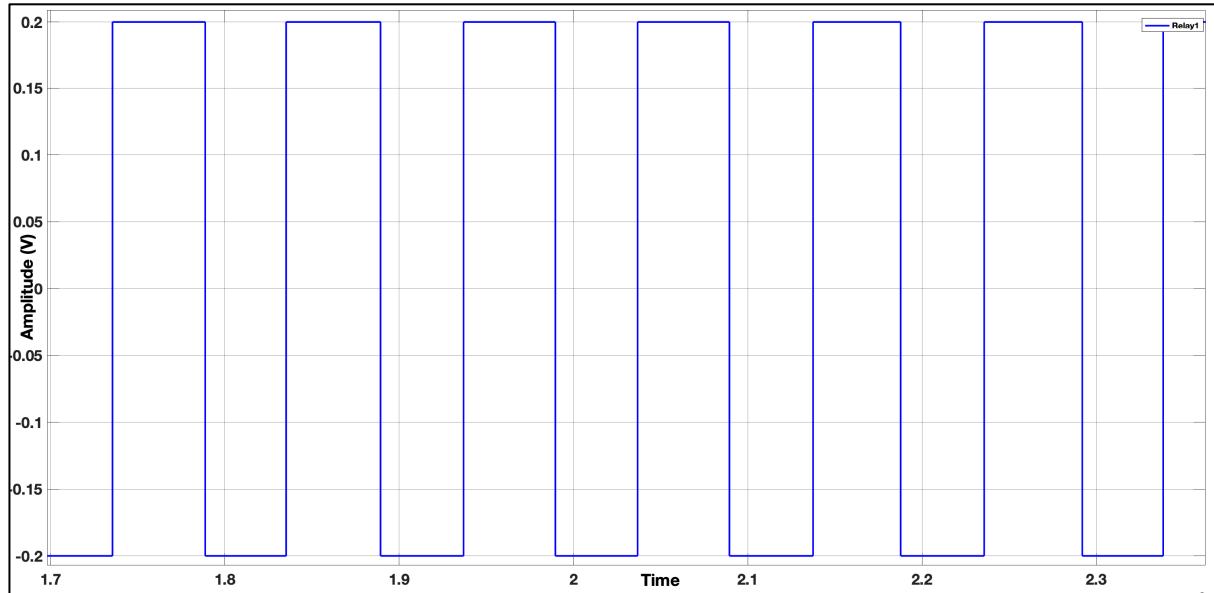


Figure 27: Clock reference signal with 50% duty cycle.

Once both arrays were exported to the MATLAB workspace, the previously described SNR equation was formatted, with the arrays inputted. The obtained SNR value was noted and the duty cycle of the corresponding clock output (Schmitt Trigger output) was then calculated. This was repeated for increasing values of noise power (decreasing SNR values) until the duty cycle returned a value not equal to the required 50% duty, indicating that the clock function was compromised. As evident from Figure 28, it was established that the system operates effectively for SNR values of  $\text{SNR} \geq 7.0332\text{dB}$ .

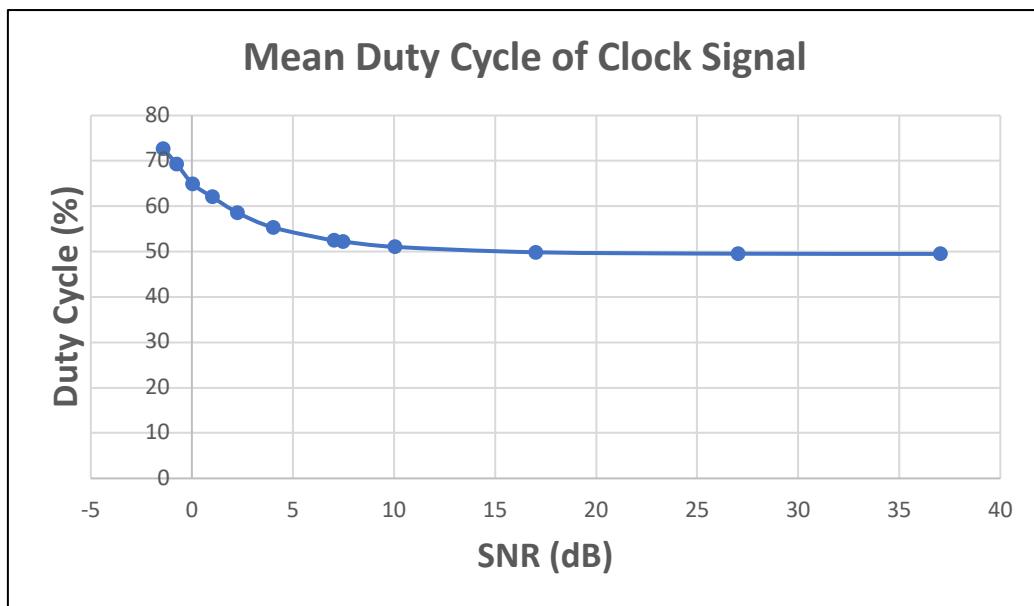


Figure 28: Mean Duty of clock signal for different SNR values.

A similar process was also conducted, conducive to obtaining the average period of the clock signal, under varying conditions of noise power. This was achieved by taking the time between consecutive highs and averaging them over fifty periods. The results of these calculations reflect the previous performance assessment and are visible in Figure 29. Through these fundamental mechanisms, graphs were developed for both the duty cycle and the period of the output clock wave, against the SNR value of the sinusoidal input. This facilitated the calculation and clear visual depiction of each resulting relationship and the consequent operating points of the system.

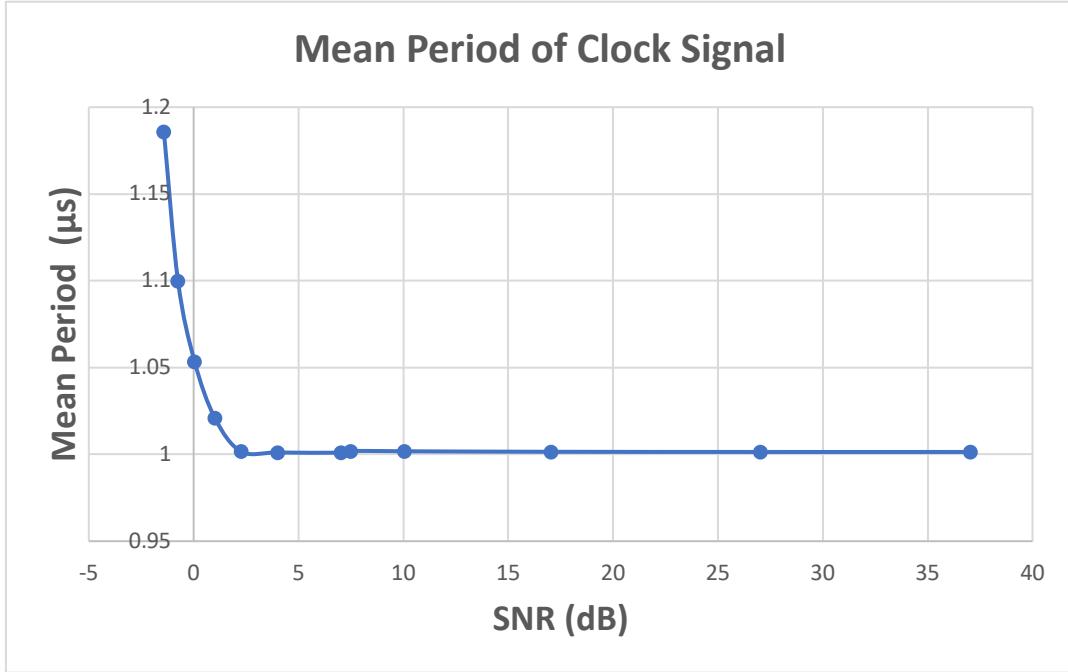


Figure 29: Mean period of clock signal for different SNR values.

## (ii) LTspice

The conduction of the Simulink simulations and the calculation of its operating points permitted the completion of a wider simulation chain, before the compilation of a real component driven representation of the model. This component simulation, constructed in LTspice, yielded the desired 1 MHz clock reference signal. The square wave clock signal with a frequency of 1 MHz and a duty cycle of 50% is seen in Figure 30, in addition to the output at each prior stage of signal processing.

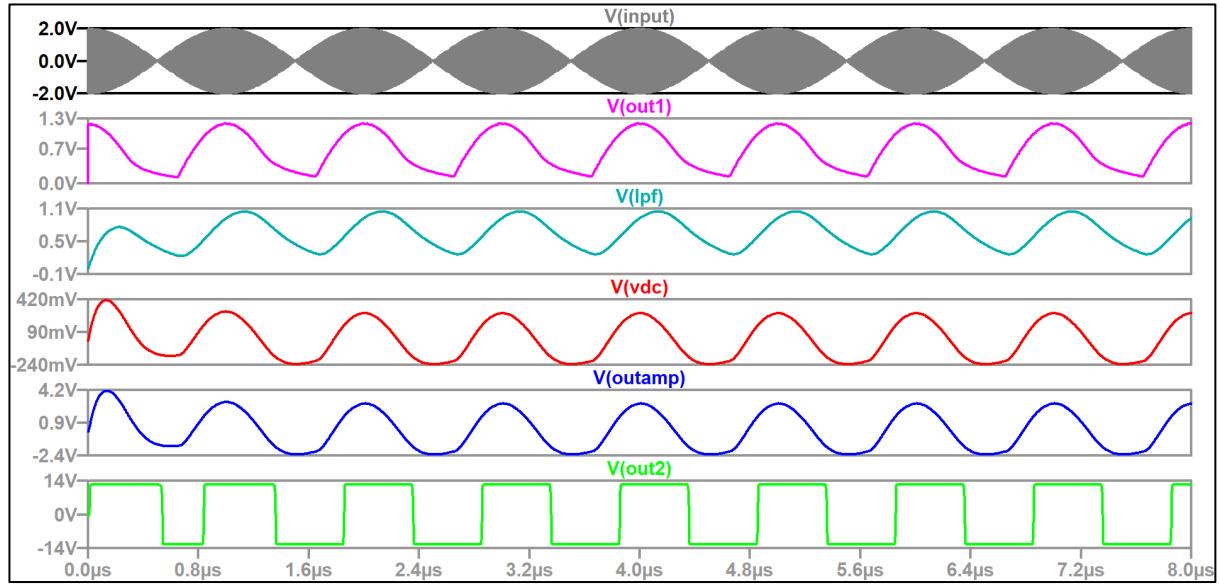


Figure 30: Output voltages at nodes labelled ‘in’ (input voltage), ‘out1’ (after envelope detector circuit), ‘vdc’ (after DC blocking capacitor), ‘lpf’ (after low pass filter) , ‘outamp’ (after amplification) and ‘out2’ (after Schmitt Trigger).

The final LTspice schematic with Dickson Rectifier is shown in Figure 31. The input signal amplitude has been reduced by 40% but the Dickson Rectifier permits the maintenance of circuit function. The Dickson Rectifier boosts input voltage before entry into envelope detector circuit. The results are shown in Figure 32.

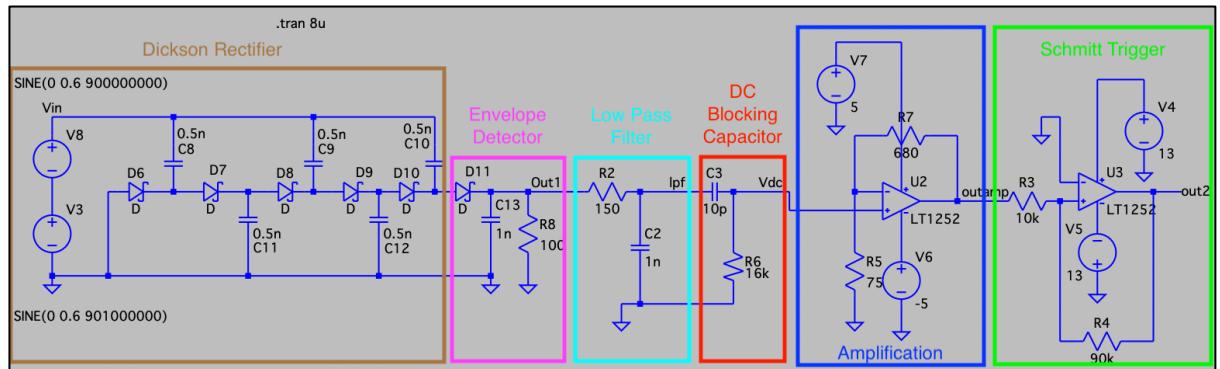


Figure 31: LTspice schematic with Dickson Rectifier.

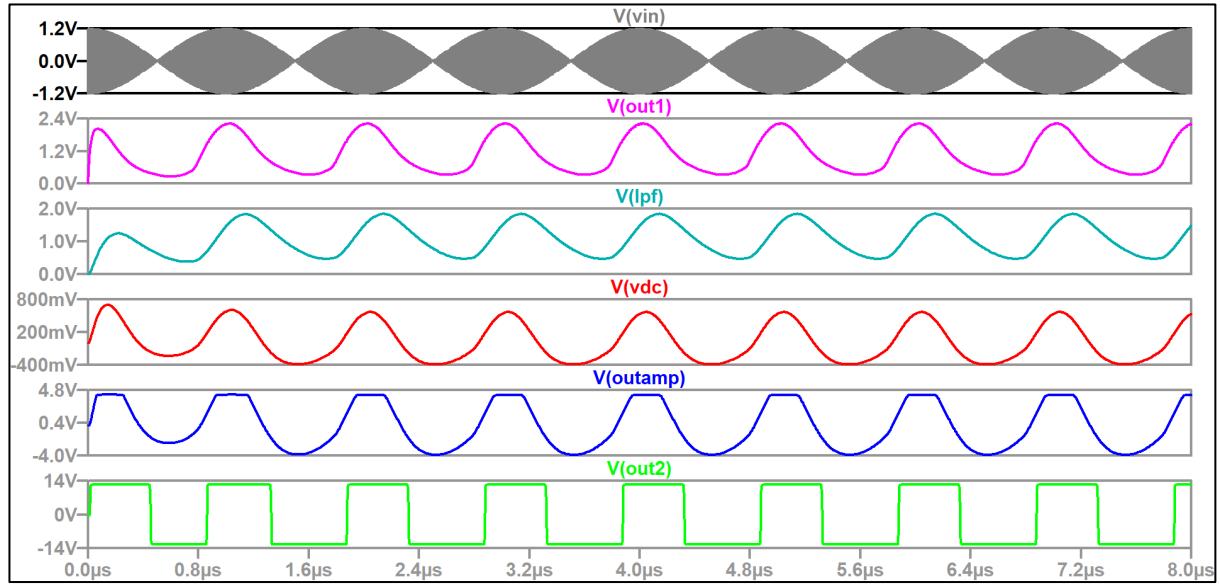


Figure 32: LTspice simulation results with Dickson Rectifier and colour coding corresponding to each schematic design stage.

### (iii) ADALM Pluto Kit

The spectrum of the transmitted signal, containing the frequency tones at 900 MHz and 901 MHz, is shown in Figure 33. This visual depiction is achieved using the passband spectrum block, in the Simulink environment. Both frequency tones are transmitted at a low power value of -20 dBm.

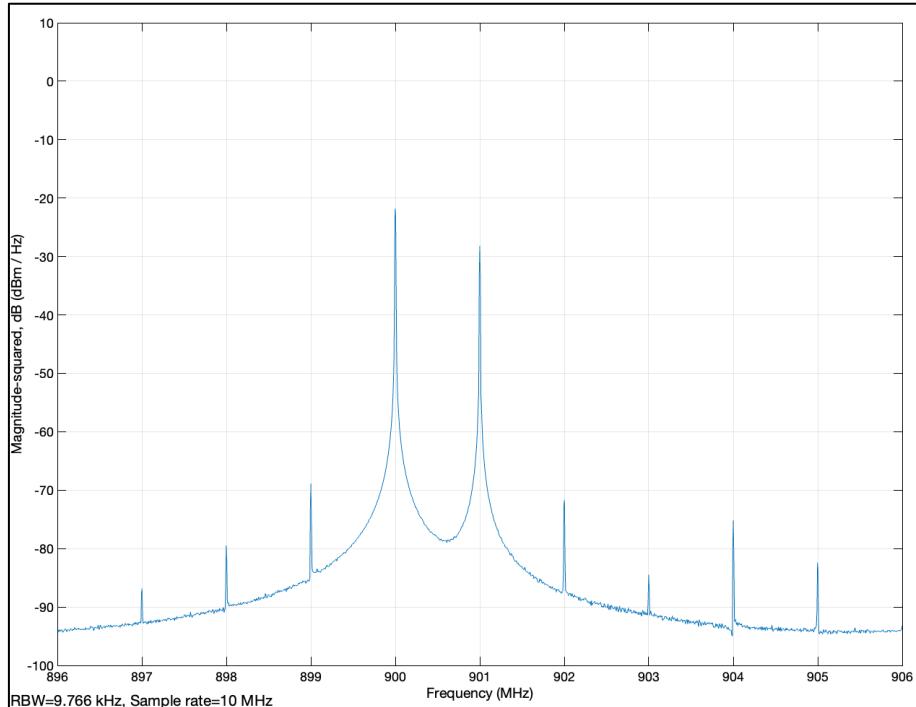


Figure 33: Passband spectrum of transmitting ADALM Pluto at 900 MHz and 901 MHz frequency tones.

#### (iv) PCB Final Design

The ADLM Pluto Simulink package was connected to the device and the frequency tones at 900 MHz and 901 MHz transmitted. Probing of the test points revealed that successful operation had been achieved for all the design stages, except for the final Schmitt Trigger design stage. This indicated the successful extraction of the 1 MHz difference frequency signal and signal processing stages but the infectivity of the sine to square wave conversion. Informed by testing using the signal generator, it was evident that the Schmitt Trigger stage did operate effectively. It was determined that the Pluto was transmitting the frequency tones at too low of a power level, -20 dBm.

#### Additional Amplification

In order to rectify the low input signal power, the optional amplification was added to the buffer stage. Upon the establishment of the requirement of this supplementary stage, through testing, the gain stage of the final amplification and Schmitt Trigger stage were increased to maximum values. This was achieved by conducting increasing iterative replacements of the amplification and Schmitt Trigger gain resistors from  $680 \Omega$  to  $100 \text{ k}\Omega$  and from  $90.9 \text{ k}\Omega$  to  $1 \text{ M}\Omega$ , respectively. Through this iterative process, it was determined that the bandwidth of the replacement op-amp was insufficient to support effective operation of the Schmitt Trigger at the 1 MHz frequency.

#### Op-amp Gain Product Bandwidth

The challenges caused by the aforementioned unavailability of the simulated op-amps, was further compounded by testing using the signal generator. Input frequencies were increased steadily from 100 kHz to 1 MHz on the signal generator, revealing that the Schmitt Trigger only operated for frequencies less than 200kHz. The limiting factor of the replacement op-amp gain product bandwidth, however, was negated by operating the system at the 100 kHz range, as opposed to the designed 1 MHz range. This was achieved by altering the Pluto transmitted frequency tones to 900 MHz and 900.1 MHz. Through this fundamental design mechanism, a 100 kHz difference frequency was obtained.

#### Frequency Difference Alteration ( $f_1-f_2 = 100 \text{ kHz}$ )

With the difference frequency altered to 100 kHz, the circuit had to be altered to suitably process the new frequency. Fundamentally, the only two stages that required alteration were the envelope detector and low pass filter design stages. The alteration involved the increased scaling of the resistors in both the design stages by a factor of 10. The previously maximised gain stages were then returned to the

initial design stages, to ensure that the op-amps executed efficacious implementation, at their operating conditions. The improved operation of the Dickson Rectifier at the lower frequency value also informed this decision.

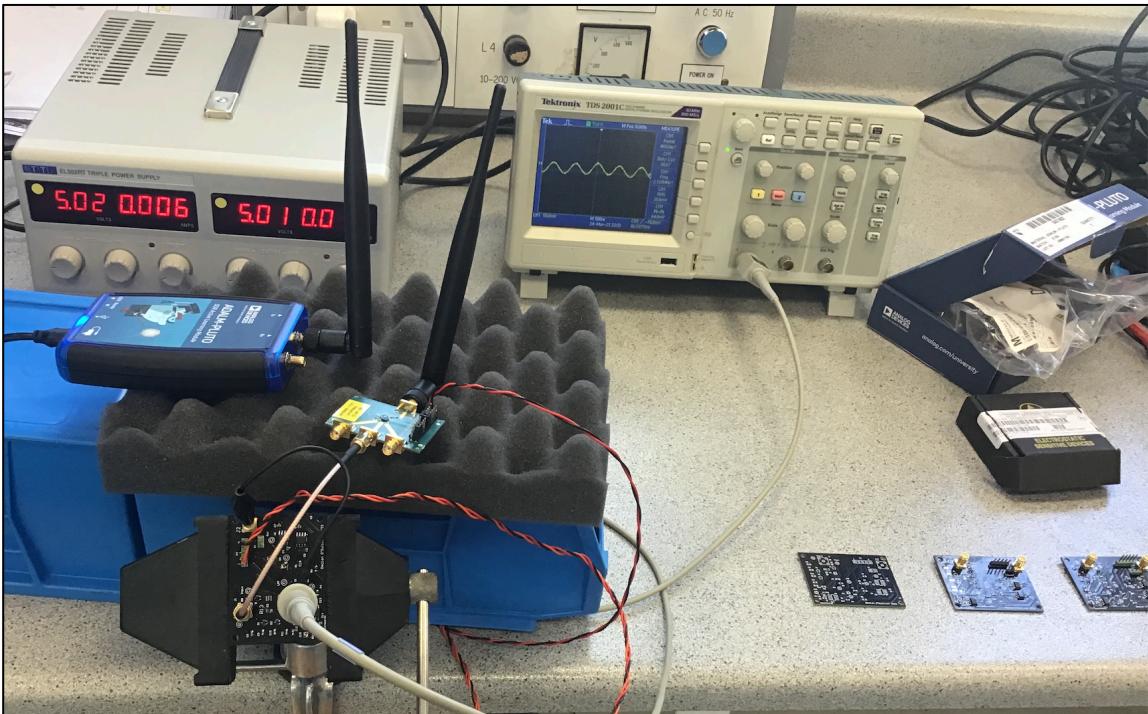


Figure 34: Final design setup.

Period: 9.786 $\mu$ s	Period: 9.877 $\mu$ s	Period: 9.975 $\mu$ s	Period: 9.963 $\mu$ s	Period: 9.943 $\mu$ s
Frequency: 102.184 kHz	Frequency: 101.240 kHz	Frequency: 100.251 kHz	Frequency: 100.374 kHz	Frequency: 100.571 kHz
Peak-peak: 5.895 V	Peak-peak: 2.037 V	Peak-peak: 1.589 V	Peak-peak: 1.682 V	Peak-peak: 5.509 V
Mean: 305.303 mV	Mean: 778.703 mV	Mean: 772.663 mV	Mean: -10.480 mV	Mean: -2.733 mV

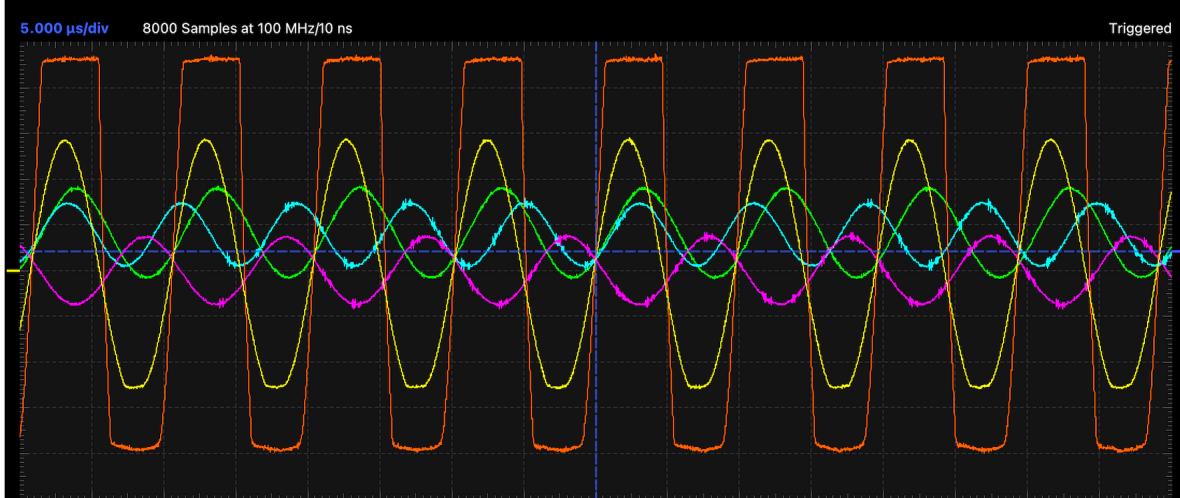


Figure 35: Generated outputs at each stage using ADALM 2000 Scopy interface. Output voltages at nodes coloured 'green' (after envelope detector circuit), 'turquoise' (after DC blocking capacitor), 'pink' (after low pass filter) , 'yellow' (after amplification) and 'orange' (after Schmitt Trigger).

The final design is shown in Figure 34. Each design stage now operated effectively, at the lower frequency of 100 kHz. The output results, including the final 100kHz square wave difference frequency clock signal, are seen in Figure 35. It was determined that the design maintained the desired output clock signal duty cycle of 50% for a range of <= 14cm.

## 9. Cost of Design

Description	Designator	Supplier	Supplier Unit Price	Quantity	Cost (\$)
CAP 1000PF 0805	C1, C2, C3, C15	Digi-Key	\$0.73	4	2.92
CAP 0.1UF 0402	C4, C5, C6, C7, C13, C14	Digi-Key	\$0.04	6	0.222
CAP 500P 0805	C8, C9, C10, C11, C12	Digi-Key	\$0.27	5	1.35
Schottky Diodes	D, D1, D2	Digi-Key	\$0.67	3	2.01
SMA Connector	J1, J2	Digi-Key	\$4.22	2	8.44
Pin Header 2 pins	P1	Digi-Key	\$0.13	1	0.13
Pin Header 5 pins	P2	Digi-Key	\$0.26	1	0.26
RES 680 OHM 0805	R1, R10	Digi-Key	\$0.10	2	0.2
RES 10K OHM 0805	R2	Digi-Key	\$0.10	1	0.1
Res 150 Ohm 0805	R3	Digi-Key	\$0.10	1	0.1
RES 16kΩ 0805	R4	Digi-Key	\$0.10	1	0.1
RES 75Ω 0805	R5, R11, R12	Digi-Key	\$0.10	3	0.3
Resistor 100 Ohm 0805	R6, R8, R9, R13	Digi-Key	\$0.03	4	0.1
RES 1MΩ 0805	R7	Digi-Key	\$0.28	1	0.28
Single Channel, High voltage Video Operational Amplifier, 4 MHz Typical GBW	U1, U2, U3	Digi-Key	\$0.58	3	1.74
<b>Total Cost (\$)</b>					<b>18.25</b>

Table 3: Components costs for each board.

The cost for each component in the PCB is shown in Table 3. The total cost of components per board was \$18.25 and the cost of manufacture for each unpopulated PCB was \$1. This provides an overall cost of \$19.25 per constructed PCB, not including the cost of shipping for the designed PCB's.

The minimum board order from the manufacturer was 5. The shipping costs totalled \$61.70, as shown in Table 4. These shipping costs, however, are independent of the number of boards. Under this premise, the shipping costs are listed as a fixed cost, as opposed to a cost per unit.

<b>Board Size</b>	<b>45.4mm × 61mm</b>
<b>Price per Board</b>	<b>\$ 1.00</b>
Total Boards Price (5)	\$ 5.00
Total Freight Cost	\$ 30.07
DDP Service Fee	\$ 16.00
Bank Fee	\$ 3.16
Duty & Tax	\$ 12.47
<b>Total Cost</b>	<b>\$ 66.70</b>

Table 4: PCB manufacturing and shipping costs.

## 10. Future Work

Future progression within the project will be focused upon expanding the range capabilities of the design. Analog Devices, the manufacturer of the ADALM Pluto kit, offers a low cost amplifier that can be attached to the Pluto device, in order to greatly increase the output power of the transmitted frequency tones. Under this premise, the range capabilities of the device could be dramatically increased. The RF amplifier is shown in Figure 36. The presence of this supplementary amplification device could potentially negate the requirement for the additional amplification op-amp stage, decreasing the size of the design. The conjunctive measure of reducing the distance between components and the removal of amplification stages, that are surplus to requirement, would greatly reduce the area of the PCB design.

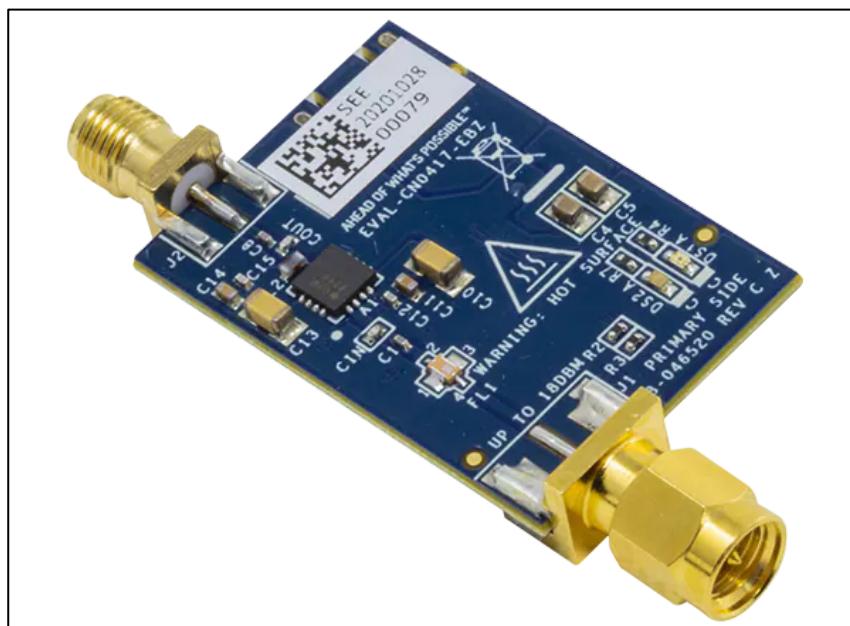


Figure 36: Analog Devices EVAL-CN0417-EBZ 2.4GHz RF Power Amplifier [21].

The alignment of the rising edges, jitter patterns, phase offsets and duty cycles could also be investigated across multiple reception nodes. This would be achieved by compiling multiple boards and placing them at both the same and different distances from the device transmitting the frequency tones. The relationship between each feature and the imposed range from the transmitter could then be generated.

An additional measure to be added to the design exists in the format of replacing the resistors in the envelope detector circuit and the low pass filter circuit with potentiometers. Through this mechanism, the design could be instantaneously altered to extract and generate a clock signal equal to the difference frequency of any two transmitted frequency tones. Under these outlined premises, a more compact design, with greater range and frequency operating capabilities, could be compiled.

## Conclusion

The final design successfully executed the extraction of the transmitted difference frequency signal of 100 kHz. The capability of the design to operate effectively at 1 MHz, with the inclusion of op-amps offering the requisite gain-product bandwidth, has also been demonstrated. The design can be applied to a wide frequency range, through the simple manipulation of the resistor values in the envelope detector and low pass filter design stages. The operation frequency range of the design can be further increased by the inclusion of op-amps with larger frequency bandwidths.

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