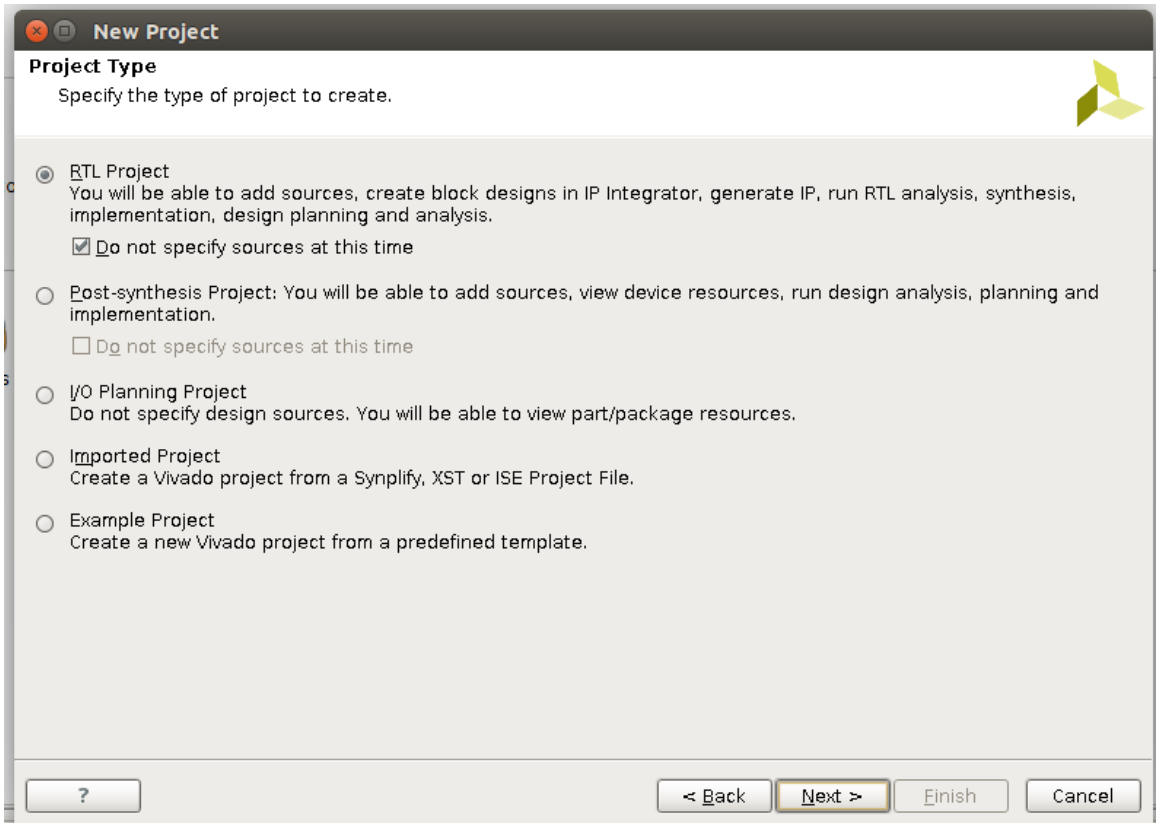
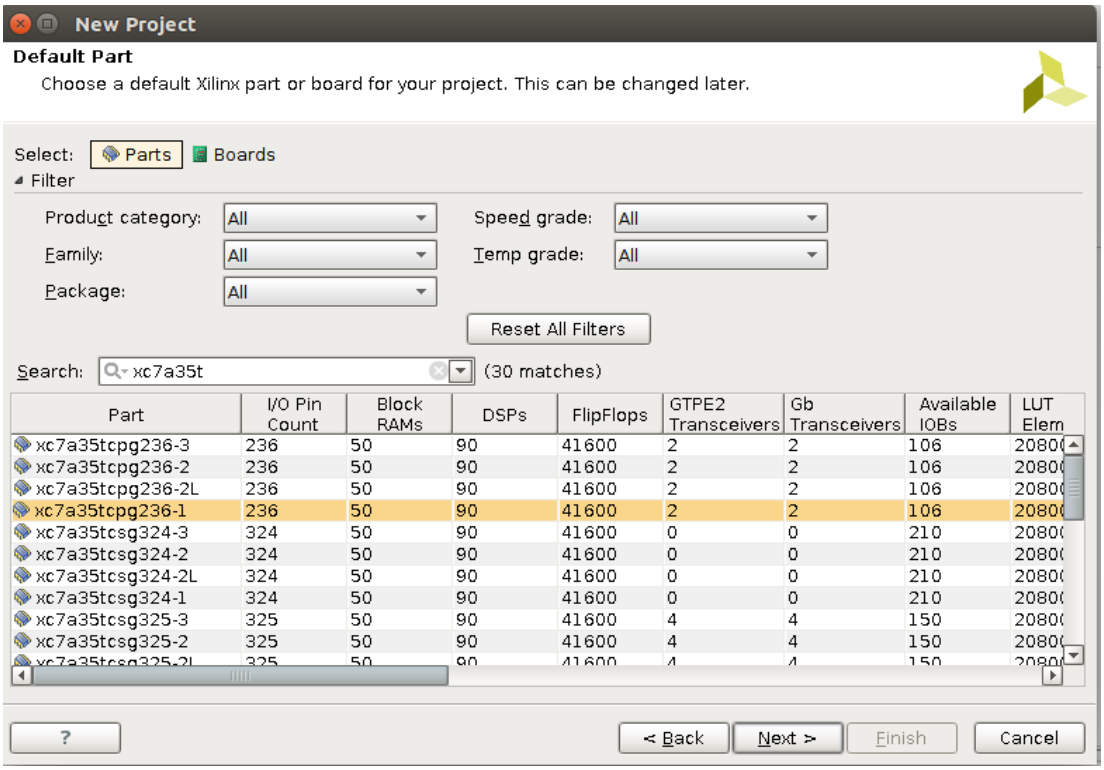
Using Vivado

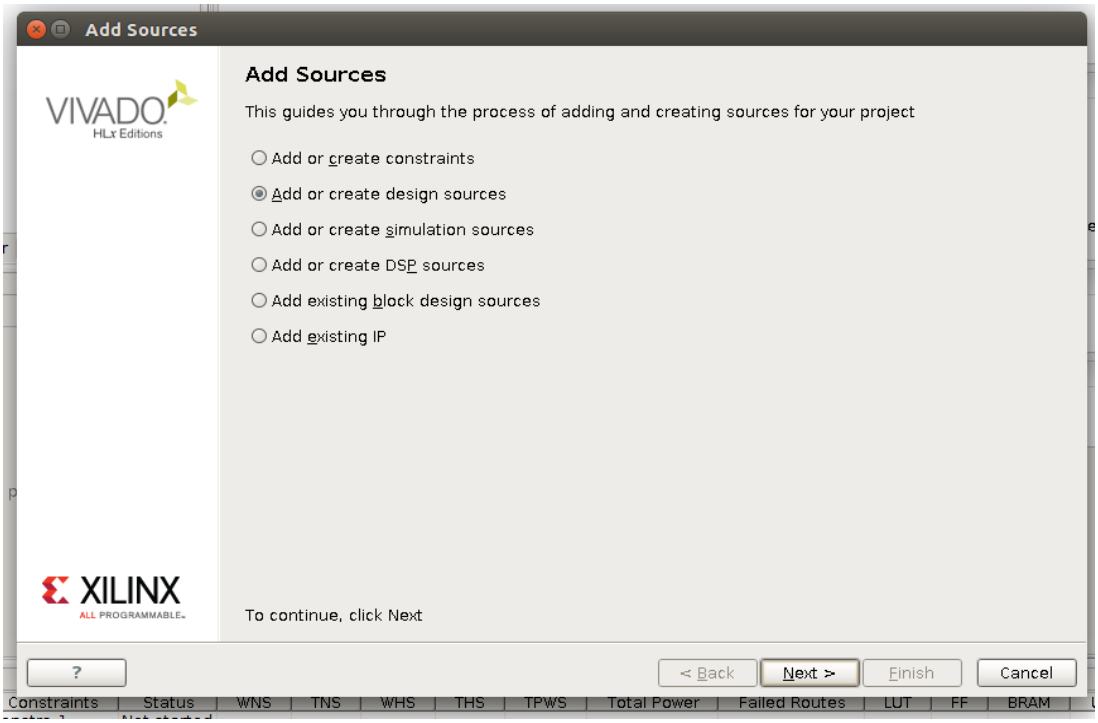
1. Open vivado (type command vivado in terminal).
2. Once the tool opens, click on Create New project.
3. Click Next.
4. Now select a directory for the project and a project name. (choose a relevant name, can be same as the ISE design name).
5. In the next screen, choose RTL project and enable the button “Do not specify sources at this time”.



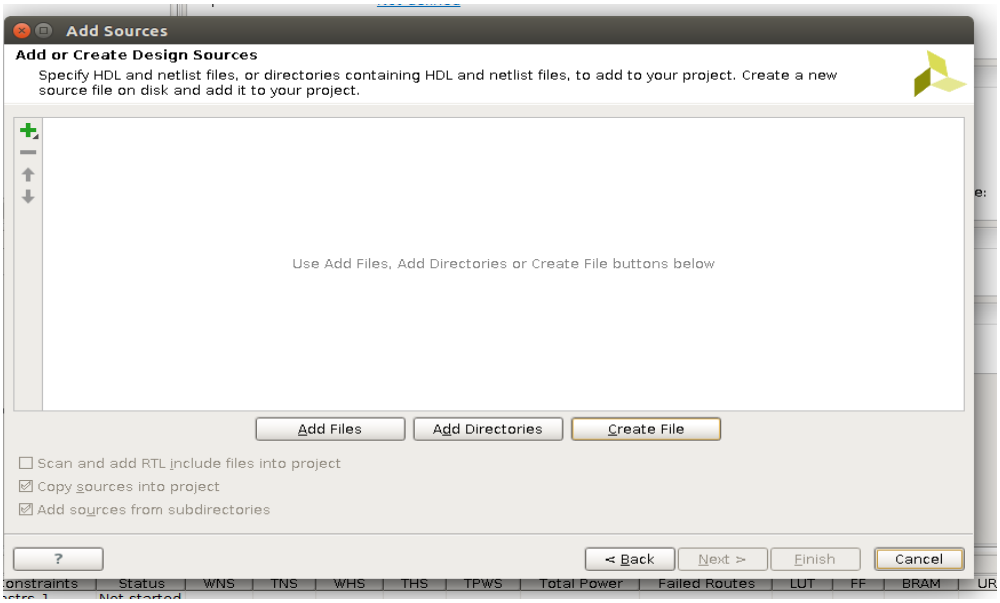
6. Click next and select the part number as xc7a35tcpg236-1 and click on next.



7. Click on Finish. The project is created.
8. Now we need to add sources. On the left pane, click on Add sources under project manager tab. Then click on “add or create design sources”

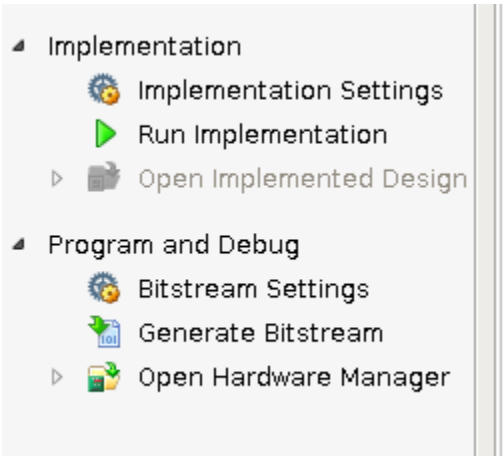


9. Click next and then on add files. Browse to add the vhdl file generated from ise schematic design. Enable the “copy sources into project” checkbox. Click on Finish.



10. Similarly, add the constraints file (*.xdc file) that is provided to you by clicking on add design sources --> add or create constraints.

11. Click on generate bitstream in the left pane in the program and debug tab.



12. Once the process is complete, click on Open hardware manager → open target → Auto connect. Make sure that the basys board is ON.
13. Once this is over, you will see a link to program device. Click on it and check that the bit file path is correct. Click on program.
14. Now you can toggle switches on the board to ensure that your design works correctly on the board.