Arithmetic in VHDL

VHDL supports arithmetic operations on data of INTEGER type, but it is preferable to use the types UNSIGNED and SIGNED with well-defined sizes. These are basically arrays of STD_LOGIC supporting arithmetic operations and are defined in packages std_logic_unsigned and std_logic_signed, respectively. Refer to sections A.2.5 to A.2.8 of Appendix A in the text book. For using these packages, you need to include the following statements in the beginning of your design.

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_unsigned.all;
USE ieee.std_logic_signed.all;
```

Alternatively, you can use the package numeric_std which defines both UNSIGNED and SIGNED. For this, you can write the following statements.

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.numeric_std.all;
```

For more information on numeric_std package, refer to the document “IEEE Standard VHDL Synthesis Packages”.