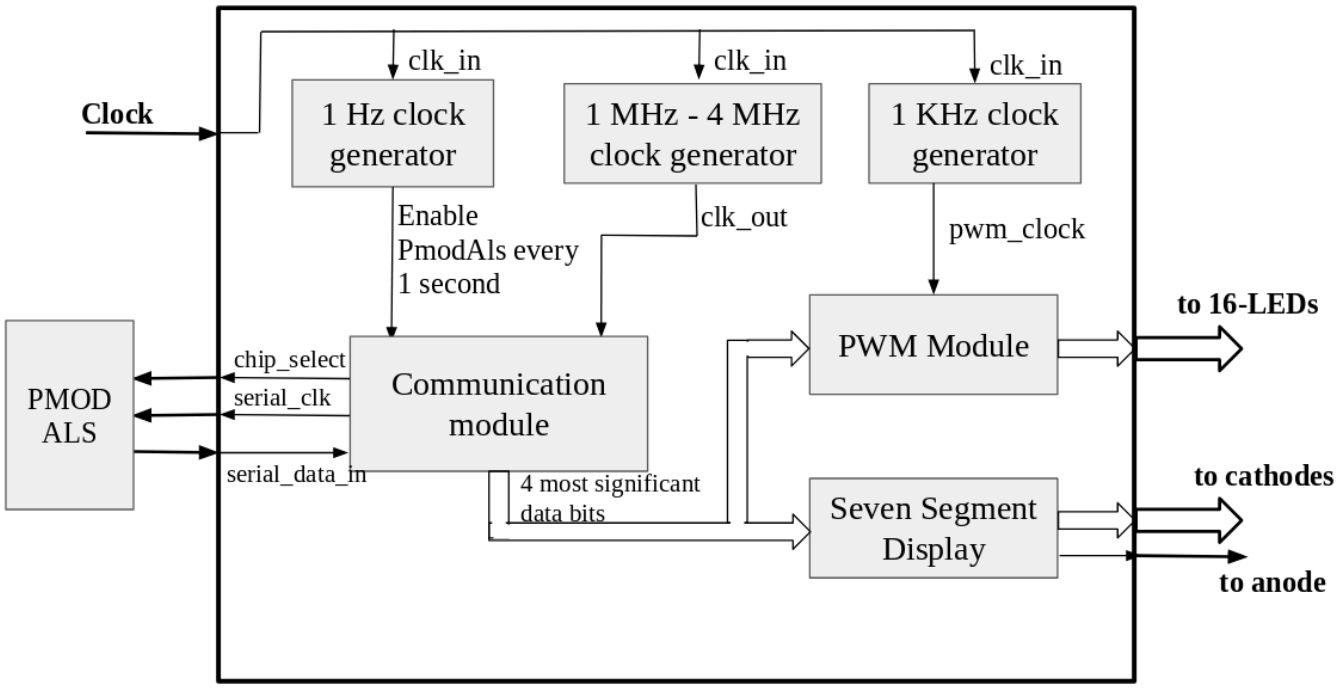
Help Document

Lab Assignment 7

Title: Smart Brightness

Block Diagram :



Note :

1. Brightness level to be displayed should be taken from the data coming from PMOD module.
2. When Chip_select (CS) of PMOD ALS is high, then Serial_clk (SCLK) also should be high as shown in waveform.
3. Request data read from PMOD ALS every 1HZ.
4. Frequency of SCLK should be between 1 MHz and 4 Mhz. Once the 15 SCLK cycles are over, CS and SCLK should be made high till next data read request.
5. During the duration for which CS is high, display brightness of read data.

Code Snippet :

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity <lab_6> is
port( clk : in std_logic;
        chip_select : out std_logic;
        -----      );
end <lab_6>;
```

```
architecture Behavioral of <lab_6> is
<signal declarations>
begin

-- 1 Hz Clock generation
   process(---,---,   )
   begin
    ------
   end process;

-- 1 KHZ Clock generation
   process(---,---,   )
   begin
    ------
   end process;

-- 1 MHZ - 4MHZ Clock generation
   process(---,---,   )
   begin
   ------
   end process;

-- SPI Communication
   process(---,---,   )
   begin
   ------
   end process;

-- PWM
   process(---,---,   )
   begin
    ------
   end process;

-- 7 Segment digit display
   process(---,---,   )
   begin
    ------
   end process;

       •

       •

       •
end Behavioral;
```