Lab Assignment 3

Title: Seven-segment Display Logic

Learning Objective:

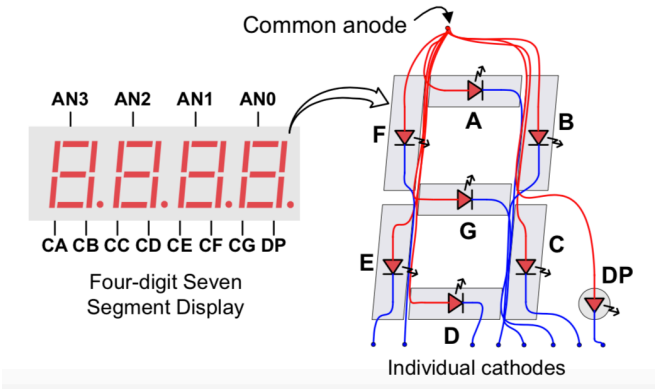
The objective of this assignment is to learn how to display decimal/hexadecimal digits using 7-segment displays. The logic designed in this assignment will be useful for subsequent assignments.

Specification:

Design a combination circuit that takes a decimal/hexadecimal digit encoded using 4 bits and produces 7-bit output for seven segment displays of BASYS3 FPGA board. Do extensive simulation of the design using Xilinx simulator, and then implement the circuit on BASYS-3 FPGA board.

Details:

The figure below shows a 7-segment display circuit of BASYS3 boards. There are four displays as shown. Each of these four consists of 7 LEDs (Light Emitting Diodes) forming 7 segments. These diodes have a common anode and individual cathodes. To display a digit, it is required to give a '1' as input to the anode and a '0' or '1' to each segment depending upon whether that segment needs to be lighted ('0') or not ('1').



Please refer to slides 24 – 30 of Lecture 4 (30.07.2019). The circuit to be designed will have 4 inputs and 7 outputs as shown in slide 28. The patterns to be displayed for various inputs are shown in slide 27. Any design style may be used, including those shown in slides 29 and 30. The 4 inputs will come from slide switches and 7 outputs will go to the cathodes of the 7-segment displays. You need to consider another 4 outputs going to the anodes of the 7-segment displays. On these 4, constant values (3 zeroes and a one) are to be output.

This assignment focuses on a single digit display. In a later assignment we will deal with all four displays and produce anode signals to control which digit(s) need to be displayed.