Lab Assignment 4

Title: 4-Digit Seven-segment Display

Learning Objective:

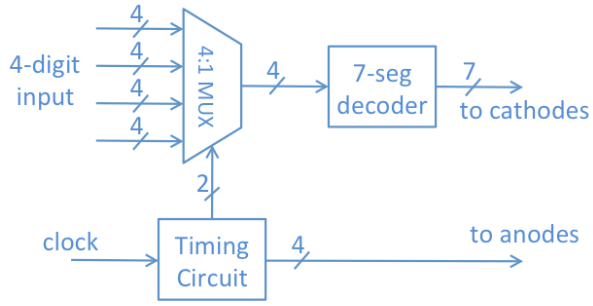
Learn how to use on-board clock and generate timing/refreshing signals.

Specification:

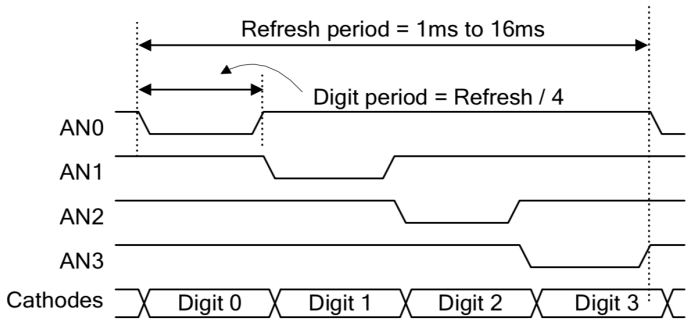
Design and implement a circuit that takes a 4-digit decimal/hexadecimal number from slide switches and displays it on seven segment displays of BASYS3 FPGA board. Use on-board clock and find valid range of refresh rates.

Details:

This assignment builds over assignment 3, extending from a single digit display to a multi-digit display by introducing proper timing and refreshing signals. It requires addition of a 4:1 multiplexer and a timing circuit to the 7-segment decoder designed in assignment 3, as shown in the figure below. Each of the 4 inputs and the output of the multiplexer are 4 bits, representing a decimal or hexadecimal digit. The timing circuit has two roles – (a) it produces 2-bit select input for the multiplexer and (b) it produces signals for the anodes (slides 27-30 of Lecture 8 – these figures are from BASYS 3 reference manual).



Create an appropriate constraint file for connecting the circuit to on-board resources - slide switches, 7-segment displays and clock.



The range of refresh period specified here is 1 ms to 16 ms. Accordingly, the clock frequency should be in the range 250 Hz to 4KHz (4 times the refresh rate). This clock needs to be generated from the on-board 100 MHz clock by dividing it suitably. In order to practically determine the valid range of refresh rates, design a circuit for generating clocks with different frequencies. Below certain frequency the display will start flickering and above certain frequency the LEDs will not be able to switch and the display will become dim.