Tutorial for Generating VHDL file from Schematic in Xilinx

1. Once you have checked your design in simulator on various input combinations, export the design as VHDL design to be used in Vivado.
2. Click on the implementation in the left window and then expand design utilities tab.
3. Click on “View HDL functional model”.
4. Copy the content of the file displayed into a new file named as per requirement (like lift_control.vhf).
5. Save the file.
6. After this follow the Vivado Tutorial.