Mnemonic Bit positions	IIII 23:20	xWWW 19:16	R/D RRR 15:12	DDDD 11:8	xRRd/W x7:4	3:0	Comments	
LD D_N, R_M	0001	0000	0mmm	nnnn	0100	xxxx	Load data register N with contents of register M	
LD R_N,D_M	0001	xnnn	0000	mmmm	0110	xxxx	Load register N with contents of data address M	
ADD R_N,R_M	0010	xnnn	1mmm	0000	0110	xxxx	$R_N = R_M + R_N$	
SUB R_N,R_M	0011	xnnn	1mmm	0000	0110	xxxx	$R_N = R_M - R_N$	
INC R_N,	0100	xnnn	1nnnn	0000	0110	xxxx	$R_N = R_N + 1$ (INC R_N, R_M)	
DEC R_N	0101	xnnn	1nnnn	0000	0110	xxxx	$R_N = R_N - 1$	
COP R_N,R_M	0110	xnnn	1mmm	0000	0110	xxxx	$R_N = R_M$	
MUL R_N,R_M	0111	xnnn	1mmm	0000	0110	xxxx	$R_N = R_N * R_M$	
AND R_N R_M	1000	xnnn	1mmm	0000	0110	xxxx	$R_N = R_N$ bit And R_M	
XOR R_N R_M	1001	xnnn	1mmm	0000	0110	xxxx	$R_N = R_N$ bit XOR R_M	
JP	1010	QQQQ	QQQQ	0000	0010	xxxx	Jump relative to current location to Q where Q is a 2'compliment number + 127 forward, -128 back. Bits in this field are ignored for jumps	
JZ	1011	QQQQ	QQQQ	0000	0010	xxxx	Jump if Zero flag set to relative Q location	
J G	1100	QQQQ	QQQQ	0000	0010	xxxx	Jump if Greater than flag set to relative Q location	
JL	1101	QQQQ	QQQQ	0000	0010	xxxx	Jump if less flag set to relative Q location	

M and N are register numbers with legal values 0 – 7 and m and n are the bit representations of M and N. N is the destination register address, M is the source address. The xWWW column is the destination register and RRR is the source register for both register to register and data transfers. Bit 15 is his high for a register transfer and low for a data transferFor the load instruction Data to register D is source and xWWW is the destination. For load register to data RRR is the source register and D is the destination register. The column labelled DDDD is the data register address The next column consists of 4bits, R is set for any register operation, Rd/W is a single bit field for the data register that is 1 when read and 0 when written. X are unused bits and their default value should be set to 0