FPGA Implementation of Efficient Signed Multiplier Using Vedic Mathematics

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Abstract

Multipliers plays an important role in todays digital signal processing and various other applications. Multiplication is most fundamental and frequently used operation in DSP applications. This operation also form the basis for other complex operations. With ever increasing need for faster clock frequency it becomes imperative to have faster arithmetic unit. This work proposes the design of high speed Multiplier based on the techniques of Ancient Indian Vedic Mathematics that have been modified to improve performance. Vedic Mathematics is based on 16 formulas with the purpose of simplification of lengthy and cumbersome mathematics. Vedic mathematics contains multiple algorithms for one operation. For arithmetic multiplication various Vedic multiplication techniques like Urdhva tiryakbhyam, Nikhilam and Anurupye is used. It has been found that Urdhva tiryakbhyam Sutra is most efficient Sutra (Algorithm), giving minimum delay for multiplication of binary numbers, either small or large. In this work Urdhva triyakbhyam sutra is used for signed binary multiplication, and carry select adder is used for handling partial products due to which the combinational path delay reduces.

Further, the VHDL coding of Urdhva tiryakbhyam Sutra for 32x32 bits multiplication is done in Xilinx Synthesis Tool (v14.1) and simulation result for same is obtained in Modelsim simulator.

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Chapter 1

Introduction

Digital Signal Processing (DSP) is a technology that is ubiquitous in almost every engineering discipline. High speed multipliers are of extreme importance in DSP to perform convolution, Fast Fourier Transform (FFT), Discrete Fourier Transforms, Digital filters etc. Digital Image Processing, Image processing architectures and microprocessors are another field where the selection of multiplier plays an important role in deciding the performance of the system. As switching and critical computations of a multiplier are high, compared to other datapath units of a processing architecture, design of low power, high speed multipliers are carried out to reduce latency and power dissipation of a processing system [10].

The demand for high speed processing has been increasing as a result of expanding computer and signal processing applications. To achieve the desired performance in many real-time signal and image processing applications higher throughput arithmetic operations are important. Multiplication is one of the key arithmetic operation in such applications and the development of fast multiplier circuit has been a subject of interest over decades. Reducing the time delay and power consumption are very essential requirements for many applications. This work presents multiplier architecture which is based on Vedic Mathematics [4].

Minimizing power consumption for digital systems involves optimization at all levels of the design. This optimization includes the technology used to implement the digital circuits, the circuit style and topology, the architecture for implementing the circuits and at the highest level the algorithms that are being implemented. Digital multipliers are the most commonly used components in any digital circuit design. They are fast, reliable and efficient components that are utilized to implement any operation. Depending upon the arrangement of the components, there are different types of multipliers available. Particular multiplier architecture is chosen based on the application [10].

The computing system generally includes large number of multiplier blocks. The amount of circuitry involved is directly proportional to the square of its resolution i.e. A multiplier of size n bits has n^2 gates. For multiplication algorithms performed in DSP applications latency and throughput are the two major concerns from delay perspective. Latency is the real delay of computing a function, a measure of how long the inputs to a device are stable is the final result available on outputs. Throughput is the measure of how many multiplications can be performed in a given period of time; multiplier is not only a high delay block but also a major source of power dissipation. That's why if one also aims to minimize power consumption, it is of great interest to reduce the delay by using various delay optimizations.

Ancient Indian Vedic Mathematics consists of sixteen mathematical formulae reconstructed from the Atharvaveda and has been recognized as a technique for improving the mathematical skills of school students. The multiplication, squaring, cubing and finding square roots and cube roots have always been time consuming processes for man as well as machine. The Vedic Mathematics provides easy and speedy solutions for these difficult processes [1].

The proposed architecture using Ancient Indian Vedic Mathematics has the advantage that as the number of bits increases, its gate delay and area increases very slowly as compared to other multiplier architectures. It is estimated that this design is quite sufficient in terms of silicon area/speed. Such a design should enable substantial savings of resources in the FPGA when used for image and video processing applications [6].

FPGAs (Field-Programmable Gate Arrays) are integrated circuits that may be electronically programmed (in the field) to execute any type of functionality. They typically consist of programmable logic cells and interconnects. Compared to the microcontroller and DSP-integrated circuits, FPGAs have the advantage of flexibility in case of changes and they enable the reduction of the execution time of the mutiplication algorithm due to their capability to integrate digital hardware with high speed and parallel processing features.

In this work all the designs are done using VHDL language. VHDL is an acronym for VHSIC (Very High Speed Integrated Circuit) Hardware Description Language. It is intended for documenting and modeling digital systems ranging from a small chip to a large system. VHDL is used because of its portability, flexibility, and readability. The design of each block includes the following steps :

1. Understanding the functionality of the module and its sub-modules.
2. Developing VHDL codes for the top module and its sub-modules.
3. Design synthesis.
4. Mapping and Routing.
5. Test-bench waveform generation and testing.
6. Error-correction.
7. FPGA Implementation.

In this work all the designs have been implemented on an Spartan 6 family using the Xilinx 14.1 ISE design tool suite.

1.1 Objective

The main objective of this work is to design and implement of a fast and efficient Signed multiplier based on Vedic maths. This vedic multiplier works for signed binary numbers. This work uses an iterative vedic multiplication method named Urdhva Triyakbhyam which means vertically and crosswise algorithm. Multiplication is done by Urdhva Triyakbhyam method and partial product addition is achieved by ripple carry adder (RCA) and carry select adder (CSeA) and their performane is compared proving CSeA is better in terms of delay.

1.2 Tools Used

Software used : Xilinx ISE 14.1 has been used for synthesis and Modelsim 10.4 has been used for simulation.
Hardware used : Xilinx Spartan 6 (Family), XC6SLX150T (Device), FGG90 (Package), -2 (Speed Grade) FPGA devices.

This report is organized as follows:

The basic concept of multiplication and need of multiplication in various fields is discussed in chapter 1. Chapter 2 discusses literature survey of multipliers. chapter 3 discusses introduction of Vedic mathematics and algorithms available for Multiplication in vedic mathematics. chapter 4 focuses on conventional method of multiplication and vedic multiplier. chapter 5 deals with architechture of signed multiplier. Synthesis and Simulation result is given in chapter 6. Chapter 7 presents the conclusion and future work.

Chapter 2

Literature Survey

Two most common multiplication algorithms followed in the digital hardware are array multiplication algorithm and Booth multiplication algorithm. In an array multiplier multiplication of two binary numbers can be obtained with one micro-operation by using a combinational circuit that forms the product bits all at once thus making it a fast way of multiplying two numbers since the only delay is the time for the signals to propagate through the gates that form the multiplication array. However, an array multiplier requires a large no gates and for this reason it is less economical [4].

Booth algorithm is another powerful algorithm for multiplication. This algorithm is a method that will reduce the number of multiplicand multiples. For a given range of numbers to be represented, a higher representation radix leads to fewer digits. Since a k bit binary number can be interpreted as k/2 digit radix 4 number, a k/3 digit radix 8 number and so on it can deal with more than one bit of the multiplier in each cycle by using high radix multiplication. Most of the multiplication algorithms for high speed implementation are based on Booth encoding algorithm and its modifications [2].

In [3] an algorithm for high-speed, two's complement, m-bit by n-bit parallel array multiplication is described. The two's complement multiplication is converted to an equivalent parallel array addition problem in which each partial product bit is the AND of a multiplier bit and a multiplicand bit, and the signs of all the partial product bits are positive. Main disadvantage of this algorithm was the need for the complements of each multiplier and multiplicand bit in forming the partial products bits.

Many have proposed the use of Vedic mathematics methods for multiplication of unsigned binary numbers. In [6] a NxN bit parallel overlay multiplier architecture for high speed DSP operations is proposed. The architecture is based on the Urdhva Tiryakbhyam the Vertical and Crosswise algorithm of Vedic Mathematics. The whole multiplication operation is decomposed into 4 x 4 bit multiplication modules. The 4 x 4 multiplication modules are implemented using array and booth multipliers and a considerable improvement in the speed is achieved.

A new multiplier and square architecture is proposed in [4], based on the algorithm of Ancient Indian Vedic Mathematics, for low power and high speed applications. It is based on generating all partial products and their sums in single step. It has been shown that as the number of bits in the multiplier increases the Vedic Multiplier has superior scalability over conventional multiplier methods. Similarly for the square architecture the gate delay and area reduces by 50 percentage [4].

In [5] design and implementation of a novel high speed signed multiplier based on vedic mathematics is proposed. In which multiplication is done by vedic multiplier and

partial product addition is done by ripple carry adder.

Thus many attempts have been reported in literature about improvement in multipliers that have the least number of gate delays and consume the least amount of chip area. So there is a need for an improved multiplier architecture that has the simple design advantages, but which does not suffer the excessive delays associated with conventional multiplier structures. This work presents a signed multiplier architecture based on the ancient Indian Vedic mathematics [1] sutra (formula) called Urdhva Tiryakbhyam (Vertically and Cross wise) which is traditionally used for decimal system in ancient India. The designs of the multiplier is considerably faster than existing multipliers reported previously in the literature. It is demonstrated that this design is quite efficient in terms of speed.

Chapter 3

Vedic Mathematics

The word Veda has this derivational meaning i.e. the fountain head and unlimited storehouse of all knowledge. Vedic mathematics shows its application in fast calculations for multiplication, division, squaring, cubing, square root, cube root, trigonometry, log and exponential. The basic sutras and upa sutras in the Vedic Mathematics helps to do almost all the numeric computations in easy and fast manner. The ancient Indian Vedic mathematics is now currently employed in our global silicon chip technology for easier and faster calculations.

Vedic mathematics is part of four Vedas (books of wisdom). It is part of Sthapatya-Veda (book on civil engineering and architecture), which is an upa-veda (supplement) of Atharva Veda. It covers explanation of several modern mathematical terms including arithmetic, geometry (plane, co-ordinate), trigonometry, quadratic equations, factorization and even calculus [1].

His Holiness Jagadguru Shankaracharya Bharati Krishna Teerthaji Maharaja (1884-1960) comprised all this work together and gave its mathematical explanation while discussing it for various applications. Swamiji constructed 16 sutras (formulae) and 13 Upa sutras (sub formulae) after extensive research in Atharva Veda. Obviously these formulae are not to be found in present text of Atharva Veda because these formulae were constructed by Swamiji himself. Vedic mathematics is not only a mathematical wonder but also it is logical, due to which Vedic mathematics has such a degree of eminence which cannot be disapproved. Having these phenomenal characteristic, Vedic mathematics has already crossed the boundaries of India and has become a leading topic of research in abroad. VM deals with several basic as well as complex mathematical operations. Especially, methods of basic arithmetic are extremely simple and powerful.

Entire mechanics of Vedic mathematics is based on 16 sutras formulas and 13 upsutras meaning corollaries which are enlisted below.
Sutras

1. Ekadhikena Purvena
2. Nikhilam Navatascharamam Dashatah
3. Urdhva-tiryagbhyam
4. Paravartya Yojayet
5. Shunyam Samyasamucchaye

6. Anurupye Sunyamanyat
7. Sankalana vyavakalanabhyam
8. Puranaprranabhyam
9. Calana Kalanabhyam
10. Yavadunam
11. Vyastisamashtih
12. Sheshanynkena Charmena
13. Sopantyadvayamantyam
14. Ekanyunena Purvena
15. Ginitasamucchayah
16. Gunaksamucchayah

Up-sutras

1. Anurupyena
2. Shishyate Sheshsamjnah
3. Adyamadye Nantyamantyena
4. Kevalaih Saptakam Gunyat
5. Vestanam
6. Yavadunam Tavadunam
7. Yavadunam Tavadunikutya Varganka ch Yojayet
8. Antyayordhshakepi
9. Antyatoreva
10. Samucchayagunitah
11. Lopanasthapanabhyam
12. Vilokanam
13. Gunitasamucchyah Samucchayagunitah

These methods and ideas can be directly applied to trigonometry, plain and spherical geometry, conics, calculus (both differential and integral), and applied mathematics of various kinds. As mentioned earlier, all these Sutras were reconstructed from ancient Vedic texts early in the last century.

The beauty of Vedic mathematics lies in the fact that it reduces the otherwise cumbersome-looking calculations in conventional mathematics to a very simple one. This is so because the Vedic formulae are claimed to be based on the natural principles on which the human mind works. This is a very interesting field and presents some effective algorithms which can be applied to various branches of engineering such as computing and digital signal processing.

3.1 Vedic Multiplication

The proposed Vedic multiplier is based on the Vedic multiplication formulae (Sutras). These Sutras have been traditionally used for the multiplication of two numbers in the decimal number system. In this work, we apply the same ideas to the binary number system to make the proposed algorithm compatible with the digital hardware. In Vedic mathematics there are 3 methods to implement multiplication. Out of three there is one generic method which can be applied to all cases whereas other two are for special cases which are simpler to deal with. Main algorithm of vedic multiplication is discussed below :

3.1.1 Urdhva triyakbhyam Sutra

Urdhva tiryakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. It literally means Vertically and Crosswise. These Sutras have been traditionally used for the multiplication of two numbers in the decimal number system. In this work, we apply the same ideas to the binary number system to make the proposed algorithm compatible with the digital hardware. It is based on a novel concept through which the generation of all partial products can be done with the concurrent addition of these partial products. The algorithm can be generalized for n x n bit number. Since the partial products and their sums are calculated in parallel, the multiplier is independent of the clock frequency of the processor. The Multiplier based on this sutra has the advantage that as the number of bits increases, gate delay and area increases very slowly as compared to other conventional multipliers. The 4x4 multiplication using urdhva triyakbhyam is shown in Figure 3.1 and 3.2.

Figure 3.1: 4x4 Multiplication method of Urdhva-Tiryakbhyam [8].

Figure 3.2: Equations used for designing a 4x4 Vedic-Multiplier [8].

1	2
3	4

Bibliography

[1] V. Jagadguru Swami Sri Bharati Krishna Tirthji Maharaja, "Vedic Mathematics", Motilal Banarsidas, Varanasi, India, 1986.

[2] Booth A.D., "A Signed Binary Multiplication Algorithm", *Quarterly Journal of Mechanics and Applied Mathematics*, Vol. 4, June, pp. 236-240, 1951.

[3] Baugh, Charles R., Wooley, B.A., "A Two's Complement Parallel Array Multiplication Algorithm,", *Computers, IEEE Transactions on* , Vol.C-22, No.12, December, pp. 1045-1047, 1973.

[4] Thapliyal H. and Arabnia H.R., "A Time- Area - Power Efficient Multiplier and Square Architecture Based on Ancient Indian Vedic Mathematics", *Proceedings of International Conference on VLSI 04, Las Vegas, U.S.A.*, 2004.

[5] Paldurai K, K. Hariharan, "Implementation of Signed Vedic Multiplier Targeted at FPGA Architectures", *ARPN Journal of Engineering and Applied Sciences*, Vol.10, No.5, March, pp. 2193-2197, 2015.

[6] Himanshu Thapliyal and M.B. Srinivas, "High Speed Efficient N X N Bit Parallel Hierarchical Overlay Multiplier Architecture Based On Ancient Indian Vedic Mathematics", *Transactions On Engineering, Computing And Technology*, Vol.2, December, pp. 225-228, 2004.

[7] Shamim Akhter, "VHDL Implementation Of Fast NxN Multiplier Based On Vedic Mathematic", *18th European Conference on Circuit Theory and Design 2007. ECCTD 2007*, August, pp. 472-475, 2007.

[8] S R Panigrahi, O P Das, B B Tripathy, T K Dey , "FPGA Implementation of a 44 Vedic Multiplier", *International Journal of Engineering Research and Development*, Vol.7, No.1, May, pp. 76-80, 2013.

[9] R.Priya and J.Senthil Kumar, "Implementation and Comparison of Vedic Multiplier using Area Efficient CSLA Architectures", *International Journal of Computer Applications (0975 8887)*, Vol.73, No.10, July, 2013.

[10] Mr.Swaroop A. Gandewar, Prof.Mamta Sarde, "Vedic Multiplier For High Speed Computation Using Vhdl", *Journal of Research in Electrical and Electronics Engineering (ISTP-JREEE)*, Vol. 3, No.2, March, pp. 13-16, 2014.

[11] Padma Devi, Ashima Girdher and Balwinder Singh, "Improved Carry Select Adder with Reduced Area and Low Power Consumption", *International Journal of Computer Applications (0975 8887)*, Vol.3, No.4, June, pp. 14-18, 2010.

[12] http://www.aoki.ecei.tohoku.ac.jp/arith/mg/algorithm.html.

[13] http://en.wikipedia.org/wiki/Carry-select-adder.