### **Router Construction**

#### Outline

**Switched Fabrics** 

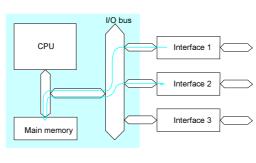
**IP Routers** 

Extensible (Active) Routers

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### Workstation-Based

- Aggregate bandwidth
  - 1/2 of the I/O bus bandwidth
  - capacity shared among all hosts connected to switch
  - example: 800Mbps bus can support 8 T3 ports
- Packets-per-second
  - must be able to switch small packets
  - 100,000 packets-persecond is achievable
  - e.g., 64-byte packets implies 51.2Mbps



2

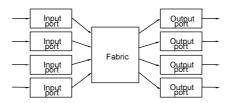
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## Switching Hardware

- Design Goals
  - throughput (depends on traffic model)
  - scalability (a function of n)

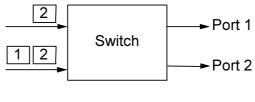


- Ports
  - circuit management (e.g., map VCIs, route datagrams)
  - buffering (input and/or output)
- Fabric
  - as simple as possible
  - sometimes do buffering (internal)

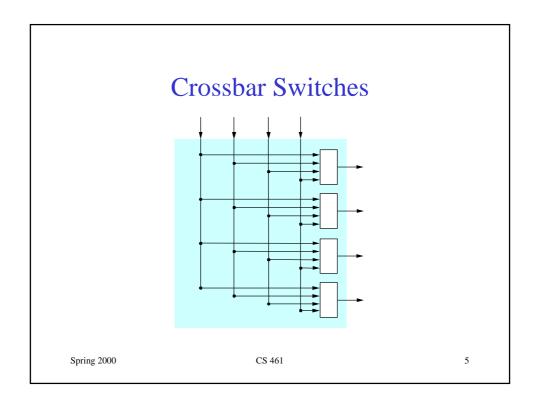
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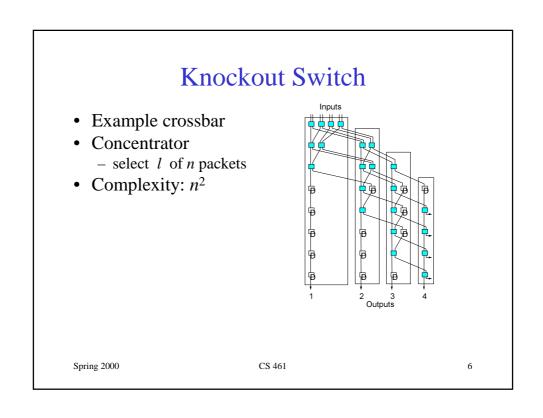
## **Buffering**

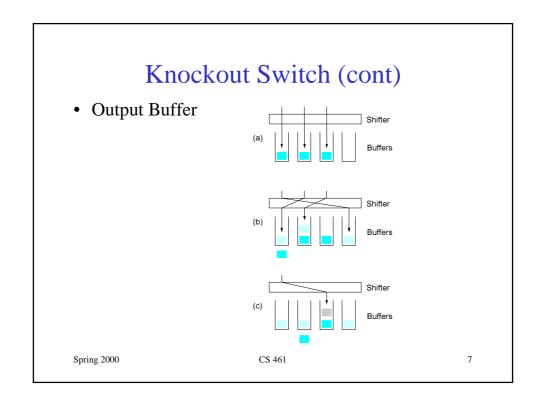
- Wherever contention is possible
  - input port (contend for fabric)
  - internal (contend for output port)
  - output port (contend for link)
- Head-of-Line Blocking
  - input buffering

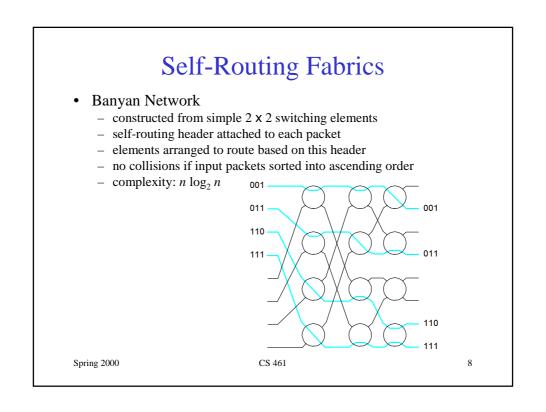


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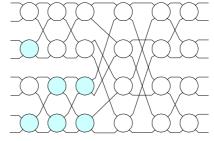






# Self-Routing Fabrics (cont)

- · Batcher Network
  - switching elements sort two numbers
    - some elements sort into ascending (clear)
    - some elements sort into descending (shaded)
  - elements arranged to implement merge sort
  - complexity:  $n \log^2_2 n$



• Common Design: Batcher-Banyan Switch

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## **High-Speed IP Router**

- Switch
- Line Cards + Forwarding Engines
  - link interface
  - router lookup (input)
  - common IP path (input)
  - packet queue (output)
- Network Processor
  - routing protocol(s)
  - exceptional cases

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