DEEKSHA DANGWAL

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RESEARCH SUMMARY

I work in computer architecture, and I am interested in understanding and characterizing program behavior through novel and efficient profiling methods. Currently, I am exploring synthetic trace generation with the intent of minimizing information leakage to promote safe program behavior sharing. Previously, I have worked on PyRTL, a Python-based RTL specification language, and built an AES-128 core and the OpenTPU on it. I have also worked on Charm, a high-level architecture modeling language.

EDUCATION

University of California, Santa Barbara, Santa Barbara, CA
Doctor of Philosophy, Computer Science — Expected Graduation: 2021
Coursework:
Computer architecture; applied cryptography;
runtime systems; operating systems; formal methods

University of California, Santa Barbara, Santa Barbara, CA
Master of Science, Electrical and Computer Engineering — Graduation: 2016
Coursework:
Computer architecture; mobile embedded systems; VLSI validation;
neuromorphic computing; parallel architectures; computer arithmetic
image processing; signal compression; matrix analysis

M.S. Ramaiah Institute of Technology, Bangalore, India
Bachelor of Engineering, Instrumentation Technology — Graduation: 2014

EXPERIENCE

Graduate Student Researcher, UCSB ArchLab — June 2015-Present
Advised by Prof. Timothy Sherwood
- Safe Program Behaviour Sharing
- Charm
- Neural-inspired approximate computing
- Evaluating architectures for cryptographic algorithms
- PyRTL

Research Intern, Microsoft, Redmond, WA — June-September 2018
Mentored by Eric Chung, Silicon Systems Futures
- Implemented parameterizable architecture-aware machine learning graph primitives for custom hardware instructions
- Wrote tools to automatically convert hardware instructions to high-level graph primitives for machine learning models that remain true-to-hardware
- Designed computational experiments to compare and verify accuracy of neural network models

Research Assistant, Oracle Labs, Austin, TX — June-September 2016
- Setup environment for measuring throughput of RAPID InfiniBand chips for ARM and x86 architectures
- Implemented network congestion tests for best/worst case traffic conditions

Teaching Assistant, Department of Physics, UCSB — January-June 2015
- PHYS 6AL, PHYS 6BL, Experimental Physics

Grader, Department of Physics, UCSB — September-December 2014
- PHYS 132, Stellar structures and evolution

PUBLICATIONS

Safer Program Behavior Sharing through Trace Wringing *(To appear)*
D. Dangwal, *W. Cui, J. McMahan, T. Sherwood. Proceedings of the 24th ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), 2019.*

Charm: A Language for Closed-form High-level Architecture Modeling
W. Cui, Y. Ding, **D. Dangwal**, *A. Holmes, J. McMahan, A. JavadiAbhari, G. Tzimpragos, F. Chong, T. Sherwood. Proceedings of the 45th International Symposium on Computer Architecture (ISCA), 2018.*

A Pythonic Approach for Rapid Hardware Prototyping and Instrumentation
J. Clow, G. Tzimpragos, **D. Dangwal**, *S. Guo, J. McMahan, and T. Sherwood. Proceedings of the International Conference on Field-Programmable Logic and Applications (FPL), September 2017. Ghent, Belgium.*

POSTERS AND PRESENTATIONS

PyRTL: Hardware design for the masses
D. Dangwal, *J. Clow, G. Tzimpragos, J. McMahan, S. Guo, and T. Sherwood. Career Workshop for Women and Minorities in Computer Architecture (CWWMCA), November 2017. Cambridge, MA. (Poster and Presentation)*

Novel Neural Computing Architectures
D. Dangwal, *A. Rajagopal, T. Sherwood. CRA-W Grad Cohort Poster Session, Washington, D.C., April 2017. (Poster)*

SELECTED PROJECTS

Safe Program Behavior Sharing *(in submission)*
Sharing program traces between vendors makes co-optimization of systems possible, but these traces can contain arbitrary amount of sensitive information. We present a synthetic trace generation pipeline for memory access traces which eliminates sensitive data and transmits only important program behaviors, thereby bounding the amount of information leaked.

Charm *June 2018*
An open-source modeling language to express architectural relationships and declare analysis goals which combined symbolic manipulation, constraint solving, and compiler techniques. Charm bridges the gap between mathematical equations and executable, optimized evaluation functions and analysis procedures.
More details: https://github.com/UCSBarchlab/Charm

OpenTPU *June 2017*
An open-source, parameterizable re-implementation of Google's Tensor Processing Unit (TPU), in PyRTL. We designed a simple ISA, a functional simulator and a hardware simulator in PyRTL.
More details: https://github.com/UCSBarchlab/OpenTPU

Trace Compression with Autoencoders *June 2017*
Designed a lossy compression algorithm for memory address traces using unsupervised neural network structures called autoencoders. The encoder and decoder are neural networks with trained parameters and can be stored on separate encoding and decoding devices as JSON files.

Evaluating Architectural Options for Proof-of-Work Cryptographic functions *March 2017*
We present guidelines for cryptographic hash function algorithms to ensure difficulty in bypassing proof-of-work criteria by designing custom hardware accelerators.

Unix File System *December 2016*
Implemented a file system (written in C++) with FUSE for CentOS. This project involved the abstraction of disk layer, inode management, and system call implementations.

Hardware implementation of AES *September 2015*
Design of AES-128 accelerator core which performs encryption and decryption. This was implemented and simulated in PyRTL to demonstrate programmer productivity, code simplicity and compaction achieved with PyRTL.

Multilevel Snoopy Cache Design for Multiprocessor System *December 2014*
Hardware implementation of of 4-way set-associative snoopy cache implemented for a 4-processor system with private L1 caches, 2-processor-shared L2 caches and main memory. Designed in Verilog with simulation in ModelSim.

Superscalar Instruction Dispatch Unit (Tomasulos algorithm) *December 2014*
Hardware implementation of dual dispatch superscalar processor with 8-deep

instruction queue, register renaming and exception handling. Designed in Verilog and simulated in ModelSim.

MENTORSHIP

Early Research Scholars Program (ERSP), *Department of Computer Science, UCSB* *2018-2019*
Mentoring 4 UCSB undergraduate students and designing a year-long project for the research apprenticeship

Women in STEM Mentorship Program, *2016-2018*

EUREKA Mentorship Program, *California NanoSystems Institute (CNSI)* *June-August 2015*
Designed research project in hardware security and mentored a UCSB undergraduate student

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LANGUAGES, ENVIRONMENTS AND DESIGN TOOLS

Python, C, C++, Verilog, MATLAB,
Valgrind, Pin, PyRTL, ModelSim, Design Compiler, Vivado, Yosys, Verilator, Icarus Verilog, TensorFlow, z3py, Android Studio

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HONORS

Second Place Winner, NXP Embedded Design Challenge *August 2015*
for the design of a "Temperature controlled switch" using LPCXpresso4337 and general-purpose shield

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PROFESSIONAL MEMBERSHIPS

Association for Computing Machinery (ACM); Association for Computing Machinery for Women in Computing (ACM-W); SIGARCH; SIGMICRO; Women in Computer Architecture (WICARCH); UCSB Women in Computer Science (WiCS)

ACTIVITIES

Co-President, Women in Computer Science (WiCS), *Department of Computer Science, UCSB* *2018-2019*

Graduate Representative for Diversity, *Department of Computer Science, UCSB* *2018-2019*

Grace Hopper Celebration of Women *October 2017, 2018*

CRA-W Grad Cohort *April 2017, 2018*

Cultivating Students' Interest in STEM, *Tech Savvy Conference, UCSB* *May 2017, April 2018*
Designed modules for and conducted workshop focused on methods young women could use to overcome biases in STEM fields

I HEART STEM Workshop, *UCSB Women's Center* *November 2016*
Conducted the "I HEART CODE" workshop introducing high school girls to Python

Make a Difference Fellowship, *Bangalore, India* *December 2012-April 2014*
Supervised operations as Center Head at the St. Patrick's Boys' Home;
Made key organizational decisions and led 250 volunteers across Bangalore;
Volunteered as an English teacher