DDCO Laboratory (UE23CS251A)

3rd Semester, Academic Year 2024-25

Date: 19/10/24 Week-6 Submission

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Implement the following using the Verilog. After each experiment attach the following.

i. Verilog Code Screenshot.

ii. Verilog VVP Output Screen Shot.

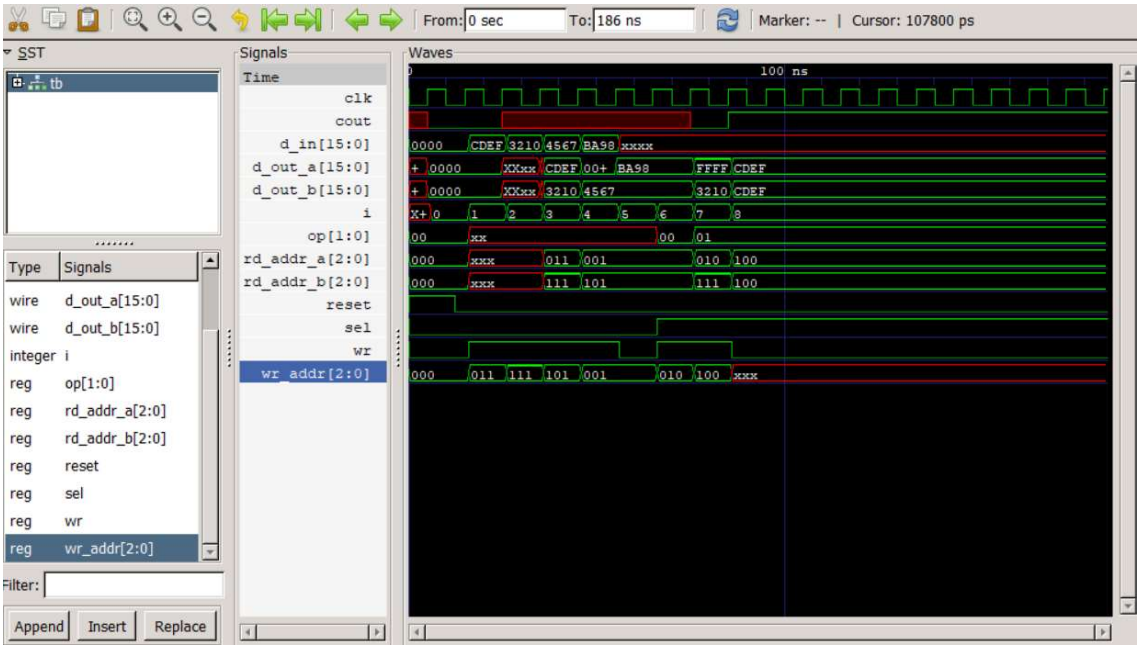
iii. GTKWAVE Screenshot.

1. ALU AND REGISTER

1_alureg.v

```
1  module reg_alu(input wire clk, reset, sel,wr,input wire [1:0] op,input wire [2:0] rd_addr_a,rd_addr_b, wr_addr,input wire [15:0] d_in, output wire [15:0] d_out_a,d_out_b, output wire cout);
2
3      wire [15:0] d_in_reg,o; wire cout_alu;
4
5      mux2_16 mux2_0(d_in,o,sel,d_in_reg);
6      reg_file rf0(clk,reset,wr,rd_addr_a,rd_addr_b,wr_addr,d_in_reg,d_out_a,d_out_b);
7      alu alu_0 (op,d_out_a,d_out_b,o,cout_alu);
8      dfr dfr_1(clk,reset,cout_alu,cout);
9  endmodule
```

```
VCD info: dumpfile tb_reg_alu.vcd opened for output.
Time=0 | sel=0, wr=0, op=00, rd_addr_a=000, rd_addr_b=000, wr_addr=000, d_in=0000, d_out_a=xxxx, d_out_b=xxxx, cout=x
Time=50 | sel=0, wr=0, op=00, rd_addr_a=000, rd_addr_b=000, wr_addr=000, d_in=0000, d_out_a=0000, d_out_b=0000, cout=0
Time=160 | sel=0, wr=1, op=xx, rd_addr_a=xxx, rd_addr_b=xxx, wr_addr=011, d_in=cdef, d_out_a=0000, d_out_b=0000, cout=0
Time=250 | sel=0, wr=1, op=xx, rd_addr_a=xxx, rd_addr_b=xxx, wr_addr=011, d_in=cdef, d_out_a=XXXx, d_out_b=XXXx, cout=x
Time=260 | sel=0, wr=1, op=xx, rd_addr_a=xxx, rd_addr_b=xxx, wr_addr=111, d_in=3210, d_out_a=XXXx, d_out_b=XXXx, cout=x
Time=350 | sel=0, wr=1, op=xx, rd_addr_a=xxx, rd_addr_b=xxx, wr_addr=111, d_in=3210, d_out_a=xxxx, d_out_b=xxxx, cout=x
Time=360 | sel=0, wr=1, op=xx, rd_addr_a=011, rd_addr_b=111, wr_addr=101, d_in=4567, d_out_a=cdef, d_out_b=3210, cout=x
Time=460 | sel=0, wr=1, op=xx, rd_addr_a=001, rd_addr_b=101, wr_addr=001, d_in=ba98, d_out_a=0000, d_out_b=4567, cout=x
Time=550 | sel=0, wr=1, op=xx, rd_addr_a=001, rd_addr_b=101, wr_addr=001, d_in=ba98, d_out_a=ba98, d_out_b=4567, cout=x
Time=560 | sel=0, wr=0, op=xx, rd_addr_a=001, rd_addr_b=101, wr_addr=001, d_in=xxxx, d_out_a=ba98, d_out_b=4567, cout=x
Time=660 | sel=1, wr=1, op=00, rd_addr_a=001, rd_addr_b=101, wr_addr=010, d_in=xxxx, d_out_a=ba98, d_out_b=4567, cout=x
Time=750 | sel=1, wr=1, op=00, rd_addr_a=001, rd_addr_b=101, wr_addr=010, d_in=xxxx, d_out_a=ba98, d_out_b=4567, cout=0
Time=760 | sel=1, wr=1, op=01, rd_addr_a=010, rd_addr_b=111, wr_addr=100, d_in=xxxx, d_out_a=ffff, d_out_b=3210, cout=0
Time=850 | sel=1, wr=1, op=01, rd_addr_a=010, rd_addr_b=111, wr_addr=100, d_in=xxxx, d_out_a=ffff, d_out_b=3210, cout=1
Time=860 | sel=1, wr=0, op=01, rd_addr_a=100, rd_addr_b=100, wr_addr=xxx, d_in=xxxx, d_out_a=cdef, d_out_b=cdef, cout=1
1_tb_reg_alu.v:55: $finish called at 1860 (100ps)
```


From: 0 sec
To: 186 ns
Marker: -- | Cursor: 107800 ps
SST
tb
Type Signals
wire d_out_a[15:0]
wire d_out_b[15:0]
integer i
reg op[1:0]
reg rd_addr_a[2:0]
reg rd_addr_b[2:0]
reg reset
reg sel
reg wr
reg wr_addr[2:0]
Filter:
Append
Insert
Replace
Signals
Time
clk
cout
d_in[15:0]
d_out_a[15:0]
d_out_b[15:0]
i
op[1:0]
rd_addr_a[2:0]
rd_addr_b[2:0]
reset
sel
wr
wr_addr[2:0]
Waves
100 ns