SAN JOSÉ STATE UNIVERSITY
CharlesW.DavidsonCollege of Engineering
DEPARTMENT OF ELECTRICAL ENGINEERING

EE271 – Advanced Digital System Design and Synthesis

Fall 2017 Optional Project Report

Topic: Design and verification of 256x8 Static RAM

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Executive Summary

This project deals with the design and verification of all memory locations of 256 x 8 static RAM. The system consists of 8-bit counter, 256 x 8 RAM and an 8-bit comparator. The counter is connected to both the address and data (IO) bus so that 0 is written in 0th location, 1 is written in 1st location,2 in 2nd location.....255 in 255th location. Then the data is read back from address 0,address1,....and compared with the counter value again in the comparator where data match or mismatch occurs.

I. GeneralProject Information

Table I.1: List of EDA Tools Used

EDA Tool Name	Company	You Used it for
Xilinx XST	Xilinx	Synthesis
Xilinx Isim	Xilinx	Simulation & test

Table I.2: Device and package details

Device name	Used with (EDA tool name)
xc6slx9-2csg324	Xilinx XST

Table I.3: List of Verilog Modules (both design and test modules)

Module Name	Ports	Short Description
Comparator	[7:0]A, [7:0]B, not_equal, equal	8-bit comparator.
Counter	[7:0]count, clock, reset,en	8-bit counter
Ram	[7:0]din, [7:0]dout, reset, clock, wr_en, rd_en, [7:0]wr_addr, [7:0]rd_addr	256 x 8 static synchronous RAM
Top	reset, clock, en, wr_en, rd_en, equal, not_equal	Top module
Top_tb	reset,clock,en,wr_en,rd_en, equal,not_equal	Top module testbench

II. Implementation Overview

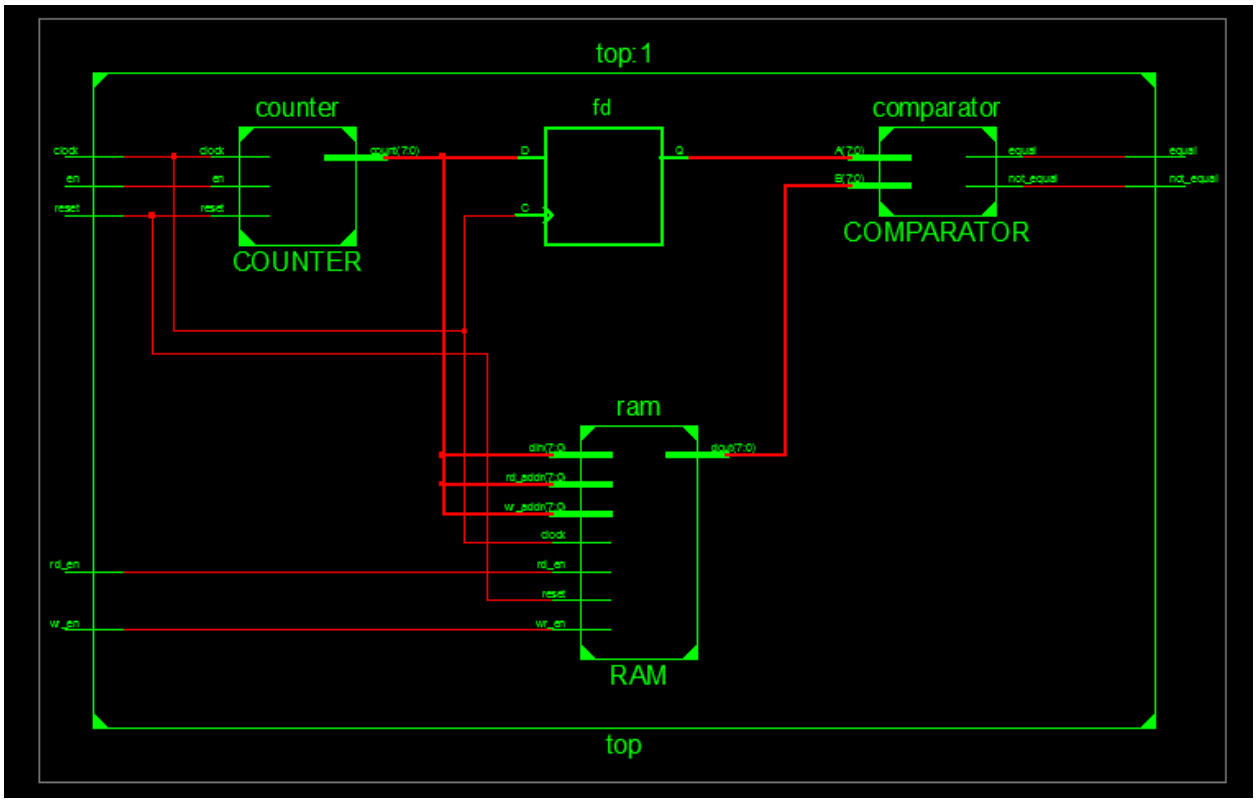

Figure II.1: Block Diagram of top

III. RTL-Level(Pre-synthesis) Simulations/Tests

Data is written into RAM in every location with 'wr_en' signal high and 'rd_en signal' low. Later when all the locations are written , 'rd_en' is made high and 'wr_en' is made low while data is compared simultaneously in the comparator.

TESTBENCH SNIPPET

```
initial
begin
     @(negedge clock);reset=1;
     repeat (254)
          begin
          @(negedge clock);en=1;wr_en=1;reset=0;
          end
     repeat(256)
     begin
          @(negedge clock);
               rd_en=1;
          wr_en=0;
     end
          @(negedge clock);
          @(negedge clock);
     #10;$finish;
end
```

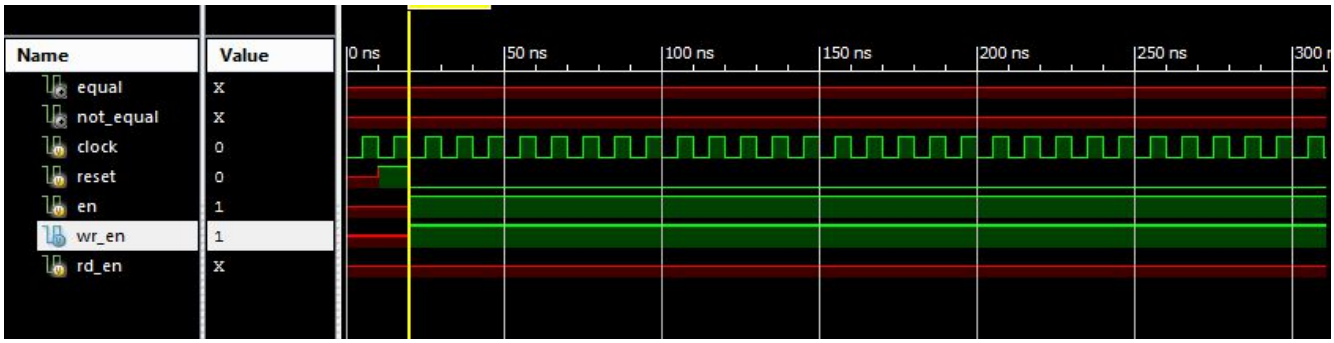

Figure III.1a:RTL simulation waveform that contains test case of write .
"*It can be noted in the waveform that the write operation is in process with wr_en high*".

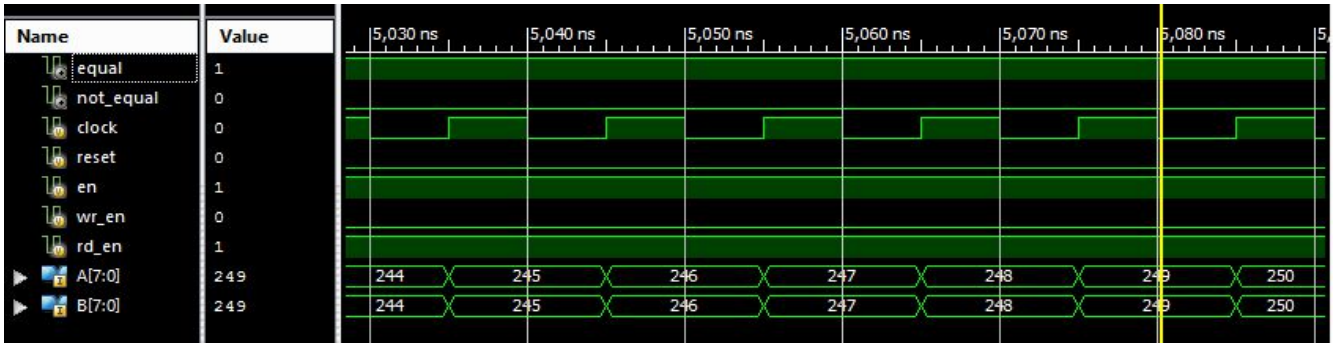

Figure III.2a:RTL simulation waveform that contains test case of read
"*It can be noted in the waveform that the read operation is in process with rd_en high and observe the inpust (A & B) of comparator and output equal* ".

IV. Conclusion

Data to all the locations of the ram where successfully written and later read while comparing the values in the comparator.

Appendix A
Completed Verilog Source Codes and Testbenches

```
module comparator (input [7:0]A,B, output not_equal,equal);

assign equal=(A==B)?1:0;
assign not_equal=(A!=B)?1:0;

/*always@(*)
begin
      $display("A=%d,B=%d",A,B);
end*/
endmodule
```

```
module counter(output reg [7:0]count, input clock,reset,en);
always@(posedge clock)
begin
      if(reset)
            count<=8'd0;
      else
      begin
            if(en)
                  count<=count+1'b1;
      end
end
endmodule
```

```
module ram(input[7:0]din,output reg [7:0]dout,input reset,clock,wr_en,rd_en,
         input [7:0]wr_addr,rd_addr);

reg [7:0]mem[255:0];  //memory declaration
integer i;

always@(posedge clock)
begin
      if(reset)
      begin
            for(i=0;i<256;i=i+1)
                  begin
                        mem[i]<=8'bx;
                  end
      end

      else
      begin
            if(wr_en)   //write_operation
                  mem[wr_addr]<=din;
            if(rd_en)         //read_operation
                  dout<=mem[rd_addr];
      end
end
endmodule
```

```
module top(input reset,clock,en,wr_en,rd_en, output equal,not_equal);
wire [7:0] w1,w3;
reg [7:0]w2;


counter COUNTER(.reset(reset),.en(en),.clock(clock),.count(w1));
ram
RAM(.rd_addr(w1),.wr_en(wr_en),.wr_addr(w1),.din(w1),.clock(clock),.reset(res
et),.dout(w3),.rd_en(rd_en));
comparator COMPARATOR(.A(w2),.B(w3),.equal(equal),.not_equal(not_equal));

always@(posedge clock)
begin
      w2<=w1;
end
endmodule
```

```
module top_tb();
reg clock,reset,en,wr_en,rd_en;
wire equal,not_equal;

top DUT(reset,clock,en,wr_en,rd_en,equal,not_equal);

always
begin
      clock=1'b0;
      #5;clock=1'b1;
      #5;
end

initial
begin
      @(negedge clock);reset=1;
      repeat (254)
            begin
            @(negedge clock);en=1;wr_en=1;reset=0;
            end
      repeat(256)
      begin
            @(negedge clock);
                  rd_en=1;
            wr_en=0;
      end
            @(negedge clock);
            @(negedge clock);
      #10;$finish;
end
endmodule
```

Appendix B
Reports EDA Tools

1.Synthesis Report

```
=========================================================================
*                      Synthesis Options Summary                        *
=========================================================================
---- Source Parameters
Input File Name                    : "top.prj"
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name                   : "top"
Output Format                      : NGC
Target Device                      : xc6slx9-2-csg324

---- Source Options
Top Module Name                    : top
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
Safe Implementation                : No
FSM Style                          : LUT
RAM Extraction                     : Yes
RAM Style                          : Auto
ROM Extraction                     : Yes
Shift Register Extraction          : YES
ROM Style                          : Auto
Resource Sharing                   : YES
Asynchronous To Synchronous        : NO
Shift Register Minimum Size        : 2
Use DSP Block                      : Auto
Automatic Register Balancing       : No

---- Target Options
LUT Combining                      : Auto
Reduce Control Sets                : Auto
Add IO Buffers                     : YES
Global Maximum Fanout              : 100000
Add Generic Clock Buffer(BUFG)     : 16
Register Duplication               : YES
Optimize Instantiated Primitives   : NO
Use Clock Enable                   : Auto
Use Synchronous Set                : Auto
Use Synchronous Reset              : Auto
Pack IO Registers into IOBs        : Auto
Equivalent register Removal        : YES

---- General Options
Optimization Goal                  : Speed
Optimization Effort                : 1
Power Reduction                    : NO
Keep Hierarchy                     : No
Netlist Hierarchy                  : As_Optimized
```

```
RTL Output                          : Yes
Global Optimization                 : AllClockNets
Read Cores                          : YES
Write Timing Constraints            : NO
Cross Clock Analysis                : NO
Hierarchy Separator                 : /
Bus Delimiter                       : <>
Case Specifier                      : Maintain
Slice Utilization Ratio             : 100
BRAM Utilization Ratio              : 100
DSP48 Utilization Ratio             : 100
Auto BRAM Packing                   : NO
Slice Utilization Ratio Delta       : 5

=========================================================================


=========================================================================
*                            HDL Parsing                                *
=========================================================================
Analyzing Verilog file "C:\Users\Pc\Desktop\project\Proj 03\ram.v" into
library work
Parsing module <ram>.
Analyzing Verilog file "C:\Users\Pc\Desktop\project\Proj 03\counter.v" into
library work
Parsing module <counter>.
Analyzing Verilog file "C:\Users\Pc\Desktop\project\Proj 03\comparator.v"
into library work
Parsing module <comparator>.
Analyzing Verilog file "C:\Users\Pc\Desktop\project\Proj 03\top.v" into
library work
Parsing module <top>.

=========================================================================
*                             HDL Elaboration                           *
=========================================================================

Elaborating module <top>.

Elaborating module <counter>.

Elaborating module <ram>.

Elaborating module <comparator>.
WARNING:HDLCompiler:413 - "C:\Users\Pc\Desktop\project\Proj 03\comparator.v"
Line 3: Result of 32-bit expression is truncated to fit in 1-bit target.
WARNING:HDLCompiler:413 - "C:\Users\Pc\Desktop\project\Proj 03\comparator.v"
Line 4: Result of 32-bit expression is truncated to fit in 1-bit target.

=========================================================================
*                            HDL Synthesis                              *
=========================================================================

Synthesizing Unit <top>.
    Related source file is "C:\Users\Pc\Desktop\project\Proj 03\top.v".
    Found 8-bit register for signal <w2>.
    Summary:
```

```
      inferred   8 D-type flip-flop(s).
Unit <top> synthesized.

Synthesizing Unit <counter>.
    Related source file is "C:\Users\Pc\Desktop\project\Proj 03\counter.v".
    Found 8-bit register for signal <count>.
    Found 8-bit adder for signal <count[7]_GND_2_o_add_1_OUT> created at line
9.
    Summary:
      inferred   1 Adder/Subtractor(s).
      inferred   8 D-type flip-flop(s).
Unit <counter> synthesized.

Synthesizing Unit <ram>.
    Related source file is "C:\Users\Pc\Desktop\project\Proj 03\ram.v".
    Found 8-bit register for signal <dout>.
    Found 2048-bit register for signal <n0268[2047:0]>.
    Found 8-bit 256-to-1 multiplexer for signal
<rd_addr[7]_mem[255][7]_wide_mux_259_OUT> created at line 22.
    Summary:
      inferred 2056 D-type flip-flop(s).
      inferred 257 Multiplexer(s).
Unit <ram> synthesized.

Synthesizing Unit <comparator>.
    Related source file is "C:\Users\Pc\Desktop\project\Proj 03\comparator.v".
    Found 8-bit comparator equal for signal <A[7]_B[7]_equal_1_o> created at
line 3
    Summary:
      inferred   1 Comparator(s).
Unit <comparator> synthesized.

=========================================================================
HDL Synthesis Report

Macro Statistics
# Adders/Subtractors                                   : 1
 8-bit adder                                           : 1
# Registers                                            : 4
 2048-bit register                                     : 1
 8-bit register                                        : 3
# Comparators                                          : 1
 8-bit comparator equal                                : 1
# Multiplexers                                         : 257
 8-bit 2-to-1 multiplexer                              : 256
 8-bit 256-to-1 multiplexer                            : 1
```

2.Timing report

```
NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
-----------------------------------+------------------------+-------+
Clock Signal                       | Clock buffer(FF name)  | Load  |
-----------------------------------+------------------------+-------+
clock                              | BUFGP                  | 352   |
-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
---------------
Speed Grade: -2

   Minimum period: 4.059ns (Maximum Frequency: 246.366MHz)
   Minimum input arrival time before clock: 5.000ns
   Maximum output required time after clock: 6.944ns
   Maximum combinational path delay: No path found

Timing Details:
---------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'clock'
  Clock period: 4.059ns (frequency: 246.366MHz)
  Total number of paths / destination ports: 4565 / 352
-------------------------------------------------------------------------
Delay:               4.059ns (Levels of Logic = 6)
  Source:            RAM/mem_0_1903 (FF)
  Destination:       RAM/dout_7 (FF)
  Source Clock:      clock rising
  Destination Clock: clock rising

  Data Path: RAM/mem_0_1903 to RAM/dout_7
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDE:C->Q             7   0.525   1.340  RAM/mem_0_1903 (RAM/mem_0_1903)
     LUT6:I1->O           1   0.254   0.000  RAM/mux2055_10_f7_12
(RAM/mux2055_10_f7_11)
     MUXF7:I1->O          1   0.175   0.000  RAM/mux2055_10_f7_1
(RAM/mux2055_10_f72)
     MUXF8:I1->O          1   0.152   0.958  RAM/mux2055_9_f8_0
(RAM/mux2055_9_f81)
     LUT6:I2->O           1   0.254   0.000  RAM/mux2055_4 (RAM/mux2055_4)
     MUXF7:I1->O          1   0.175   0.000  RAM/mux2055_3_f7
(RAM/mux2055_3_f7)
```

```
     MUXF8:I1->O           1   0.152   0.000  RAM/mux2055_2_f8
(RAM/rd_addr[7]_mem[255][7]_wide_mux_259_OUT<7>)
     FDE:D                     0.074          RAM/dout_7
    ----------------------------------------
    Total                      4.059ns (1.761ns logic, 2.298ns route)
                                       (43.4% logic, 56.6% route)

=========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'clock'
  Total number of paths / destination ports: 433 / 425
-------------------------------------------------------------------------
Offset:              5.000ns (Levels of Logic = 2)
  Source:            reset (PAD)
  Destination:       RAM/dout_7 (FF)
  Destination Clock: clock rising

  Data Path: reset to RAM/dout_7
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O            82   1.328   2.177  reset_IBUF (reset_IBUF)
     LUT2:I0->O            8   0.250   0.943  RAM/_n0535_inv1
(RAM/_n0535_inv)
     FDE:CE                    0.302          RAM/dout_0
    ----------------------------------------
    Total                      5.000ns (1.880ns logic, 3.120ns route)
                                       (37.6% logic, 62.4% route)

=========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'clock'
  Total number of paths / destination ports: 32 / 2
-------------------------------------------------------------------------
Offset:              6.944ns (Levels of Logic = 3)
  Source:            w2_1 (FF)
  Destination:       equal (PAD)
  Source Clock:      clock rising

  Data Path: w2_1 to equal
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FD:C->Q               1   0.525   1.137  w2_1 (w2_1)
     LUT6:I0->O            2   0.254   1.181  equal81 (equal8)
     LUT6:I0->O            1   0.254   0.681  equal83 (equal_OBUF)
     OBUF:I->O                 2.912          equal_OBUF (equal)
    ----------------------------------------
    Total                      6.944ns (3.945ns logic, 2.999ns route)
                                       (56.8% logic, 43.2% route)

=========================================================================
```

```
Cross Clock Domains Report:
--------------------------

Clock to Setup on destination clock clock
---------------+---------+---------+---------+---------+
               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
clock          |    4.059|         |         |         |
---------------+---------+---------+---------+---------+
```

3. Device Utilization summary

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	352	11440	3%
Number of Slice LUTs	646	5720	11%
Number of fully used LUT-FF pairs	294	704	41%
Number of bonded IOBs	7	200	3%
Number of BUFG/BUFGCTRLs	1	16	6%