EE 735: ASSIGNMENT 8

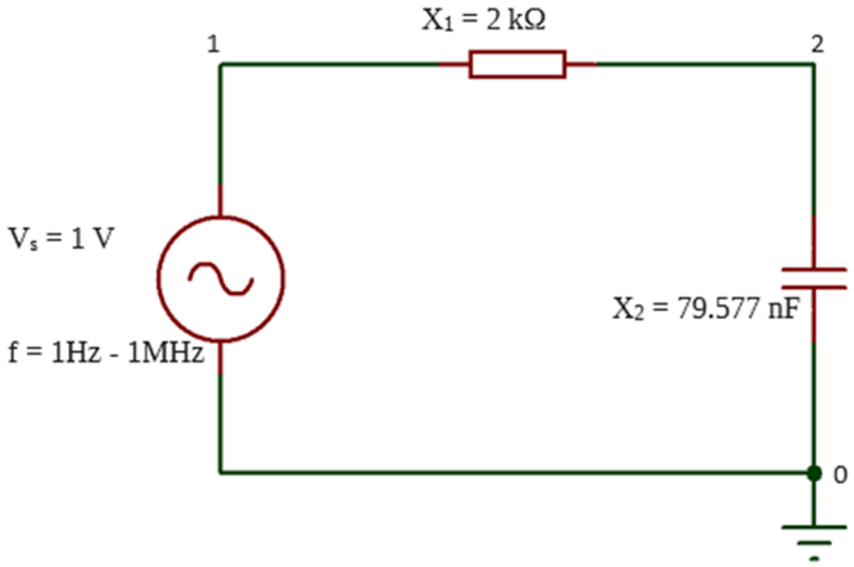
Deep Kumar Pal, 23M1135

November 3rd, 2023

QUESTION 1

Use your customized models for resistor and capacitor to design RC low pass filter with -3 dB bandwidth of 1KHz. Perform AC analysis to verify the result. Overwrite appropriate values in place of default values for Resistor and Capacitor. Draw the circuit showing V_s, X_1, X_2 and node labels.

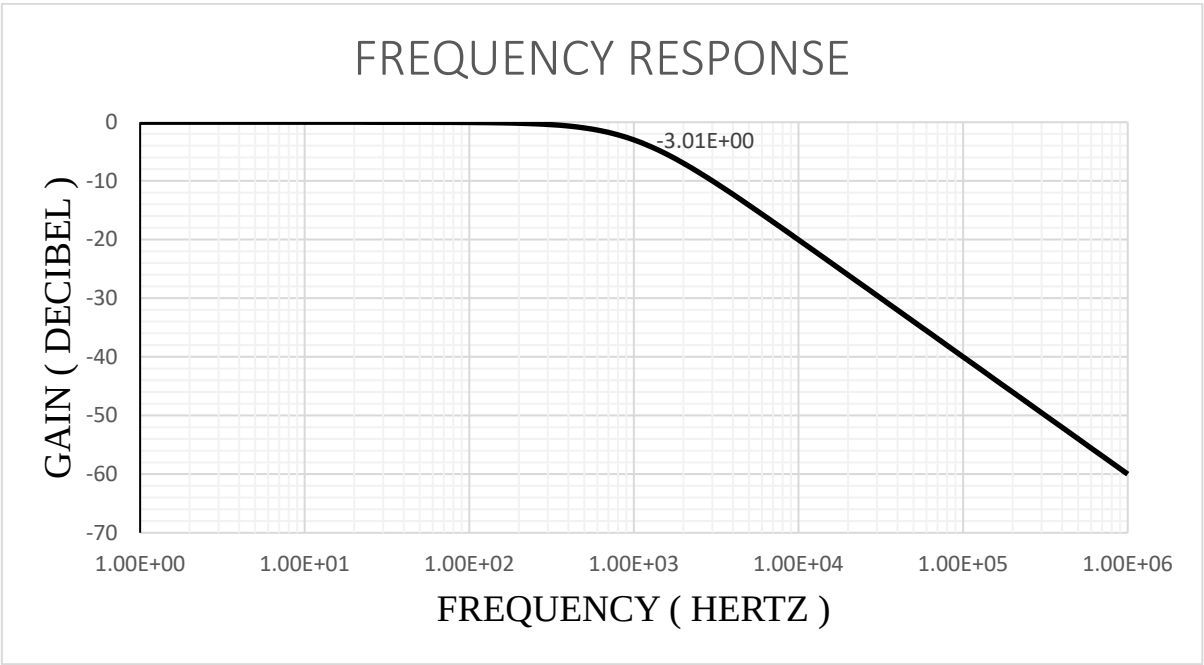
CIRCUIT



RESULT AND OBSERVATION

The value of R = 2 kΩ and C = 79.577 nF.

The frequency response is given below,

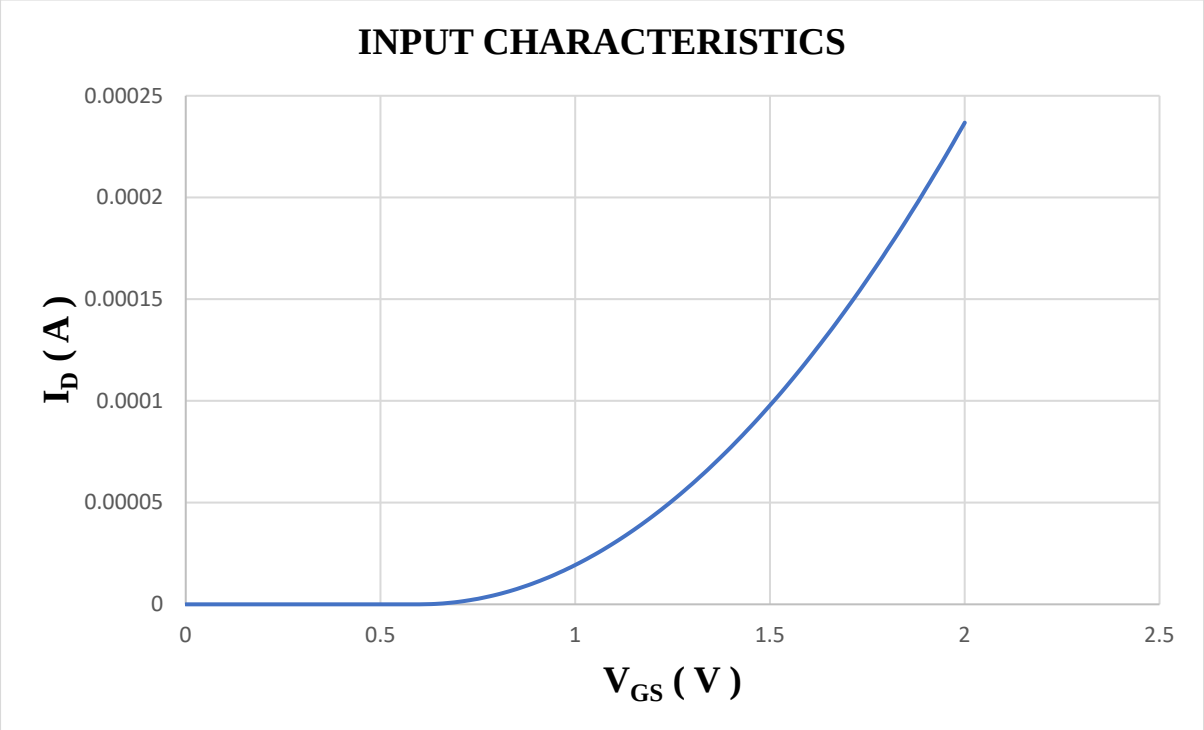


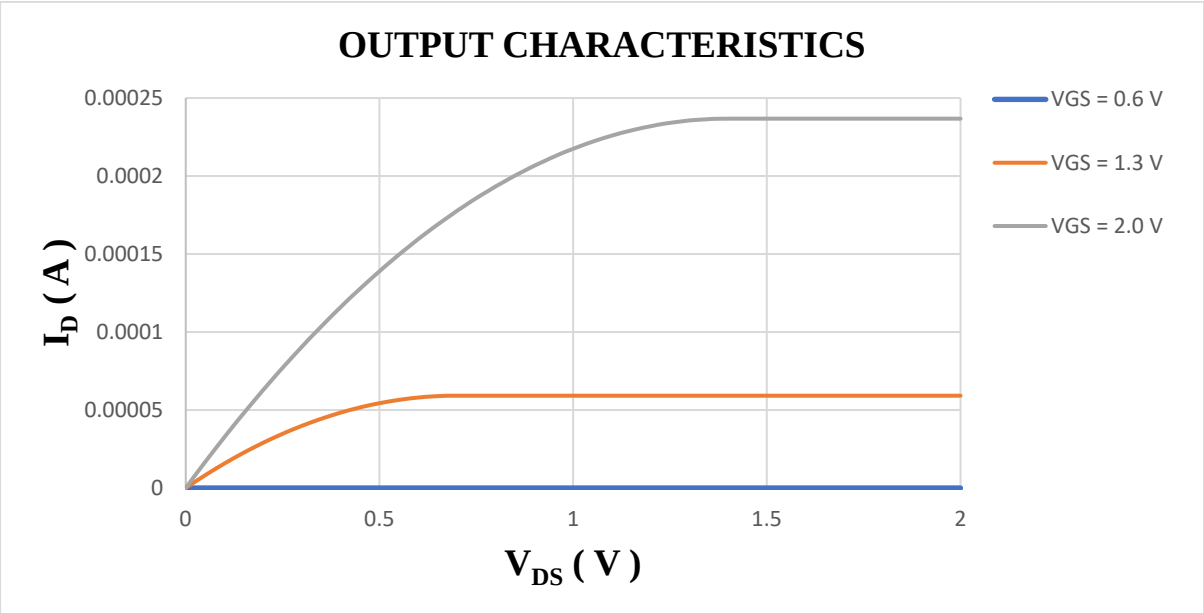
QUESTION 2

(a) Make a Verilog-A model for a simple n-channel MOSFET (NMOS) by defining current equations in linear and saturation regions. Verify by plotting INPUT and OUTPUT characteristics in HSPICE. Consider V_{th} = 0.6 V.

RESULT AND OBSERVATION

The input and output characteristics are given below,

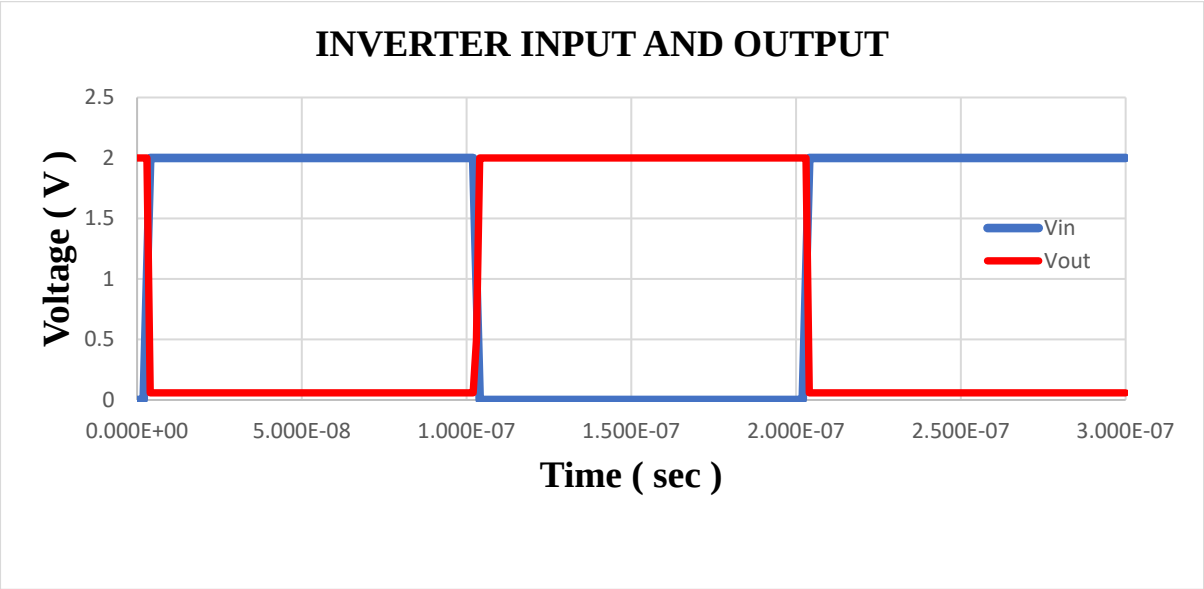




(b) Design a basic INVERTER using the NMOS and verify by applying a square pulse at Gate.

RESULT AND OBSERVATION

The input and output pulse waveforms are given below,



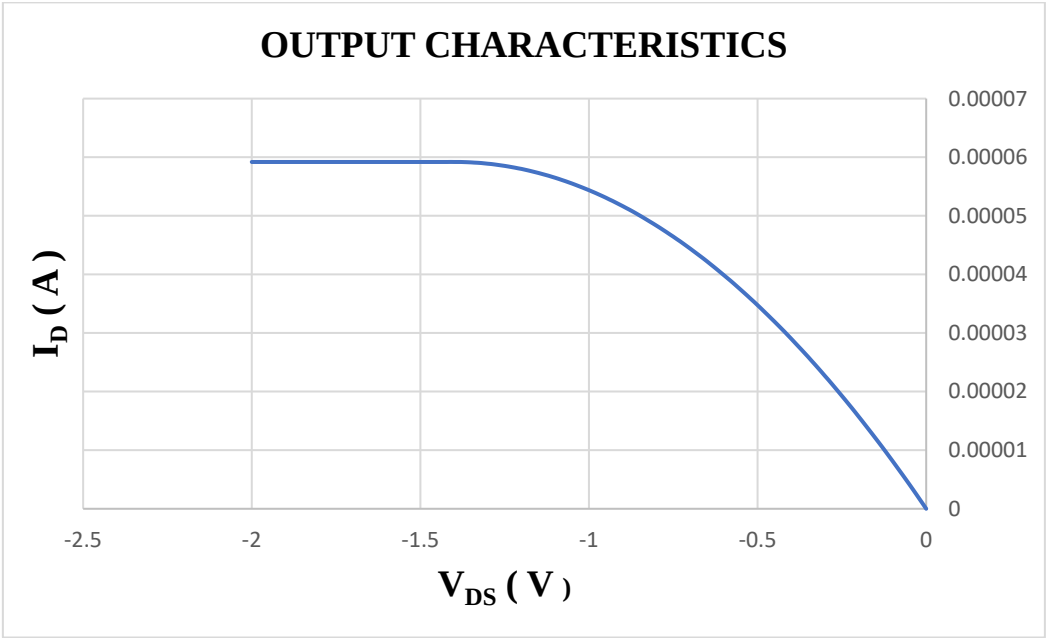
QUESTION 3

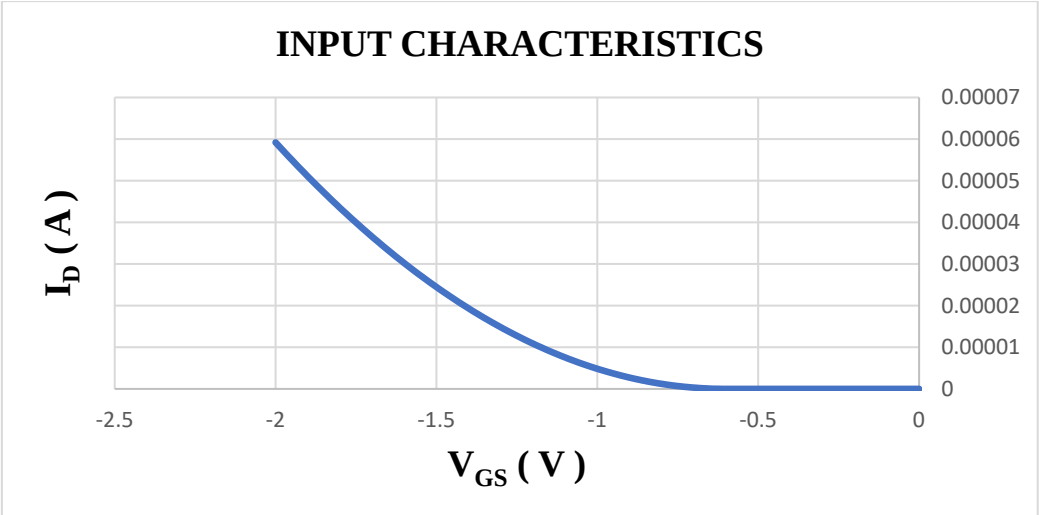
Repeat Q2(a) for a PMOS transistor. Plot magnitude of current versus V_{ds} (V_{dd} = 0 to -2 V) at V_{gg} = -2 V, and magnitude of current versus V_{gs} (V_{gg} = 0 to -2 V) at V_{dd} = -2 V. Consider V_{th} = -0.6 V.

Note the following differences compared to NMOS: PMOS is ON when **V_{gs} < Vth**, is in linear region when **V_{ds} >= (V_{gs} - V_{th})**, and is in saturation when **V_{ds} < (V_{gs} - V_{th})**.

RESULT AND OBSERVATION

The output and input characteristics are given below,





QUESTION 4

Design a CMOS inverter using NMOS (from Q2) and PMOS (from Q3) and verify by applying the same input square pulse as in Q2(b), however the pulse oscillates between 0 V and 2 V in this case. The circuit for CMOS is shown in Fig. A.

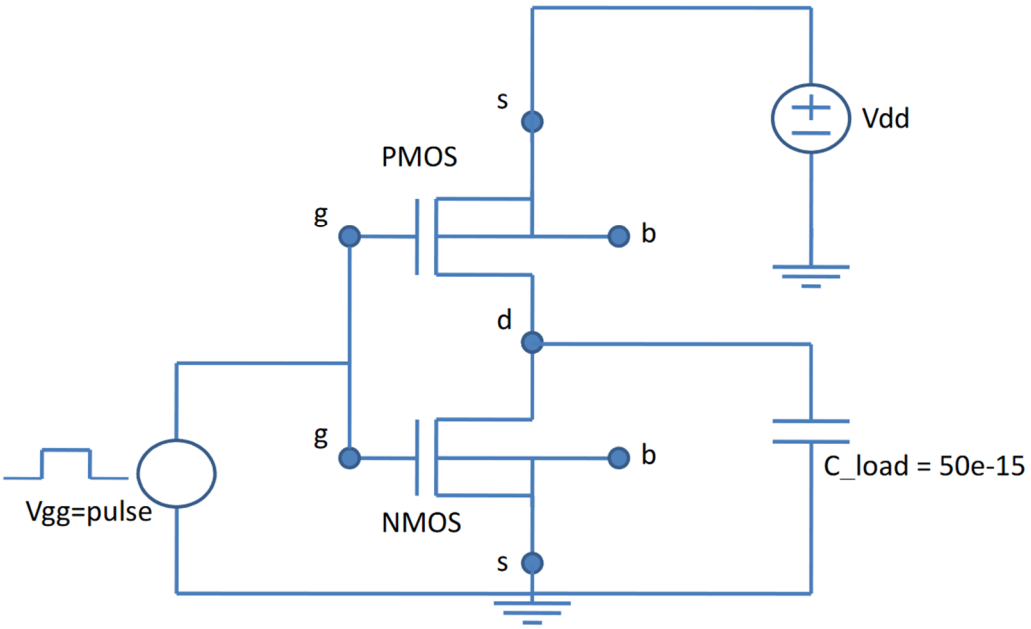


Fig. A: CMOS Inverter circuit

RESULT AND OBSERVATION

The input and output pulse waveforms are given below,