NETAJI SUBHAS UNIVERSITY OF TECHNOLOGY

CMOS Inverter Layout

Under the Guidance of:

Dr. URVASHI BANSAL

(Department of Electronics and Communication Engineering)

Submitted by:

Deepak Kumar (2023PEV3227)

Experiment

Aim

CMOS Inverter Layout Design Using Electric EDA Tool.

Software Used

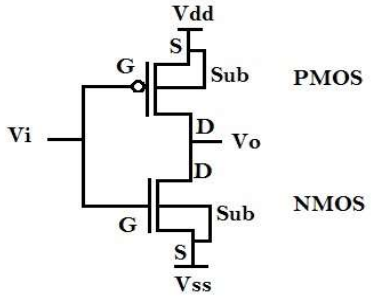
Electric EDA Tool
LTspice

Model File

- CMOS inverter layout at 180 nm technology.
- Model file essential for transistor characterization.
- Parameters include threshold voltage, mobility, capacitance.

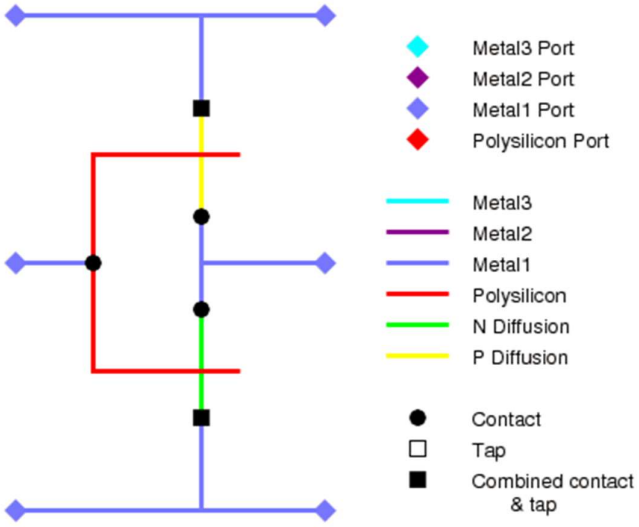
Theory

CMOS inverter layout involves physically designing NMOS and PMOS transistors, interconnections, and metal layers to create an inverter circuit. Stick diagram Euler, a graphical representation, simplifies this process by illustrating transistor placement and connections, aiding in efficient layout design for digital integrated circuits.



G = Gate Terminal
S = Source Terminal
D = Drain Terminal
Sub = Substrate Terminal

Schematic diagram of CMOS Inverter



Experimental Procedure

For Designing a CMOS Inverter Using an Electric VLSI EDA Tool:

1. Setting up Electric EDA:

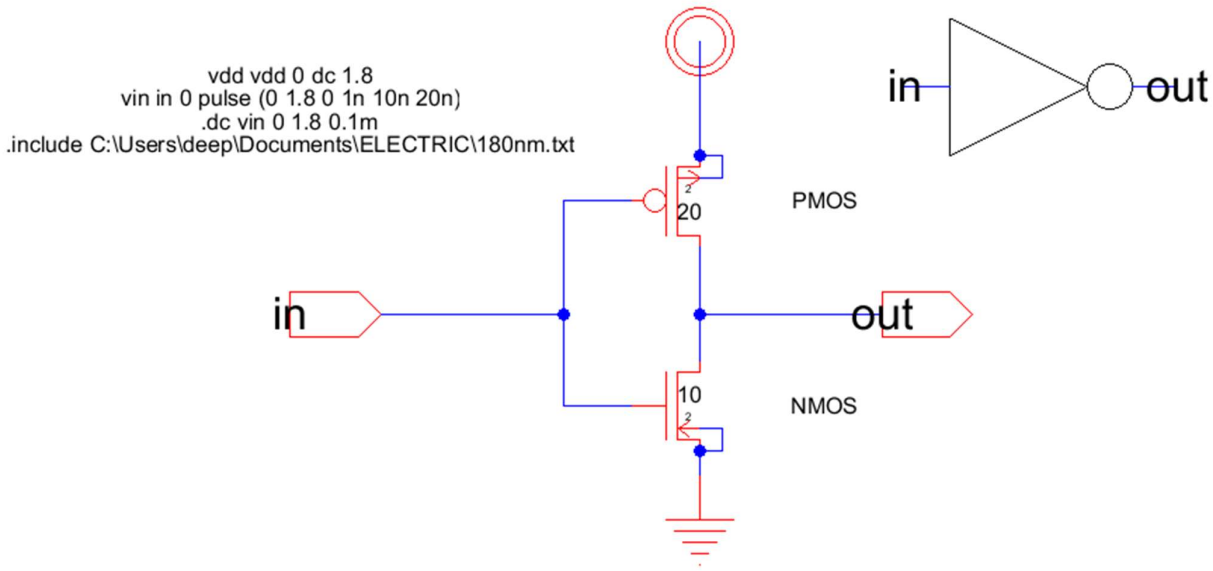
- Launch the Electric EDA tool on your computer.
- Ensure that the required technology library for CMOS is loaded.

2. Creating a New Project:

- Start a new project in Electric EDA.
- Define the technology parameters, such as feature size and layers, based on your CMOS library.

3. Designing CMOS Inverter Schematic:

- Design the CMOS inverter circuit by connecting the NMOS and PMOS transistors appropriately.
- Ensure the gate of the NMOS transistor is connected to the input signal and the gate of the PMOS transistor is connected to the inverse of the input signal.



4. Simulation Setup:

- Configure the simulation parameters, including the analysis type (e.g., DC analysis or transient analysis) and the input stimulus.

```
*\\DC Analysis\\*
vdd vdd 0 dc 1.8
vin in 0 pulse (0 1.8 0 1n 10n 20n)
.dc vin 0 1.8 0.1m
.include C:\Users\deep\Documents\ELECTRIC\180nm.txt

*\\Transient Analysis\\*
vdd vdd 0 dc 1.8
vin in 0 pulse 0 1.8 0 1n 1n .5m 1m
.tran 2m
.include C:\Users\deep\Documents\ELECTRIC\180nm.txt
```

5. Netlist Generation:

DC Characteristics

inverter_deepak.spi | inverter_deepak.spi

```
***     Metal-2: areacap=0.0843FF/um^2,  edgecap=0.0974FF/um,     res=0.078ohms/sq
***     Via2:    areacap=0.0FF/um^2, edgecap=0.0FF/um,    res=0.9ohms/sq
***     Metal-3: areacap=0.0843FF/um^2,  edgecap=0.0974FF/um,     res=0.078ohms/sq
***     Via3:    areacap=0.0FF/um^2, edgecap=0.0FF/um,    res=0.8ohms/sq
***     Metal-4: areacap=0.0843FF/um^2,  edgecap=0.0974FF/um,     res=0.078ohms/sq
***     Via4:    areacap=0.0FF/um^2, edgecap=0.0FF/um,    res=0.8ohms/sq
***     Metal-5: areacap=0.0843FF/um^2,  edgecap=0.0974FF/um,     res=0.078ohms/sq
***     Via5:    areacap=0.0FF/um^2, edgecap=0.0FF/um,    res=0.8ohms/sq
***     Metal-6: areacap=0.0423FF/um^2,  edgecap=0.1273FF/um,     res=0.036ohms/sq
***     Hi-Res:  areacap=0.0FF/um^2, edgecap=0.0FF/um,    res=1.0ohms/sq

*** TOP LEVEL CELL: inverter_deepak{lay}
Mnmos@0 out in#2nmos@0_poly-right gnd gnd NMOS L=0.36U W=1.8U AS=6.172P AD=4.228P PS=19.26U PD=13.86U
Mpmos@0 vdd in#0pmos@0_poly-right out vdd PMOS L=0.36U W=3.6U AS=4.228P AD=8.764P PS=13.86U PD=26.46U
** Extracted Parasitic Capacitors ***
C0 out 0 1.829fF
C1 in#1pin@2_polysilicon-1 0 0.168fF
** Extracted Parasitic Resistors ***
R0 in#0pmos@0_poly-right in#0pmos@0_poly-right##0 7.75
R1 in#0pmos@0_poly-right##0 in#1pin@2_polysilicon-1 7.75
R2 in#1pin@2_polysilicon-1 in#2nmos@0_poly-right 9.3
R3 in#1pin@2_polysilicon-1 in#1pin@2_polysilicon-1##0 8.525
R4 in#1pin@2_polysilicon-1##0 in#1pin@2_polysilicon-1##1 8.525
R5 in#1pin@2_polysilicon-1##1 in#1pin@2_polysilicon-1##2 8.525
R6 in#1pin@2_polysilicon-1##2 in 8.525

* Spice Code nodes in cell cell 'inverter_deepak{lay}'
vdd vdd 0 dc 1.8
vin in 0 pulse (0 1.8 0 1n 10n 20n)
.dc vin 0 1.8 0.1m
.include C:\Users\deep\Documents\ELECTRIC\180nm.txt
.END
```

Transient Characteristics

inverter_deepak.spi | inverter_deepak.spi

```
***     Metal-2: areacap=0.0843FF/um^2,  edgecap=0.0974FF/um,     res=0.078ohms/sq
***     Via2:    areacap=0.0FF/um^2, edgecap=0.0FF/um,    res=0.9ohms/sq
***     Metal-3: areacap=0.0843FF/um^2,  edgecap=0.0974FF/um,     res=0.078ohms/sq
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***     Metal-4: areacap=0.0843FF/um^2,  edgecap=0.0974FF/um,     res=0.078ohms/sq
***     Via4:    areacap=0.0FF/um^2, edgecap=0.0FF/um,    res=0.8ohms/sq
***     Metal-5: areacap=0.0843FF/um^2,  edgecap=0.0974FF/um,     res=0.078ohms/sq
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R1 in#0pmos@0_poly-right##0 in#1pin@2_polysilicon-1 7.75
R2 in#1pin@2_polysilicon-1 in#2nmos@0_poly-right 9.3
R3 in#1pin@2_polysilicon-1 in#1pin@2_polysilicon-1##0 8.525
R4 in#1pin@2_polysilicon-1##0 in#1pin@2_polysilicon-1##1 8.525
R5 in#1pin@2_polysilicon-1##1 in#1pin@2_polysilicon-1##2 8.525
R6 in#1pin@2_polysilicon-1##2 in 8.525

* Spice Code nodes in cell cell 'inverter_deepak{lay}'
vdd vdd 0 dc 1.8
vin in 0 pulse 0 1.8 0 1n 1n .5m 1m
.tran 2m
.include C:\Users\deep\Documents\ELECTRIC\180nm.txt
.END
```
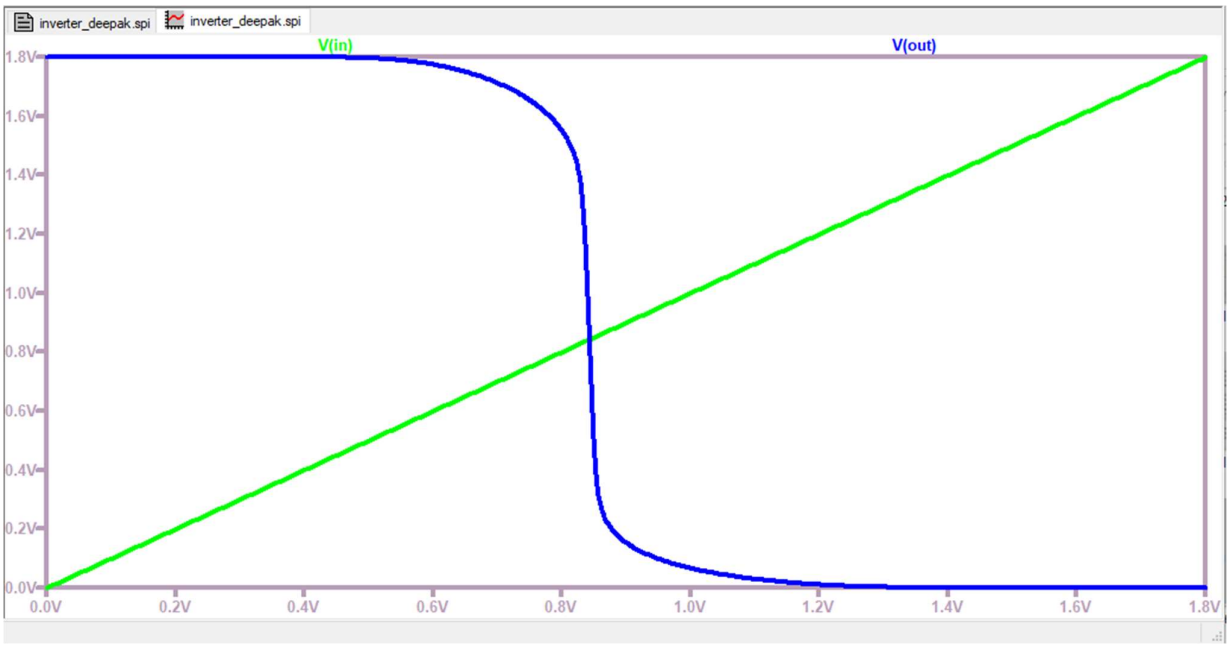
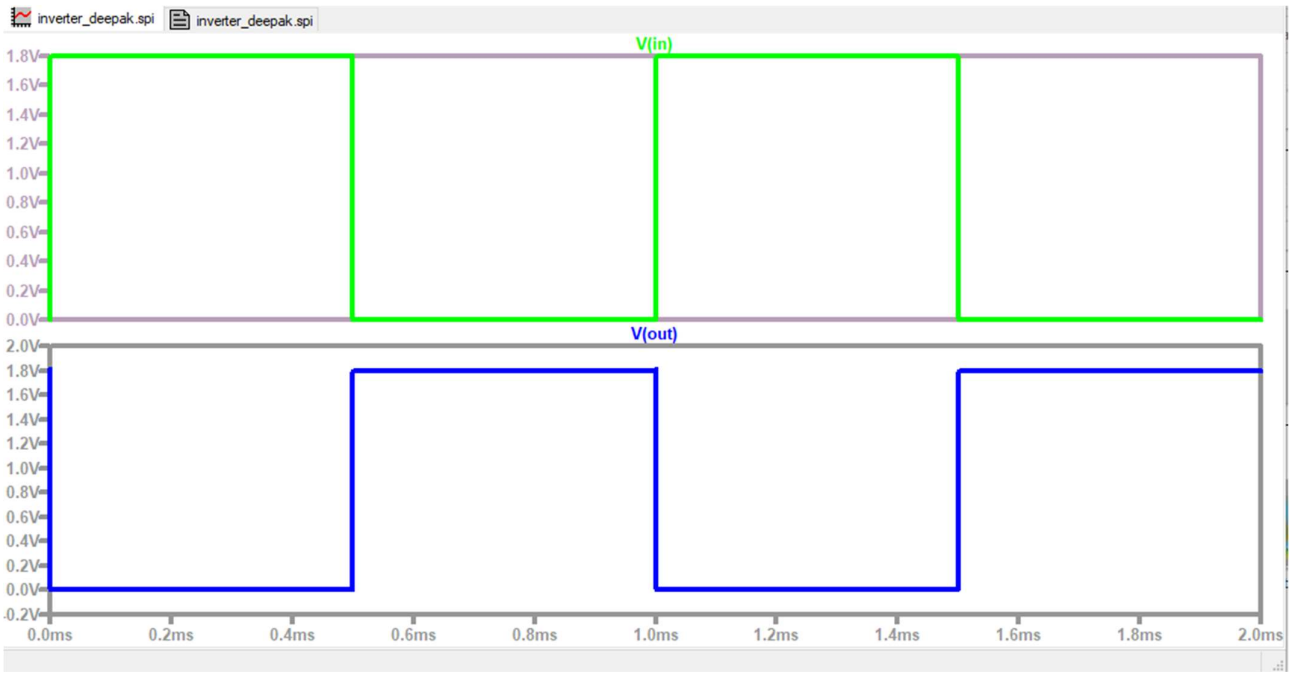

6. Simulation:

- Run a simulation to verify the functionality of the CMOS inverter.

DC Characteristics



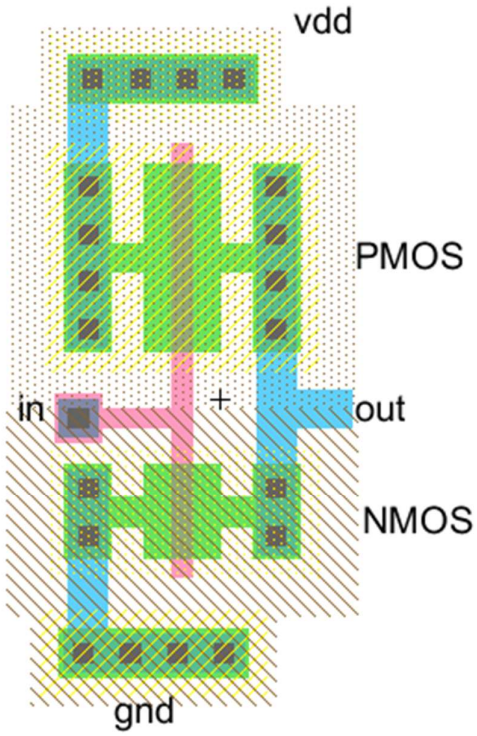
Transient Characteristics



7. Layout Design:

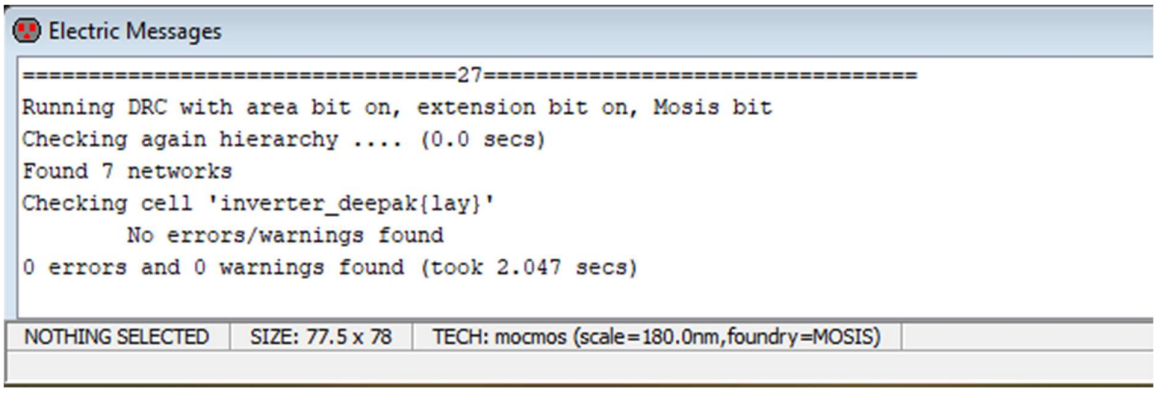
- Create a new layout file within the project.
- Start laying out the transistors and wires based on the schematic design.
- Pay attention to proper transistor sizes and spacing, adhering to the design rules of the chosen technology library.

```
vdd vdd 0 dc 1.8
vin in 0 pulse (0 1.8 0 1n 10n 20n)
.dc vin 0 1.8 0.1m
.include C:\Users\deep\Documents\ELECTRIC\180nm.txt
```



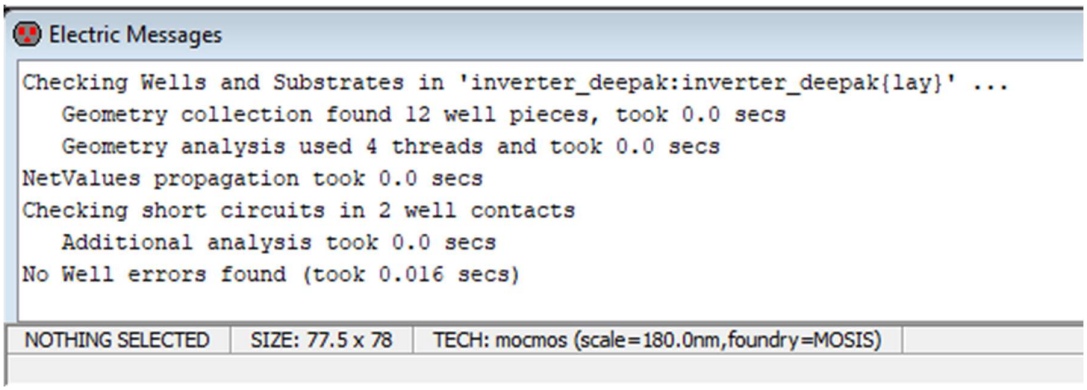
8. Design Rule Check (DRC):

- Run a DRC check to ensure that your layout complies with the technology-specific design rules.



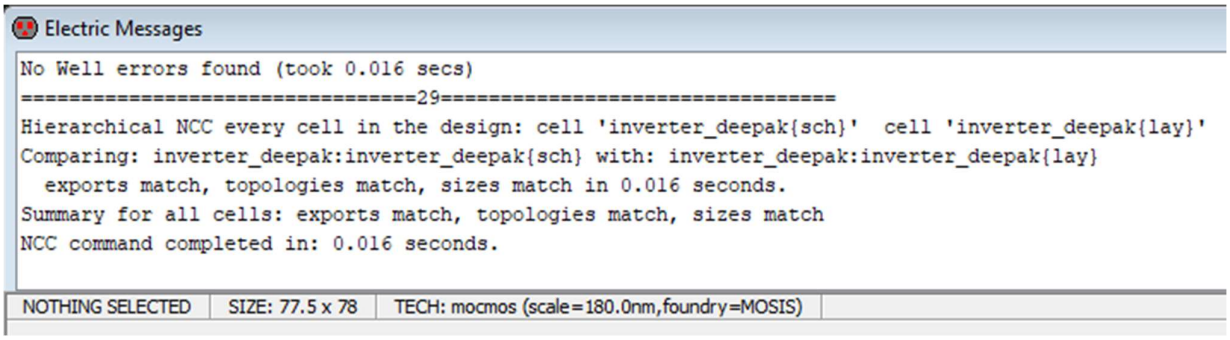
9. Well Check:

- Perform a Well check to ensure that the layout matches the schematic and that there are no connectivity or device mismatches.



10. NCC Check:

- NCC checks the layout and schematic of a CMOS inverter to see if they match



11. Final Layout Review:

- Carefully review the final layout to ensure it meets the design specifications.

12. Tape-Out:

- Prepare the design for manufacturing by generating the final GDSII layout file for fabrication.

13. Final Verification:

- Perform a final check to ensure all design rules and specifications.

14. Fabrication:

- Submit the GDSII layout to a foundry for semiconductor fabrication.

15. Testing:

- After fabrication, the CMOS inverter can be tested in a lab to validate its performance.

3D view of the Layout