Computer Organization and Architecture Laboratory (CS39001)

Design of a pipelined CPU

AIM: To design a pipelined version of the CPU for the same ISA specification for which a multi-cycle CPU has already been designed in the last experiment, by

1. first identifying whether the ISA specification or any other design constraints need any modification;
2. designing a single cycle data path for the CPU for this modified specification;
3. transforming it to a pipelined version by incorporating the pipeline stations among the stages of the datapath.

Assignment statement

1. Modify the ISA specification or other design constraints of the CPU of the previous experiment (on CPU Design) (in the least possible way) so that all the instructions in the instruction set can be executed on a single cycle datapath having a separate instruction memory and one data memory module, a separate incrementor / decrementor block over and above a single ALU.
2. Design and implement a single cycle datapath for the modified specification satisfying the aforementioned resource constraints.
3. Design the controller for the processor.
4. Testing of the single cycle CPU.
5. Incorporate the pipeline registers (stations) for storing operands / addresses and the control signal outputs of the decoder.
6. Testing of the pipelined CPU design.

Submissibles with marks:

1. **Lab day 1** Modified ISA specs and other design constraints, if any, with clear indication and brief justification of each of the modifications **in the lab record** **[5]**
   Deadlines with commensurate max. credits:
   100% max. credit – 2.11.'17 – 3.30 PM
   80% max. credit – 3.11.'17 – 2.30 PM
   70% max. credit – 3.11.'17 – 4.30 PM
   60% max. credit – later submissions
2. **Lab days 1 & 2**
   (a) Datapath paper design with diagrams **in the lab record**. Diagram should be neat. **[15]**
   Deadlines with commensurate max. credits:
   100% max. credit – 2.11.'17 – 4.30 PM
   90% max. credit – 3.11.'17 – 2.30 PM
   80% max. credit – 3.11.'17 – 4.30 PM
   60% max. credit – later submissions

   (b) Verilog structural coding of the controller with test bench **[15]**
   Deadlines with commensurate max. credits:
   100% max. credit – 3.11.'17 – 11.55 PM
   90% max. credit – 4.11.'17 – 11.55 PM
   70% max. credit – 5.11.'17 – 11.55 PM
   60% for later submission

3. **Lab days 3 and 4**

   (a) Verilog structural coding of the top level datapath assuming the Instruction Memory and Data Memory as two internal modules; **[10]**
   Deadlines with commensurate max. credits:
   100% max. credit – 9.11.'17 – 11.55 PM
   80% max. credit – 10.11.'17 –11.55 PM
   70% max. credit – 12.11.'17 –11.55 PM
   60% max. credit – later submissions

   (b) Verilog encoding of the data path modules — structural or behavioural as was done for the multi-cycle version with modifications, as needed. **[10]**
   Deadlines with commensurate max. credits:
   100% max. credit – 9.11.'17 – 11.55 PM
   80% max. credit – 10.11.'17 –11.55 PM
   70% max. credit – 12.11.'17 –11.55 PM
   60% max. credit – later submissions

4. **Lab days 5 and 6**

   (a) Combined module of the CPU with test bench. **[15]**
   Deadlines with commensurate max. credits:
   100% max. credit – 16.11.'17 – 11.55 PM
   80% max. credit – 17.11.'17 –11.55 PM
   70% max. credit – 18.11.'17 –11.55 PM
   60% max. credit – 19.11.'17 – 10.00 AM

   (b) Verilog structural encoding of the pipelined data path by incorporating into the structural description of the top level single cycle data path structure the modules corresponding to the pipeline stations and defining these modules by their behavioural encodings along with the same test bench as given in 4a. **[15]**
   Deadlines with commensurate max. credits:
   100% max. credit – 16.11.'17 – 11.55 PM
   80% max. credit – 17.11.'17 –11.55 PM
   70% max. credit – 18.11.'17 –11.55 PM
   60% max. credit – 19.11.'17 – 10.00 AM