PROJECT REPORT

ON

FPGA BASED TRAFFIC LIGHT CONTROLLER

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ABSTRACT

The function of a traffic light controller requires control, coordination to ensure that traffic, and pedestrian move as safely and smoothly as possible. This project proposes a modern FPGA based traffic light control system to manage the road traffic. A variety of different control systems are used to accomplish this ranging from simple clock-work mechanisms to sophisticated computerized control and coordination systems that self-adjust to minimize delay. Our approach is to control the access to areas shared among multiple intersections and allocating effective time between various users. The implementation is based on a real location in San Jose California. The proposed design is universal and intelligent approach to the situation and will be implemented using FPGA.

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CHAPTER 1

INTRODUCTION

The traffic congestion has always been a plight in modern cities all around the world. This problem has led to jamming around a signal, which reduces the ease of commute and hence decreases productivity of commuters. The traffic system has two major tasks, the first being right of way for a particular group of commuters for a given time and the second task is to avoid gridlock situation. The objective of this project is to design a traffic control system of a real location in San Jose, California where the given intersection is in harmony with the neighboring intersections with appropriate delay to clear the congestion between them and yields the pedestrian crosswalks.

The design is implemented using Field Programmable Gate Array, which has various benefits such as speed, hardware acceleration and parallelism, increasing reliability by having fewer on-board devices, long-term maintenance. FPGA uses fewer clock cycles to process larger data, and the update on FPGA is easier as no change in circuit layout is required. Altera Cyclone II EP2C20F484C7N FPGA is used to implement the proposed design.

CHAPTER 2

DESIGN AND IMPLEMENTATION

The traffic light controller is designed for the intersections shown in Fig 2.1. The two junctions on the right of Freeway 280 are considered for implementation. Junction-1 from the exit of Freeway 280 has two signals and three pedestrian switches. Further ahead is junction-2 which also has two traffic signals and three pedestrian switches.

Since the distance from junction-1 to junction-2 is less, this leads to congestion at junction-2 region, so in-order to combat this issue, the delay between the two needs to be taken care.

Fig 2.1: 11th Street, San Jose, California

2.1 STATE TABLE

RST	CLK	STATE	N1S	N1R	N2S	N2L	E1S	E1L	W1S	W1R	P1	P2	P3	P4
0	↑	s1	R	G	G	G	R	G	R	R	OFF	OFF	OFF	ON
0	↑	s2	R	Y	G	Y	R	Y	R	R	OFF	OFF	OFF	ON
0	↑	s3	G	R	G	R	R	R	R	R	OFF	ON	OFF	ON
0	↑	s4	G	R	Y	R	R	R	R	R	OFF	ON	ON	ON
0	↑	s5	Y	R	R	R	R	R	G	G	OFF	ON	ON	OFF
0	↑	s6	R	R	R	R	G	R	G	Y	ON	OFF	ON	OFF
0	↑	s7	R	R	R	R	G	R	G	Y	ON	OFF	ON	OFF
0	↑	s8	R	R	R	R	Y	R	Y	R	ON	OFF	ON	OFF

Table 2.1: State Table

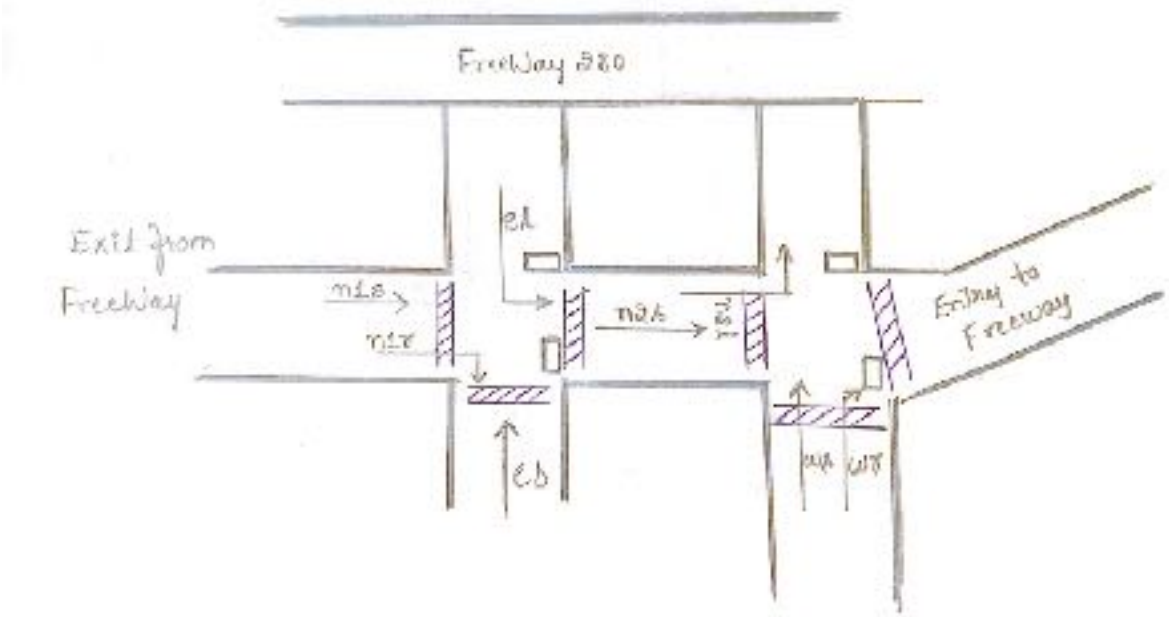

Fig 2.2: Signal Variables

The signal variables assigned to junction-1 are **n1s**, **n1r**, **es**, **el** and **n2s**, **n2l**, **ws**, **wr** are for junction-2. In addition, **p1**, **p2**, **p3**, **p4** are the pedestrian switches at both the junctions.This design has 8 states, with specific delay assigned to each state. A change in signal condition is depicted in each signal variable at every state.

2.2 STATE DIAGRAM

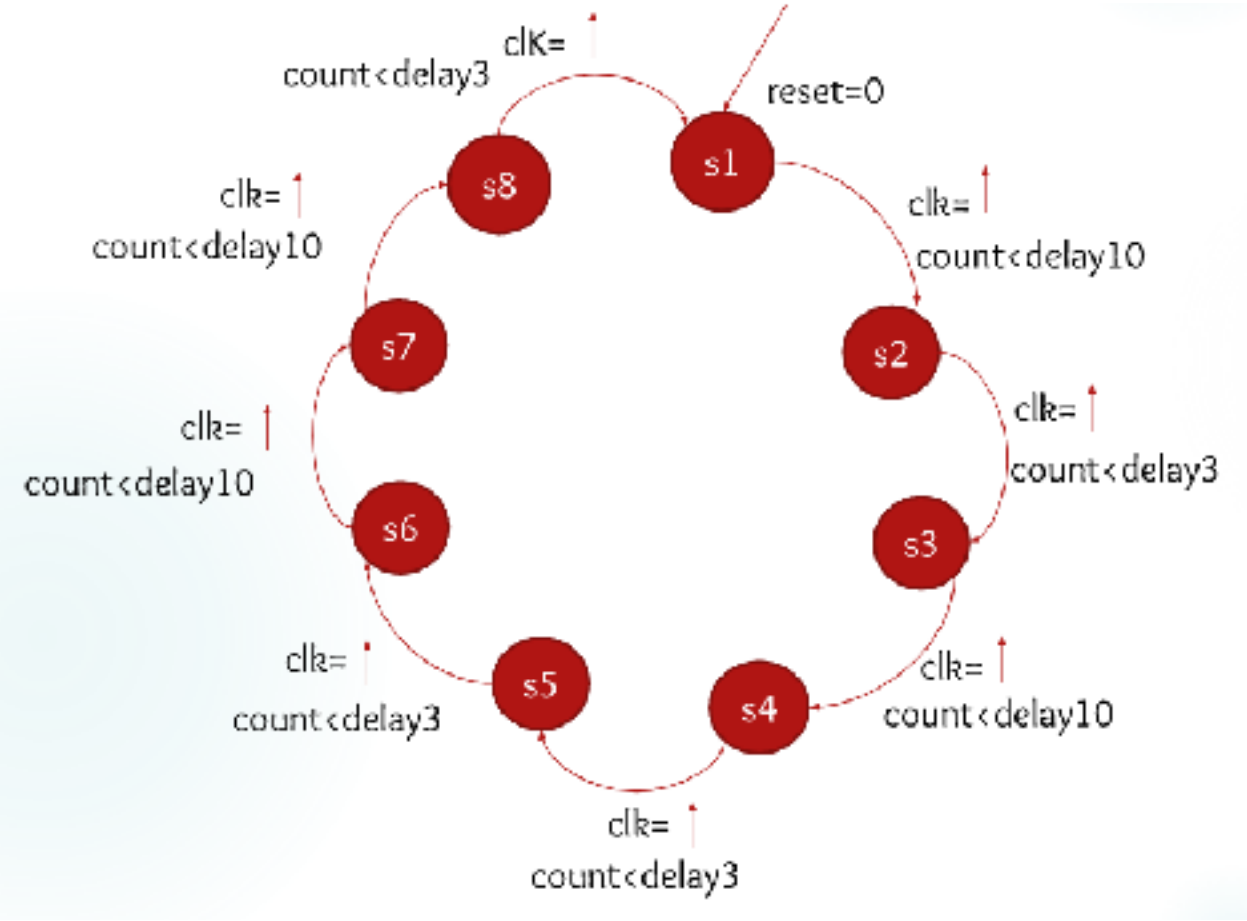

Fig 2.3: State Diagram

The State diagram starts with positive edge of clock, reset is considered for just state **S1** and change in reset condition leads to next state. Every state has a delay time specified. Some states have delay time to be just 3 sec and the others are for 10 sec considering the condition of signal variable .These states are of the finite state machine type. In the duration of the delays for each state, the pedestrian switch change yielding the pedestrians.

2.3 Delays and Pedestrian Switch

Delays are given high importance in implementation of traffic signals, as they play major role in clearing and avoiding gridlock situation at junction-2. Delays are assigned such that the traffic at **n2s** is less and the efficient functioning of other signals are also maintained. The delays for every state changes considering the signal condition of all the signal variable.

Pedestrian switch gives right to yield on the given intersections. At the normal functioning of the states, the pedestrian switch are taken care according to changing signal conditions. At every state the pedestrian switch condition changes giving fair chance to the pedestrian even when the switch is not pressed.

If a pedestrian switch is on and the incoming vehicles are low at a particular signal, yield is given to the pedestrian by stopping the functioning of the traffic light clock.

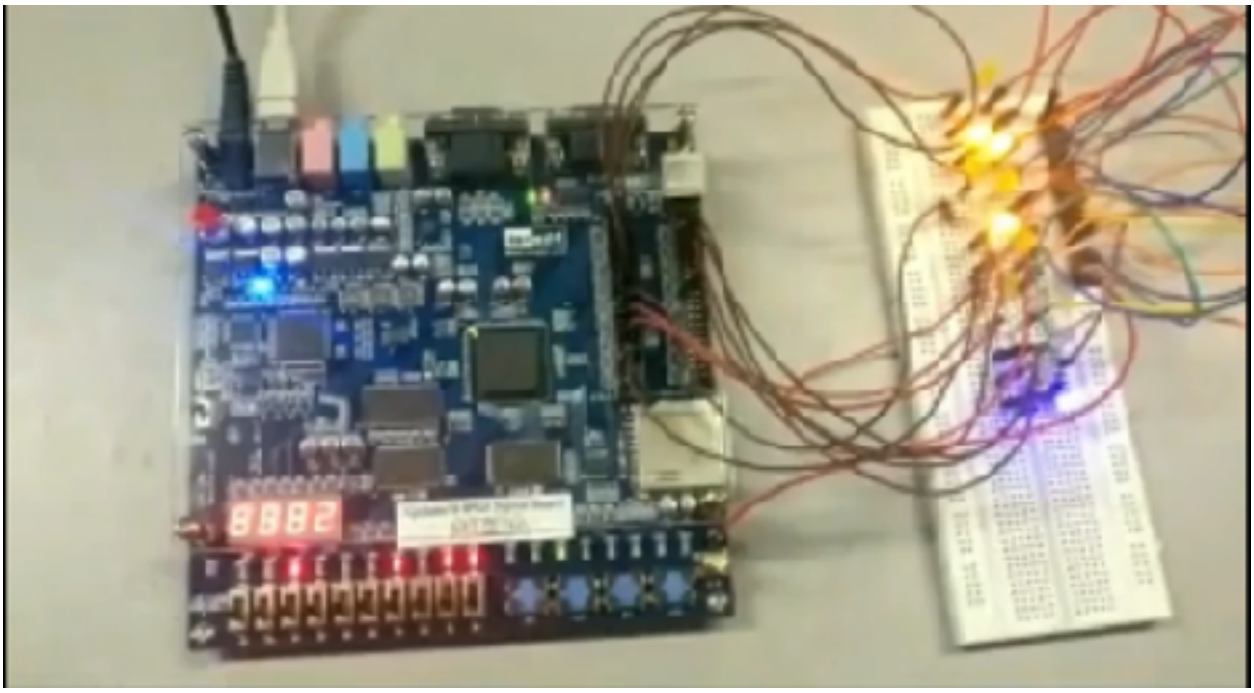

Fig 2.3.1: Working signal states

2.4 PIN PLANNER

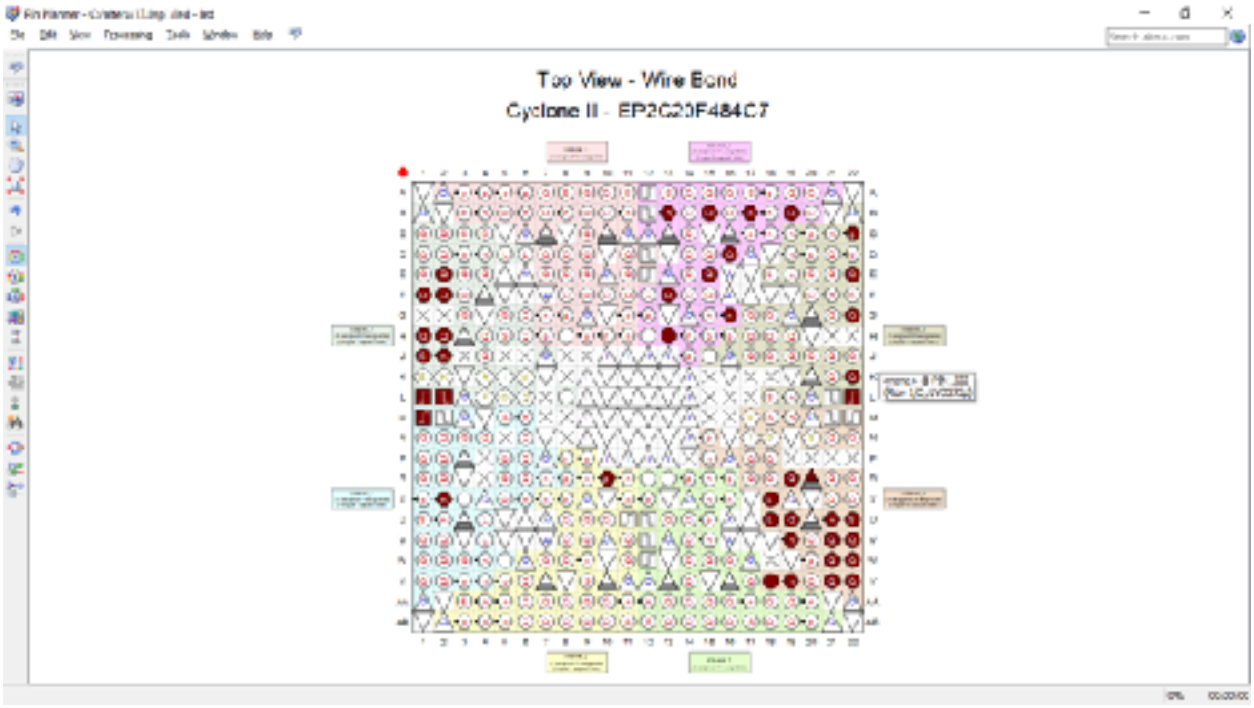

Fig 2.4.1: Graphical view of pins

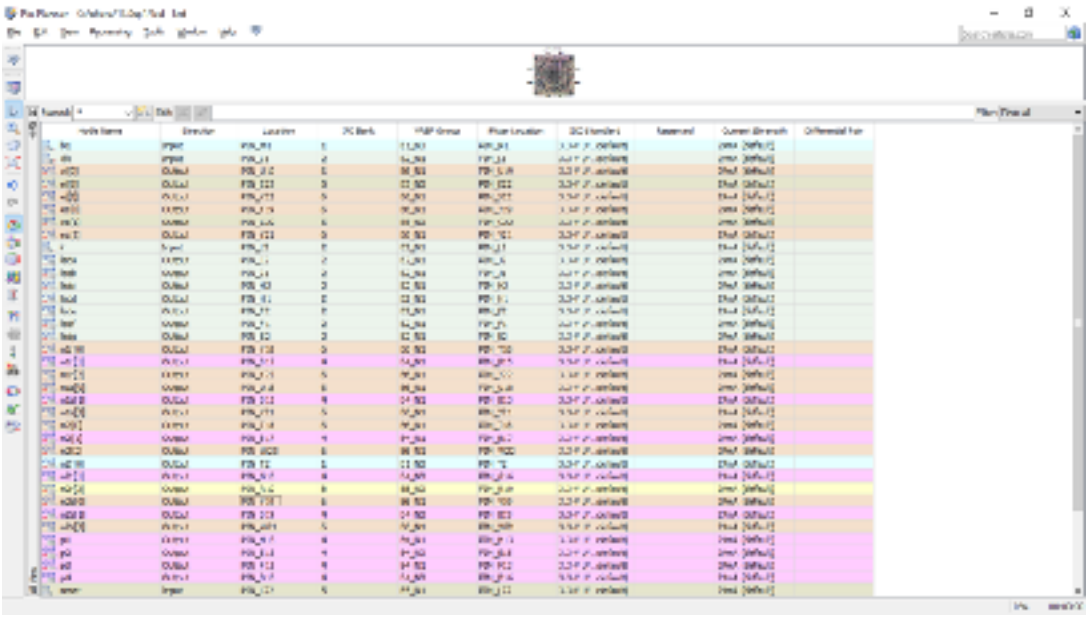

Fig 2.4.2: Pin assignments

CHAPTER 3

HARDWARE AND SOFTWARE REQUIREMENTS

3.1 Altera Cyclone II EP2C20F484C7N FPGA

Cyclone series FPGAs and SoC FPGAs are the company's lowest cost, lowest power FPGAs, with variants offering integrated transceivers up to 5 Gbit/s. Cyclone II FPGAs are perfectly suited as an embedded processor or microcontroller when combined with Intel's 32-bit Nios II embedded processor IP cores. The Cyclone II FPGA Starter Development Kit features:

- Cyclone II Starter Development Board
- Cyclone II EP2C20F484C7N device
- Configuration
    - USB-Blaster™ download cable (embedded)
    - EPCS4 serial configuration device
- Memory
    - 8-Mbyte SDRAM
    - 512-Kb SRAM
    - 1- to 4-Mbyte flash
- Clocking
    - SMA connector (external clock input)
- Audio
    - 24-bit coder/decoder (CODEC)
- Switches and indicators
    - Ten switch and four push buttons
    - Four, 7-segment displays

    - Ten red and eight green LEDs
- Connectors
    - VGA, RS-232, and PS/2 ports
    - Two 40-pin expansion ports
    - SD/MMC socket

3.2 Quartus II 13.0sp

The Altera Quartus II design software is a multiplatform design environment that easily adapts to your specific needs in all phases of FPGA and CPLD design. Quartus II software delivers the highest productivity and performance for Altera FPGAs, CPLDs, and HardCopy ASICs. Quartus II software delivers superior synthesis and placement and routing, resulting in compilation time advantages. Compilation time reduction features include:

• Multiprocessor support

• Rapid Recompile

• Incremental compilation

The Altera Quartus II design software provides a complete design environment that easily adapts to your specific design requirements.

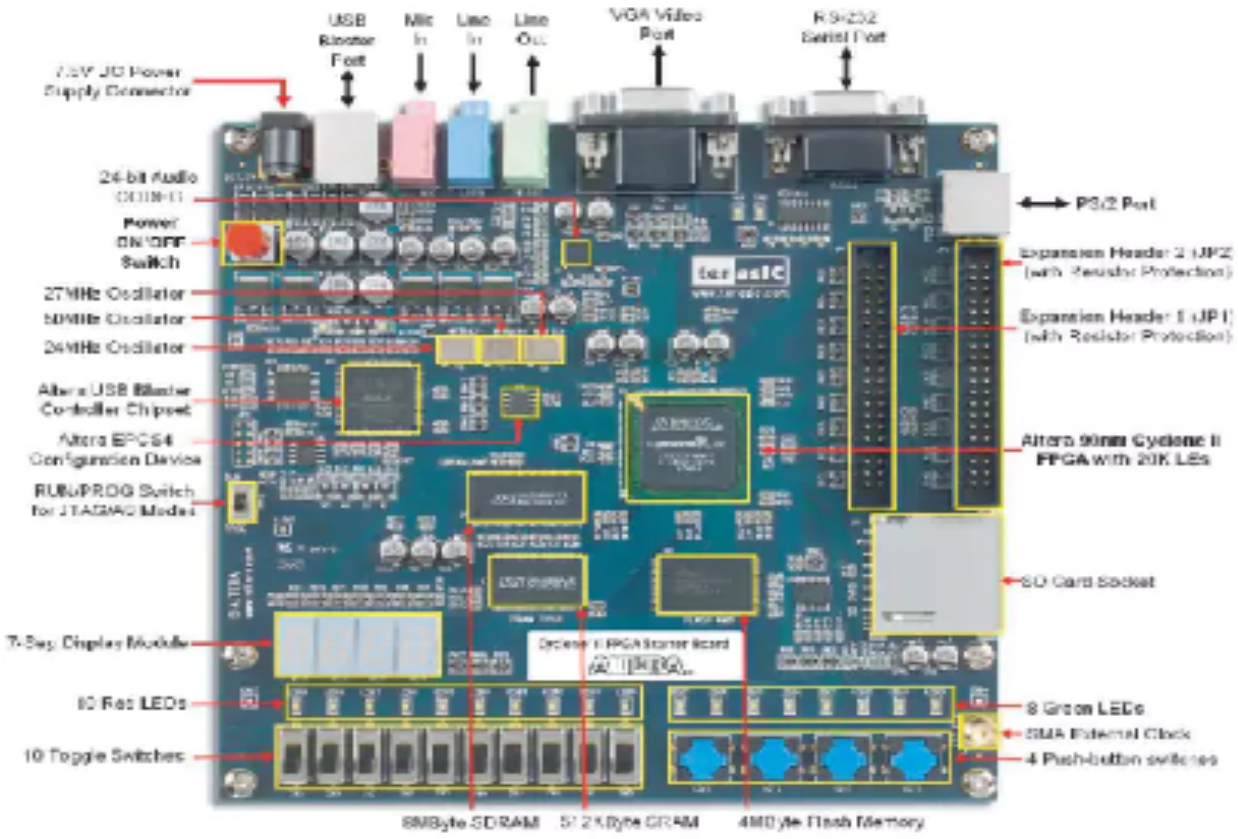

Fig 3.1: Cyclone II FPGA Starter Development Kit

3.3 LEDS

LEDs stand for Light Emitting Diodes. They are a type of a diode, which converts electrical energy into light.

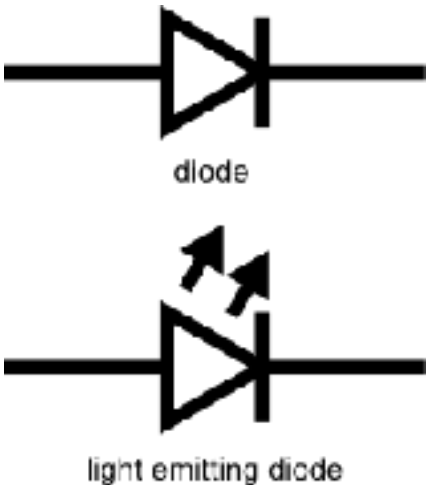

Fig3.3.1 Light Emitting Diode

In short, LEDs are like tiny lightbulbs. However, LEDs require a lot less power to light up by comparison. They are also more energy efficient, so they don't tend to get hot like conventional lightbulbs do. This makes them ideal for mobile devices and other low-power applications. High-intensity LEDs have found their way into accent lighting, spotlights and even automotive headlights.

Fig3.3.2:Red, Green and Blue LEDs

These LEDs can work on different spectrum of wavelengths from Infrared region used in object detection, remote control to ultra-violet LEDs to make certain materials fluoresce, just like a black light. They are also used for disinfecting surfaces, because many bacteria are sensitive to UV radiation.

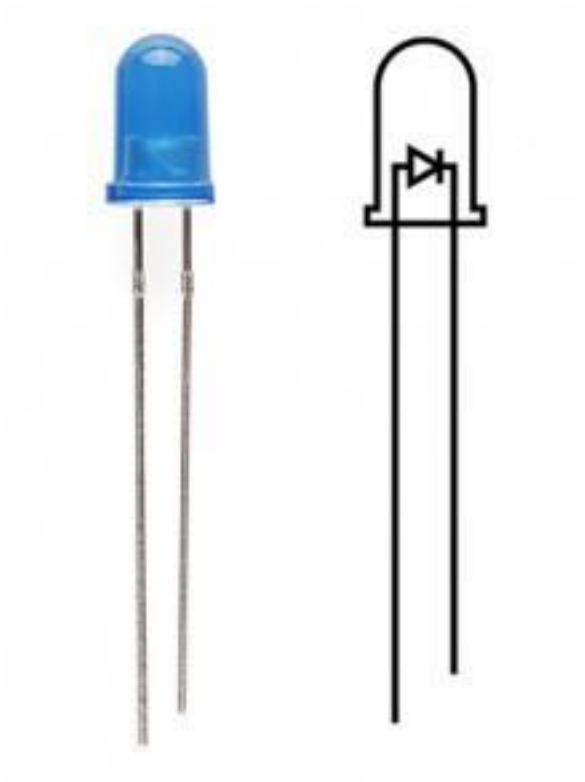

Fig 3.3.3: Anode and Cathode of LED

The positive side of the LED is called the **“anode”** and is marked by having a longer “lead,” or leg. The other, negative side of the LED is called the **“cathode.”** Current flows from the anode to the cathode and never the opposite direction. A reversed LED can keep an entire circuit from operating properly by blocking current flow.

3.4 Seven Segment Display

The *7-segment display*, also written as “seven segment display”, consists of seven LEDs (hence its name) arranged in a rectangular fashion as shown. Each of the seven LEDs is called a segment because when illuminated the segment forms part of a numerical digit (both Decimal and Hex) to be displayed. An additional 8th LED is sometimes used within the same package thus allowing the indication of a decimal point, (DP) when two or more 7-segment displays are connected together to display numbers greater than ten.

Each one of the seven LEDs in the display is given a positional segment with one of its connection pins being brought straight out of the rectangular plastic package. These individually LED pins are labelled from a through to g representing each individual LED. The other LED pins are connected together and wired to form a common pin.

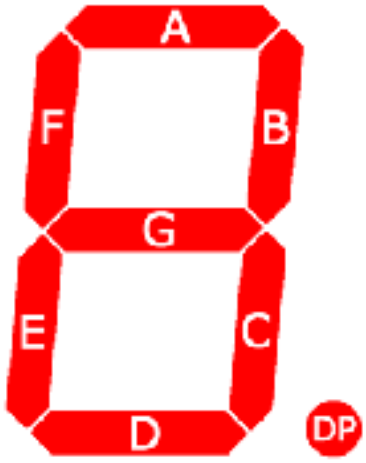

Fig 3.4.1: Seven-Segment Display

By forward biasing the appropriate pins of the LED segments in a particular order, some segments will be light and others will be dark allowing the desired character pattern of the number to be generated on the display. This then allows us to display each of the ten decimal digits 0 through to 9 on the same 7-segment display.

The displays common pin is generally used to identify which type of 7-segment display it is. As each LED has two connecting pins, one called the “Anode” and the other called the “Cathode”, there are therefore two types of LED 7-segment display called: **Common Cathode** (CC) and **Common Anode** (CA).

Decimal Digit	Input lines				Output lines							Display pattern
	A	B	C	D	a	b	c	d	e	f	g	
0	0	0	0	0	1	1	1	1	1	1	0	
1	0	0	0	1	0	1	1	0	0	0	0	
2	0	0	1	0	1	1	0	1	1	0	1	
3	0	0	1	1	1	1	1	1	0	0	1	
4	0	1	0	0	0	1	1	0	0	1	1	
5	0	1	0	1	1	0	1	1	0	1	1	
6	0	1	1	0	1	0	1	1	1	1	1	
7	0	1	1	1	1	1	1	0	0	0	0	
8	1	0	0	0	1	1	1	1	1	1	1	
9	1	0	0	1	1	1	1	1	0	1	1	

Table 3.4.1: Seven segment Display Truth table

CHAPTER 4

SIMULATION RESULTS

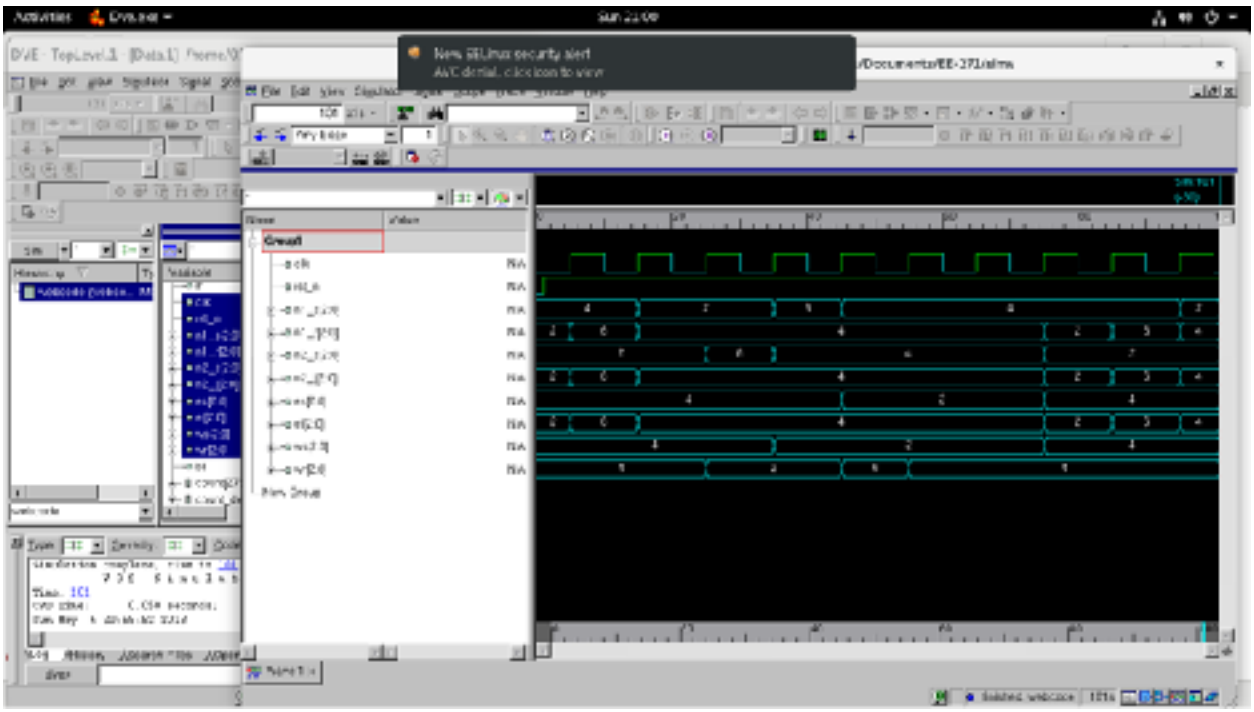

Fig 4.1: Waveform

The simulation is performed using Synopsys VCS based on the design discussed above.

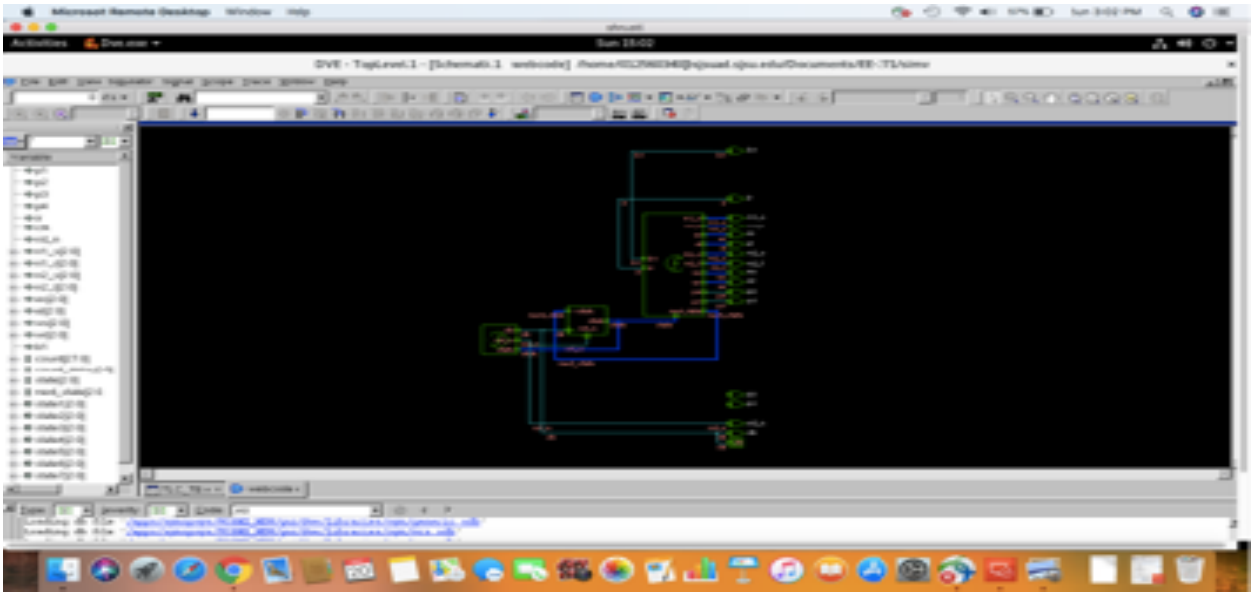

Fig 4.2: Schematic View

CHAPTER 5

CONCLUSION

- With our project, we have tried to resolve the traffic congestion at the given location i.e. 11th street San Jose, California.
- The delays given in our project helps in providing ease of commute for commuters at every direction.
- Our implementation of synchronous traffic clock cycle reduces the bottleneck situation at **n2s**.
- We have also managed to prioritize pedestrians by giving additional switch case along with the normal flow of traffic clock.

CHAPTER 6

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