

**PROJECT REPORT**  
**ON**  
**FPGA BASED VENDING MACHINE**

Submitted by

**Deepak Shivani (012560340)**

**Navyashree Chandraiah (012555192)**

**Shrusti Shashidhar (012418523)**

Under the guidance of

**Prof. John (JeongHee) Kim**

## **ABSTRACT**

A vending machine is an automated machine that provides items such as snacks, beverages, and lottery tickets to consumers after money, a credit card, or specially designed card is inserted into the machine. Vending machines exist in many countries, and in more recent times, specialized vending machines that provide less common products compared to traditional vending machine items have been created and provided to consumers.

The FPGA based vending machines are more flexible and faster than the CMOS based machines. The FPGA based vending machine is also programmable and can be reprogrammed. This project proposes a modern FPGA Vending machine, which is flexible, programmable and can be reprogrammed.

# TABLE OF CONTENTS

## **Abstract**

<b>1. Introduction</b>	<b>1</b>
<b>2. Design and Implementation</b>	<b>2</b>
2.1. State Table	2-3
2.2. Pin Planner	4
<b>3. Hardware and Software Requirements</b>	<b>5-9</b>
<b>4. Simulation Results</b>	<b>10-11</b>
<b>5. Conclusion</b>	<b>12</b>
<b>6. References</b>	<b>13</b>

# CHAPTER 1

## INTRODUCTION

Vending machines are commonly used to dispense beverages and snack items after entering certain amount of money into it. They can be accessed around the clock without any regard of holiday. These machines also provide diversity in their selling products. Zero labor required for its functioning makes this machine widely recognized. For the added advantage they can be installed in disaster relief area and they can also work on low electricity, giving ease in maintenance. These machines aren't just for selling food products but are also used for selling/lending electronic devices in these modern days.

As FPGA based vending machines are more flexible, the design is implemented using FPGA, which has various benefits such as speed, hardware acceleration and parallelism, increasing reliability by having fewer on-board devices, long-term maintenance. FPGA uses fewer clock cycles to process larger data, and the update on FPGA is easier as no change in circuit layout is required. Altera Cyclone II EP2C20F484C7N FPGA is used to implement the proposed design.



Fig 1.1: Vending machine

## CHAPTER 2

### DESIGN AND IMPLEMENTATION

The design of vending machine involves selection from the available choices. It starts with selecting an item and inserting the right amount of money into the machine, and then the product is dispensed. The excess amount calculated within the machine is then refunded based on the price of the item selected and the amount inserted by the customer.

#### 2.1 STATE TABLE

State	Item1 (Price-\$1)	Item2 (Price-\$2)	Item3 (Price-\$3)	M1 (\$1)	M5 (\$5)	Change (7Seg1)	Amount to be added (7Seg2)	Item Selected (7Seg4)
1	1	0	0	1	0	0	0	1
2	1	0	0	0	1	4	0	1
3	0	1	0	1	0	0	1	2
4	0	1	0	0	1	3	0	2
5	0	0	1	1	0	0	2	3
6	0	0	1	0	1	2	0	3

Table 2.1.1: State Table

Our design involves three items namely Item1, Item2 and Item3. Item1 is considered as \$1, Item2 is of \$2, and Item3 of \$3. To test the proper functioning of the machine, the valid currency to be inserted is \$1 and \$5 as depicted in the Table 2.1. And the design involves three seven segment display's on the FPGA. The first seven segment displays the change to be returned to the customer, the second seven segment displays the excess amount to be added when the customer has entered lesser amount with respect to the item selected, and the fourth seven segment display on the FPGA displays the item selected. The vending machine works only when the reset switch is high.

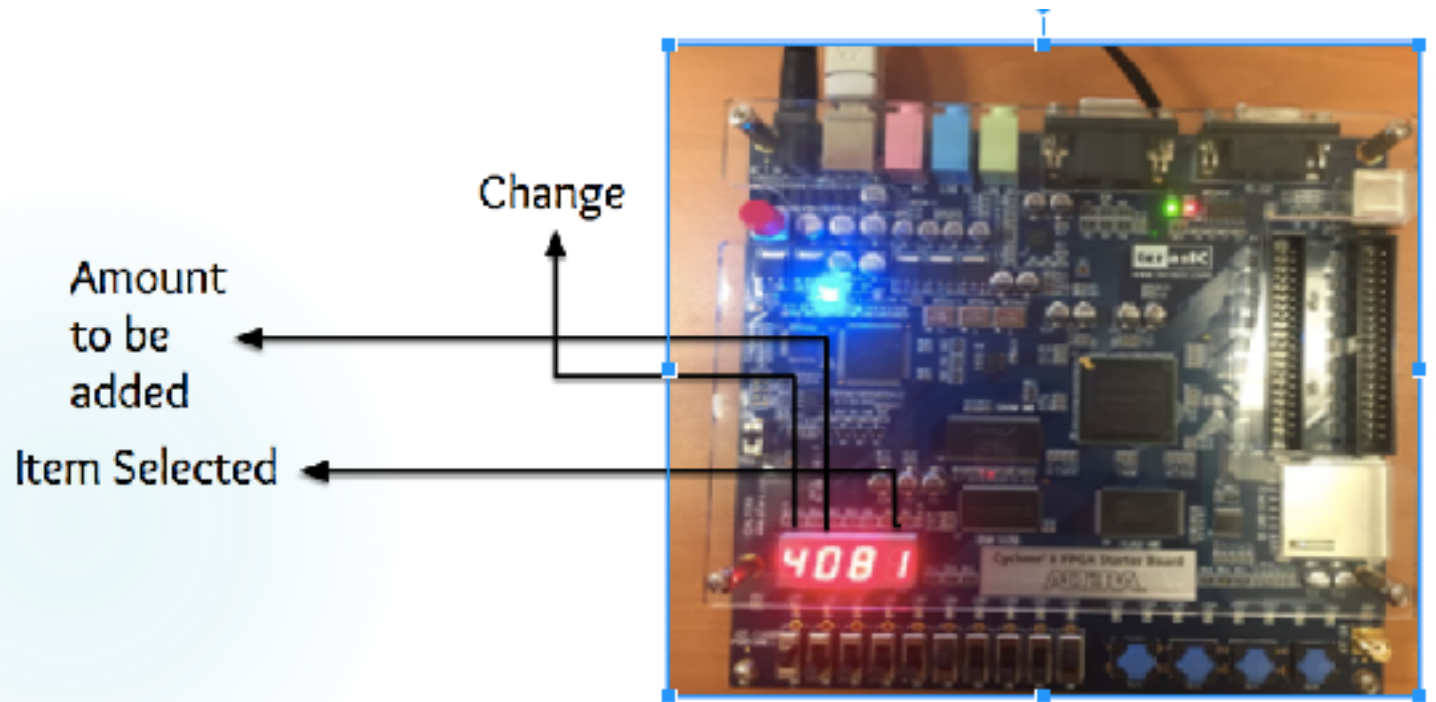


Fig 2.1 Working image of a vending machine

2.2 PIN PLANNER

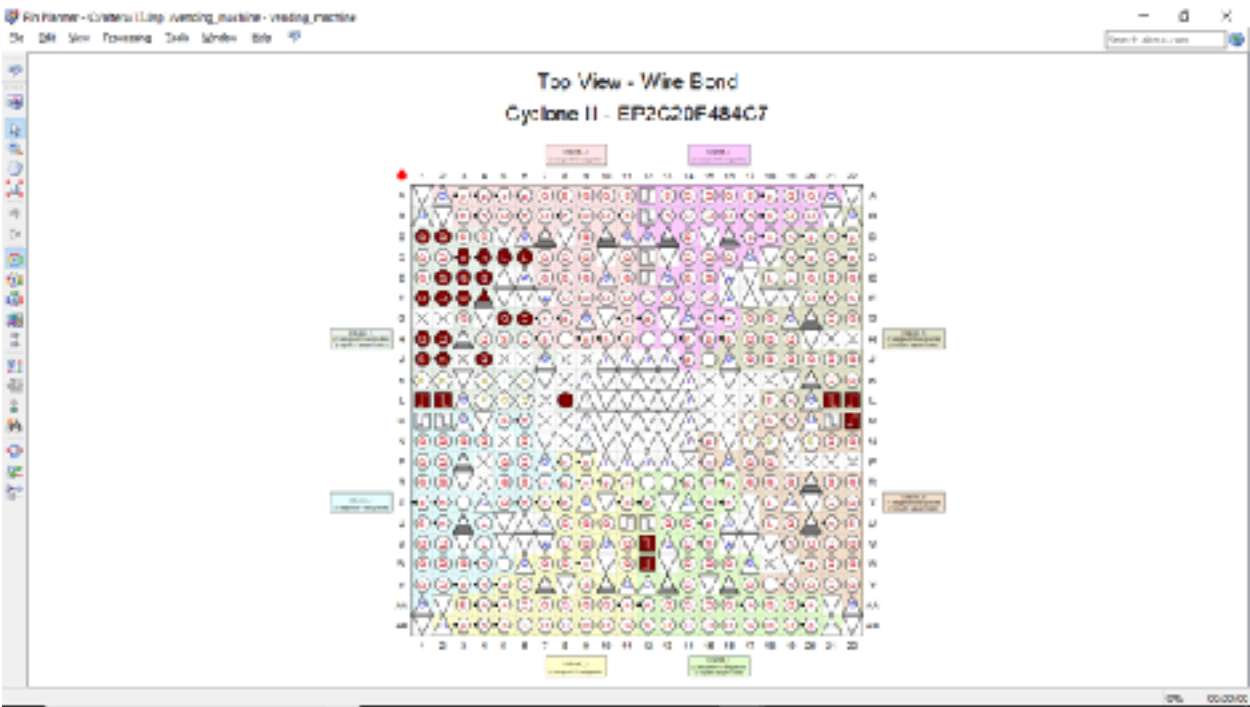


Fig 2.2.1: Graphical view of pins

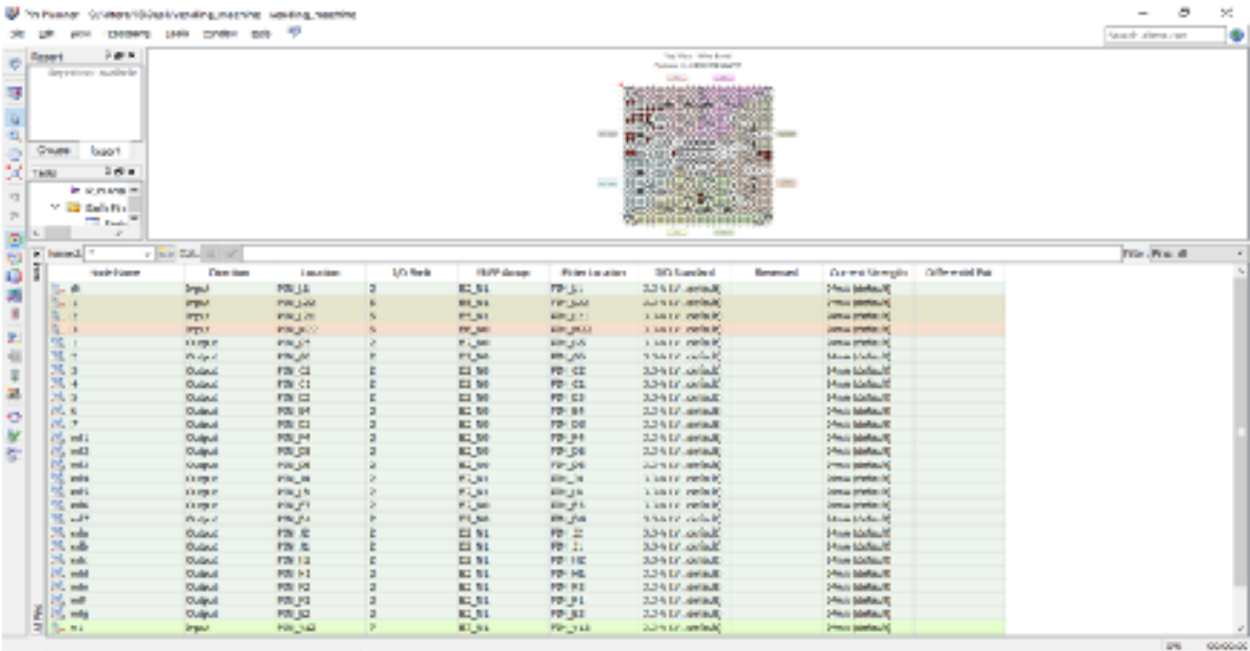


Fig 2.2.2: Pin assignments

## CHAPTER 3

### HARDWARE AND SOFTWARE REQUIREMENTS

#### 3.1 Altera Cyclone II EP2C20F484C7N FPGA

Cyclone series FPGAs and SoC FPGAs are the company's lowest cost, lowest power FPGAs, with variants offering integrated transceivers up to 5 Gbit/s. Cyclone II FPGAs are perfectly suited as an embedded processor or microcontroller when combined with Intel's 32-bit Nios II embedded processor IP cores. The Cyclone II FPGA Starter Development Kit features:

- Cyclone II Starter Development Board
- Cyclone II EP2C20F484C7N device
- Configuration
  - USB-Blaster™ download cable (embedded)
  - EPCS4 serial configuration device
- Memory
  - 8-Mbyte SDRAM
  - 512-Kb SRAM
  - 1- to 4-Mbyte flash
- Clocking
  - SMA connector (external clock input)
- Audio
  - 24-bit coder/decoder (CODEC)
- Switches and indicators
  - Ten switch and four push buttons
  - Four, 7-segment displays



- Ten red and eight green LEDs
- Connectors
  - VGA, RS-232, and PS/2 ports
  - Two 40-pin expansion ports
  - SD/MMC socket

### **3.2 Quartus II 13.0sp**

The Altera Quartus II design software is a multiplatform design environment that easily adapts to your specific needs in all phases of FPGA and CPLD design. Quartus II software delivers the highest productivity and performance for Altera FPGAs, CPLDs, and HardCopy ASICs. Quartus II software delivers superior synthesis and placement and routing, resulting in compilation time advantages. Compilation time reduction features include:

- Multiprocessor support
- Rapid Recompile
- Incremental compilation

The Altera Quartus II design software provides a complete design environment that easily adapts to your specific design requirements.

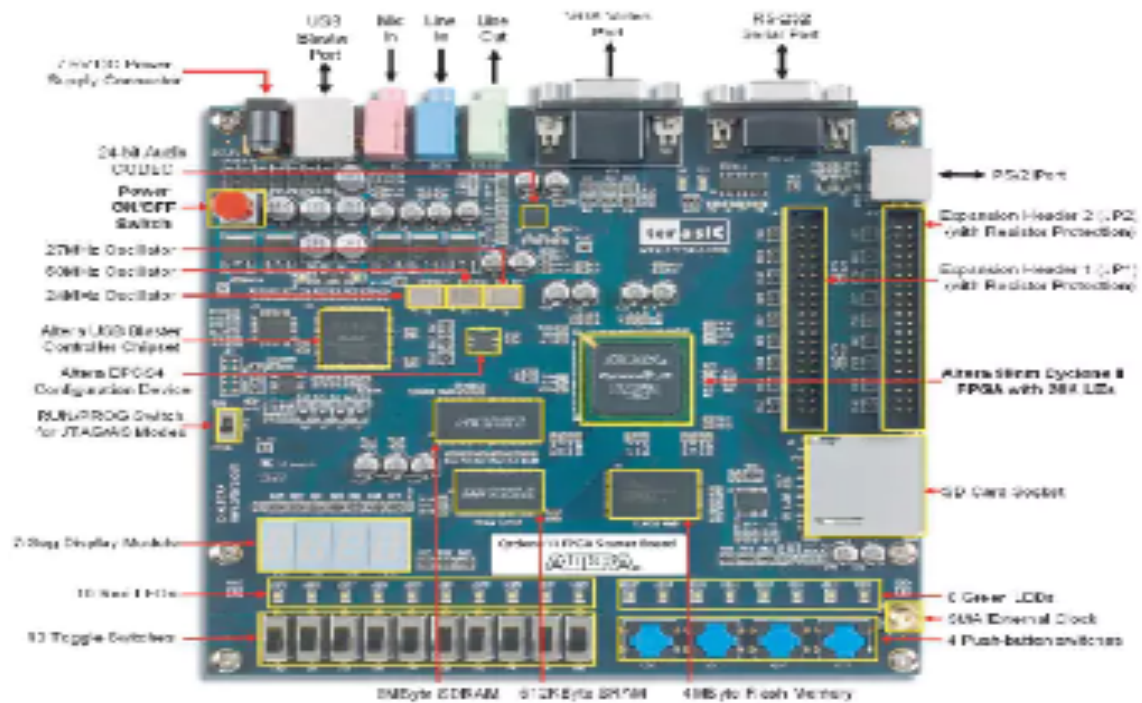


Fig 3.2.1: Cyclone II FPGA Starter Development Kit

### 3.3 Seven Segment Display

The *7-segment display*, also written as “seven segment display”, consists of seven LEDs (hence its name) arranged in a rectangular fashion as shown. Each of the seven LEDs is called a segment because when illuminated the segment forms part of a numerical digit (both Decimal and Hex) to be displayed. An additional 8th LED is sometimes used within the same package thus allowing the indication of a decimal point, (DP) when two or more 7-segment displays are connected together to display numbers greater than ten.

Each one of the seven LEDs in the display is given a positional segment with one of its connection pins being brought straight out of the rectangular plastic package. These individually LED pins are labelled from a through to g representing each individual LED. The other LED pins are connected together and wired to form a common pin.

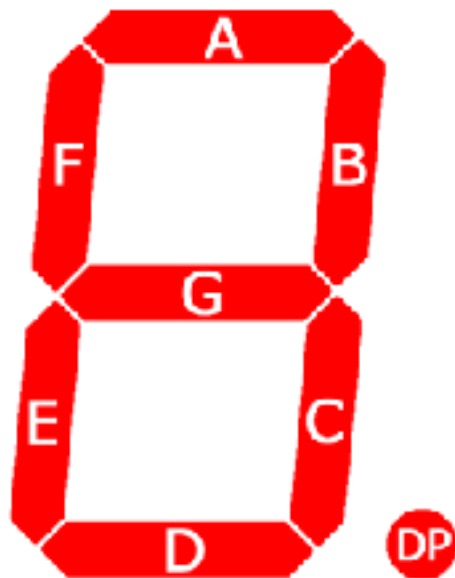


Fig 3.3.1: Seven-Segment Display

By forward biasing the appropriate pins of the LED segments in a particular order, some segments will be light and others will be dark allowing the desired character pattern of the number to be generated on the display. This then allows us to display each of the ten decimal digits 0 through to 9 on the same 7-segment display.

The displays common pin is generally used to identify which type of 7-segment display it is. As each LED has two connecting pins, one called the “Anode” and the other called the “Cathode”, there are therefore two types of LED 7-segment display called: **Common Cathode** (CC) and **Common Anode** (CA).

Decimal Digit	Input lines				Output lines							Display pattern
	A	B	C	D	a	b	c	d	e	f	g	
0	0	0	0	0	1	1	1	1	1	1	0	0
1	0	0	0	1	0	1	1	0	0	0	0	1
2	0	0	1	0	1	1	0	1	1	0	1	2
3	0	0	1	1	1	1	1	1	0	0	1	3
4	0	1	0	0	0	1	1	0	0	1	1	4
5	0	1	0	1	1	0	1	1	0	1	1	5
6	0	1	1	0	1	0	1	1	1	1	1	6
7	0	1	1	1	1	1	1	0	0	0	0	7
8	1	0	0	0	1	1	1	1	1	1	1	8
9	1	0	0	1	1	1	1	1	0	1	1	9

Table 3.3.1: Seven segment Display Truth table

## CHAPTER 4

## SIMULATION RESULTS

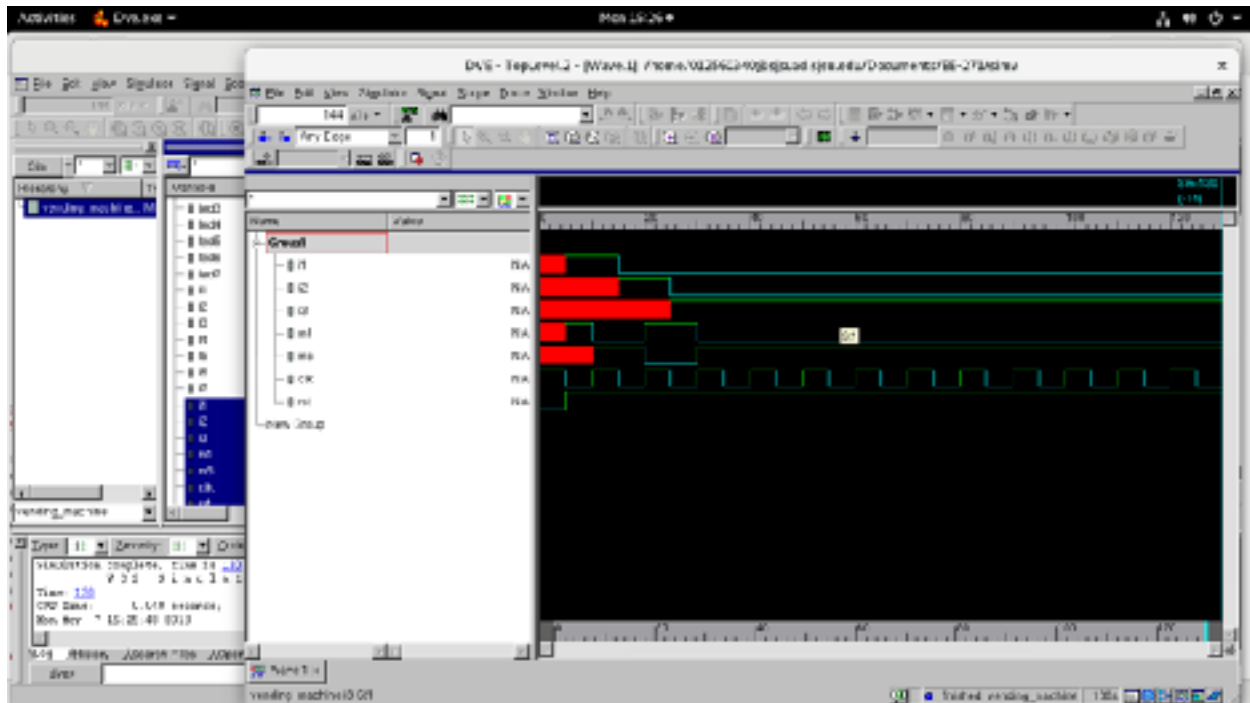


Fig 4.1 Waveform

The simulation is performed using Synopsys VCS based on the design discussed above.

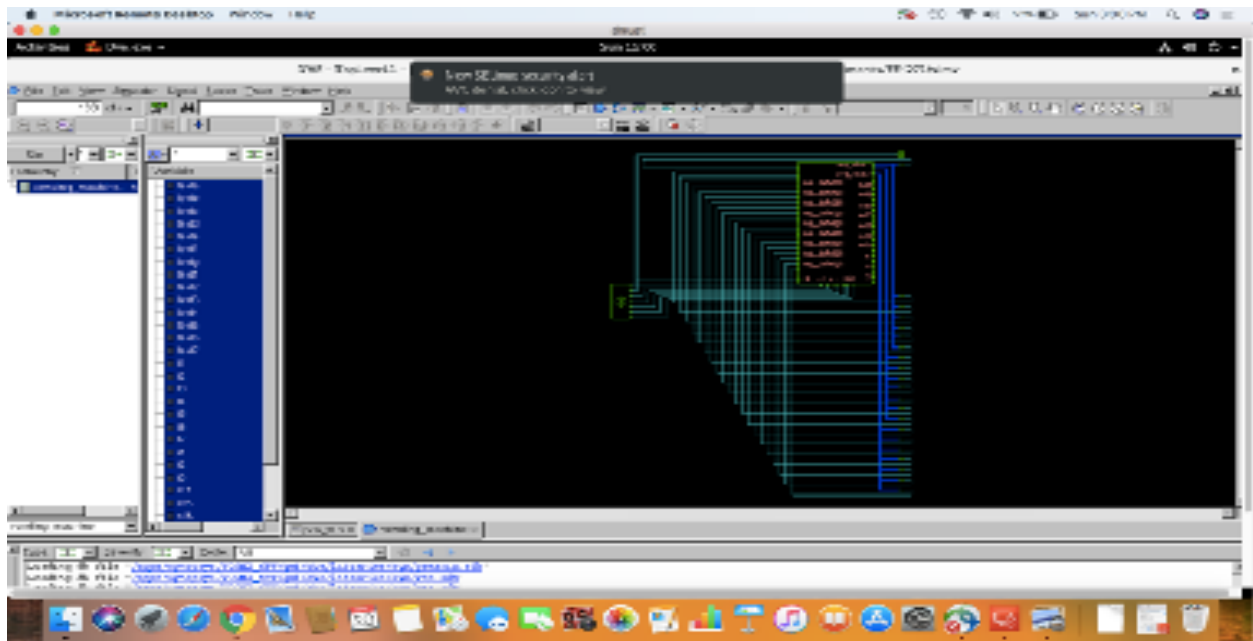


Fig 4.2 Schematic View

## **CHAPTER 5**

### **CONCLUSION**

- In this project, we achieved FPGA based vending machine, which is flexible and reprogrammable.
- The design can also be extended to as many number of selections as desired.
- This vending machine can work all around the clock which reduces time and labor force.
- This vending machine is designed to be user friendly.

## CHAPTER 6

### REFERENCES

- Wikipedia: Vending Machine [https://en.wikipedia.org/wiki/Vending\\_machine](https://en.wikipedia.org/wiki/Vending_machine)
- B Jyothi, I. Sarah 2, A. Srinivas, "Implementation of FPGA Based Smart Vending Machine", International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 NATIONAL CONFERENCE on Developments, Advances & Trends in Engineering Sciences (NCDATES- 09th & 10th January 2015)
- Seven Segment Display  
<https://www.electronics-tutorials.ws/blog/7-segment-display-tutorial.html>