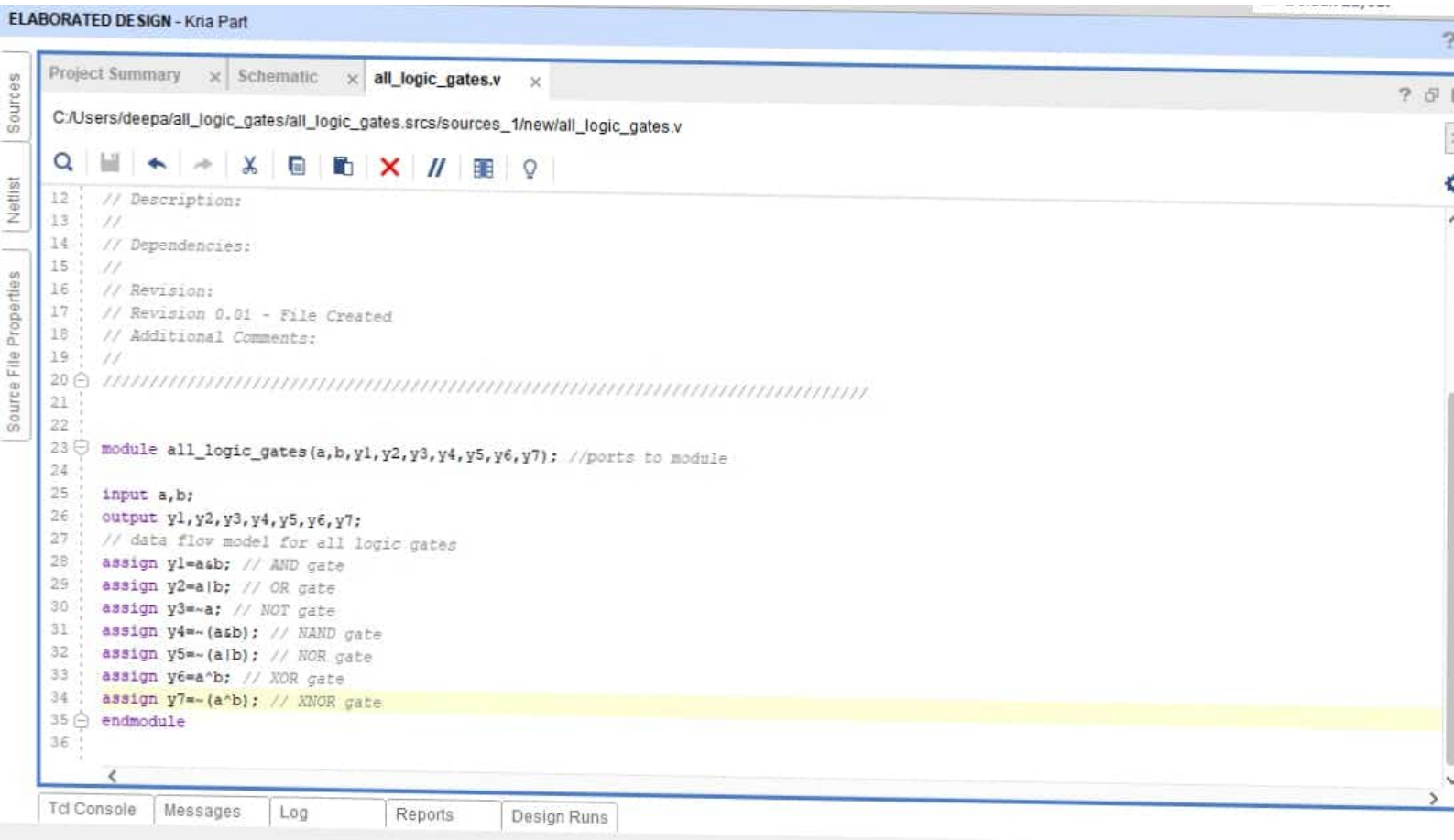
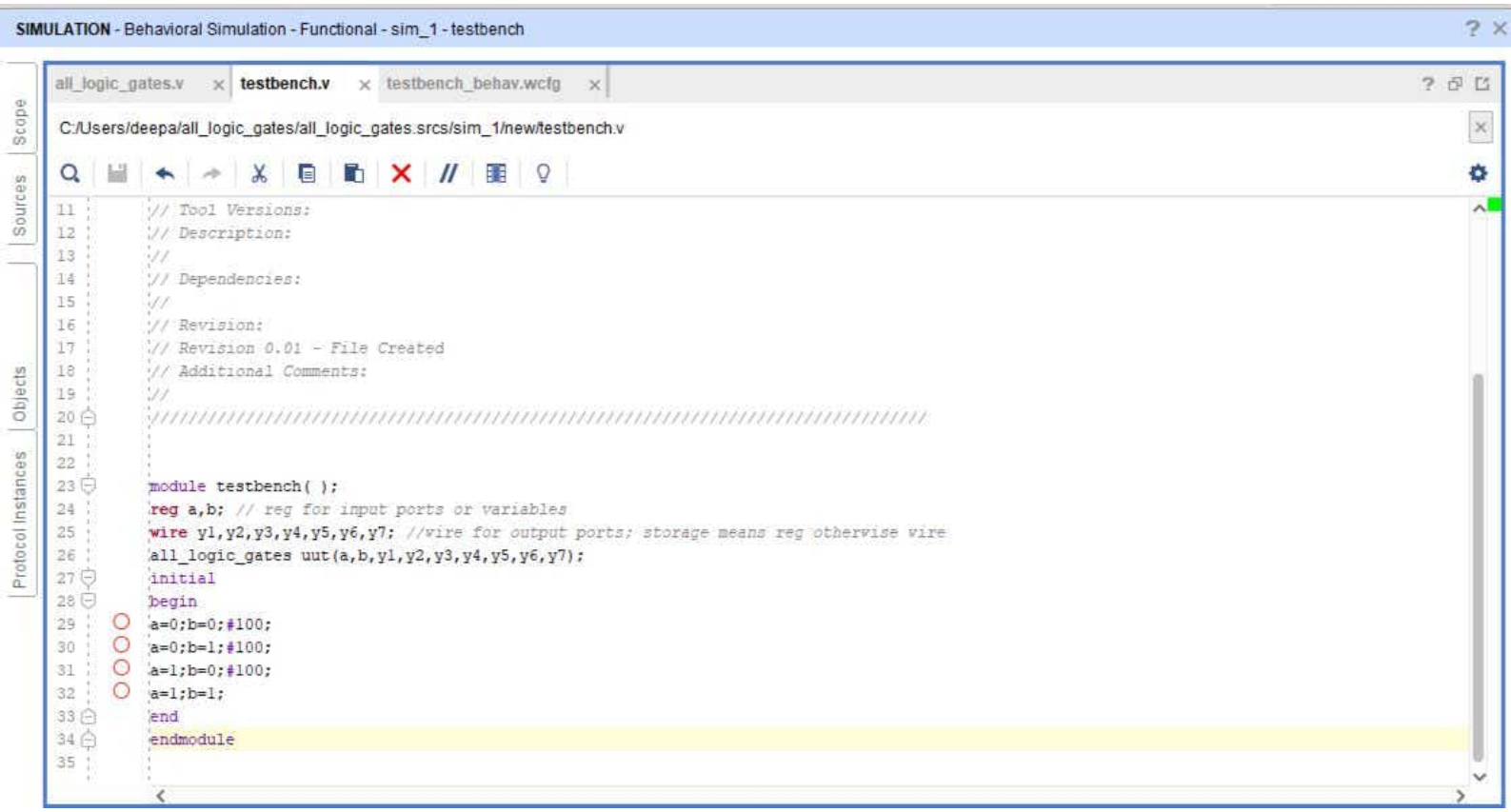
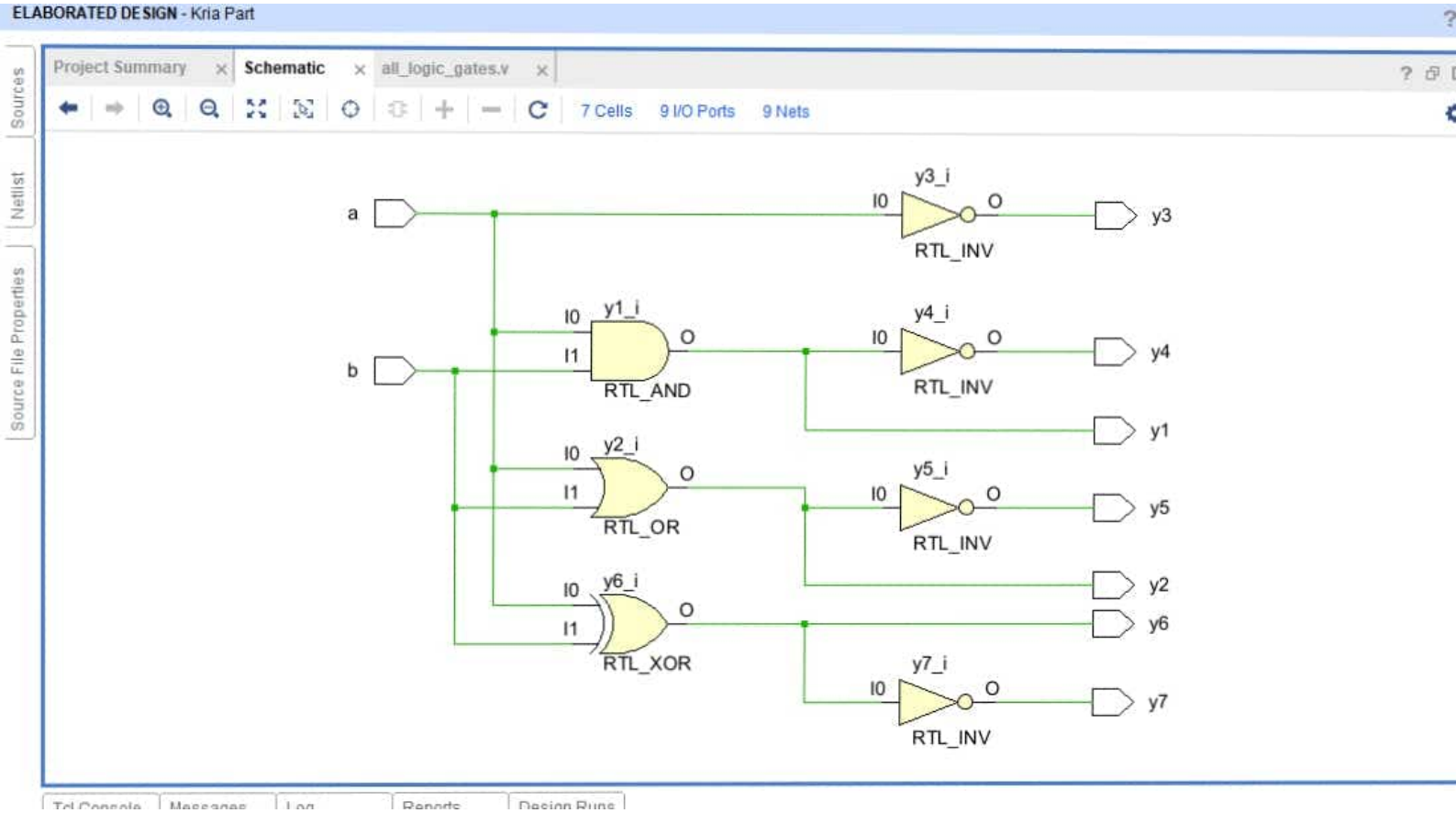
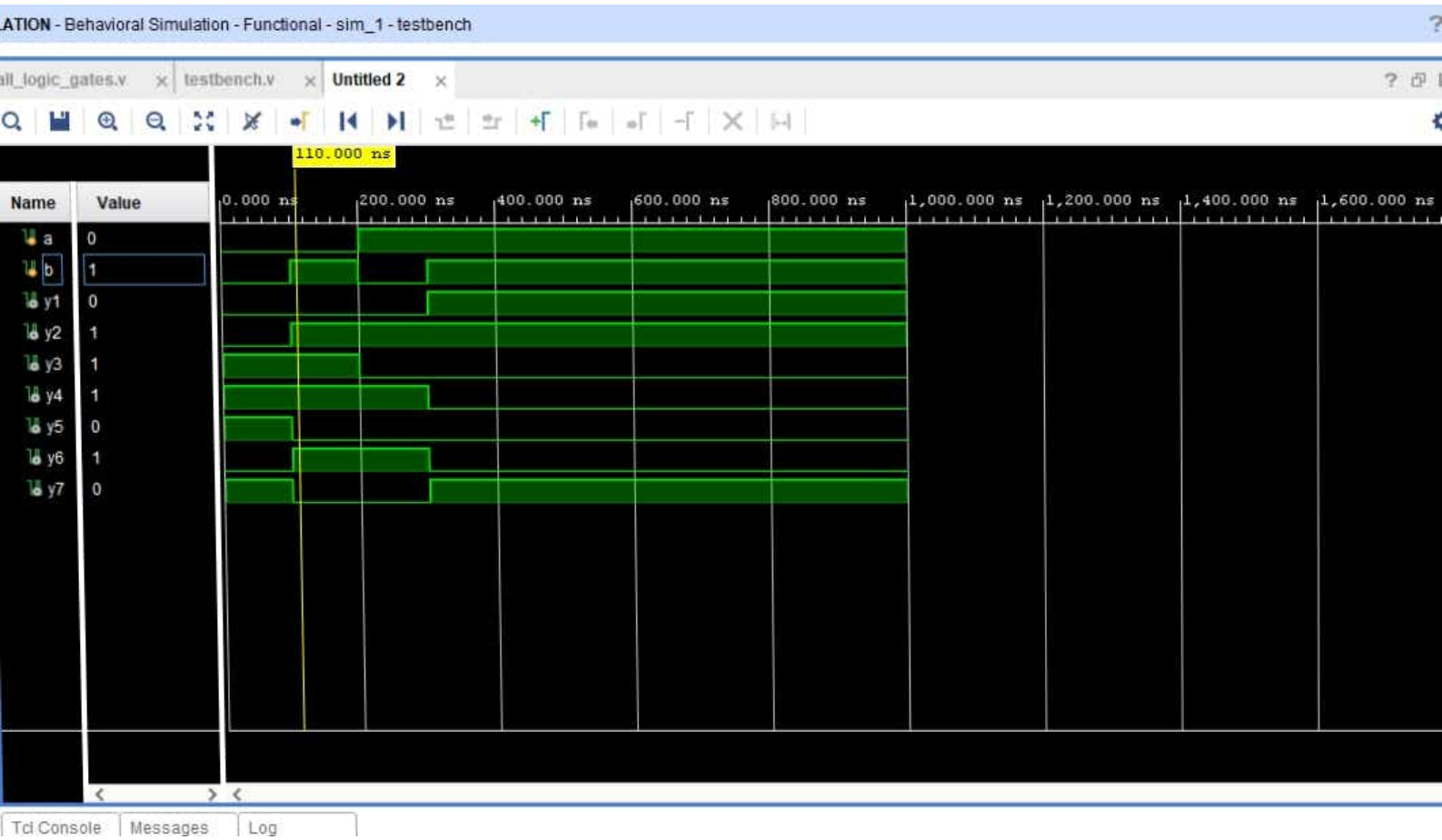
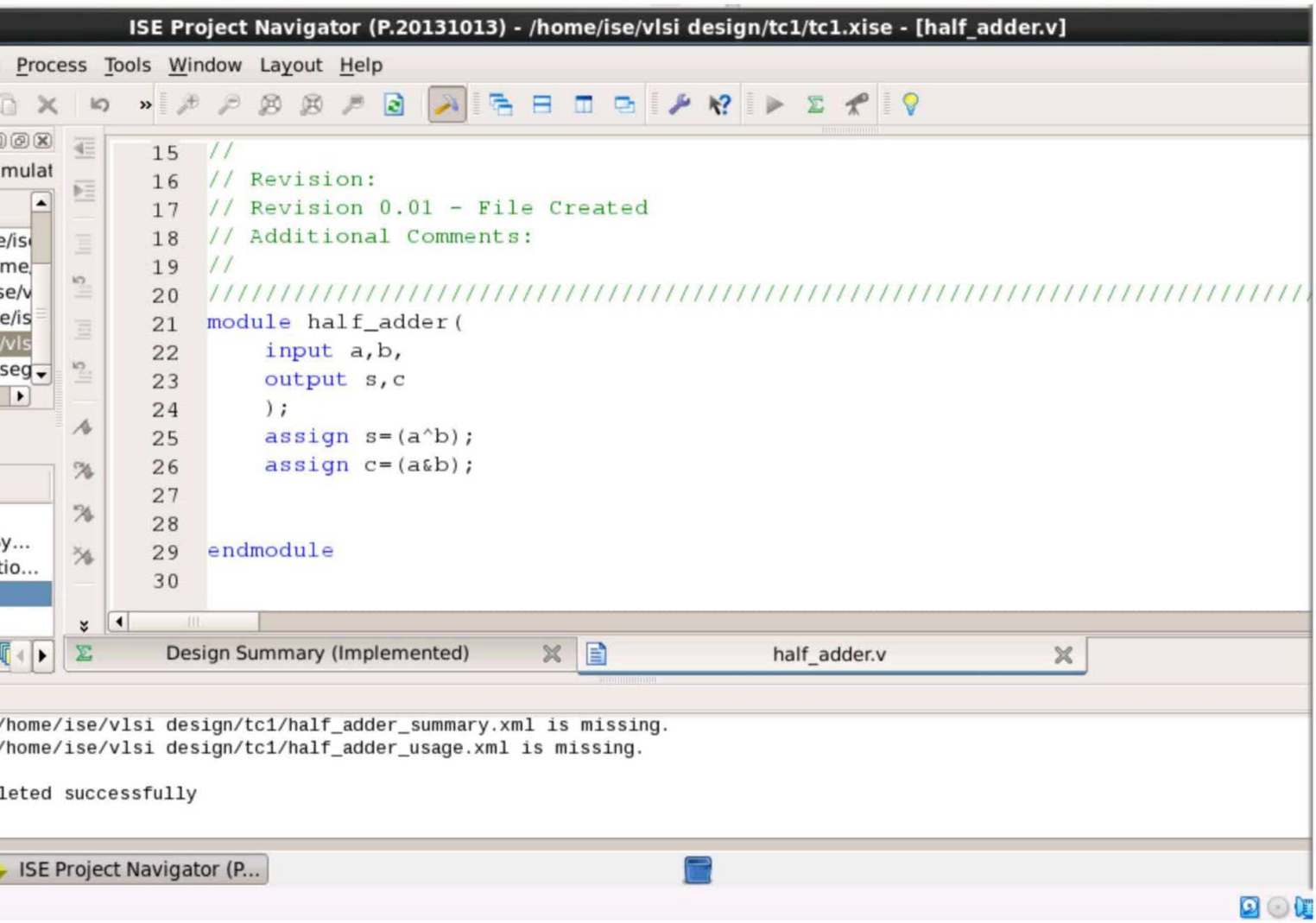

ELABORATED DESIGN - Kria Part
Project Summary
Schematic
all_logic_gates.v
C:/Users/deepa/all_logic_gates/all_logic_gates.srcs/sources_1/new/all_logic_gates.v
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//
module all_logic_gates(a,b,y1,y2,y3,y4,y5,y6,y7); //ports to module
input a,b;
output y1,y2,y3,y4,y5,y6,y7;
// data flow model for all logic gates
assign y1=a&b; // AND gate
assign y2=a|b; // OR gate
assign y3=~a; // NOT gate
assign y4=~(a&b); // NAND gate
assign y5=~(a|b); // NOR gate
assign y6=a^b; // XOR gate
assign y7=~(a^b); // XNOR gate
endmodule
Tcl Console
Messages
Log
Reports
Design Runs
Sources
Netlist
Source File Properties


SIMULATION - Behavioral Simulation - Functional - sim_1 - testbench
Scope
Sources
Objects
Protocol Instances
all_logic_gates.v
testbench.v
testbench_behav.wcfg
C:/Users/deepa/all_logic_gates/all_logic_gates.srcs/sim_1/new/testbench.v
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//
module testbench( );
reg a,b; // reg for input ports or variables
wire y1,y2,y3,y4,y5,y6,y7; //wire for output ports; storage means reg otherwise wire
all_logic_gates uut(a,b,y1,y2,y3,y4,y5,y6,y7);
initial
begin
a=0;b=0;#100;
a=0;b=1;#100;
a=1;b=0;#100;
a=1;b=1;
end
endmodule

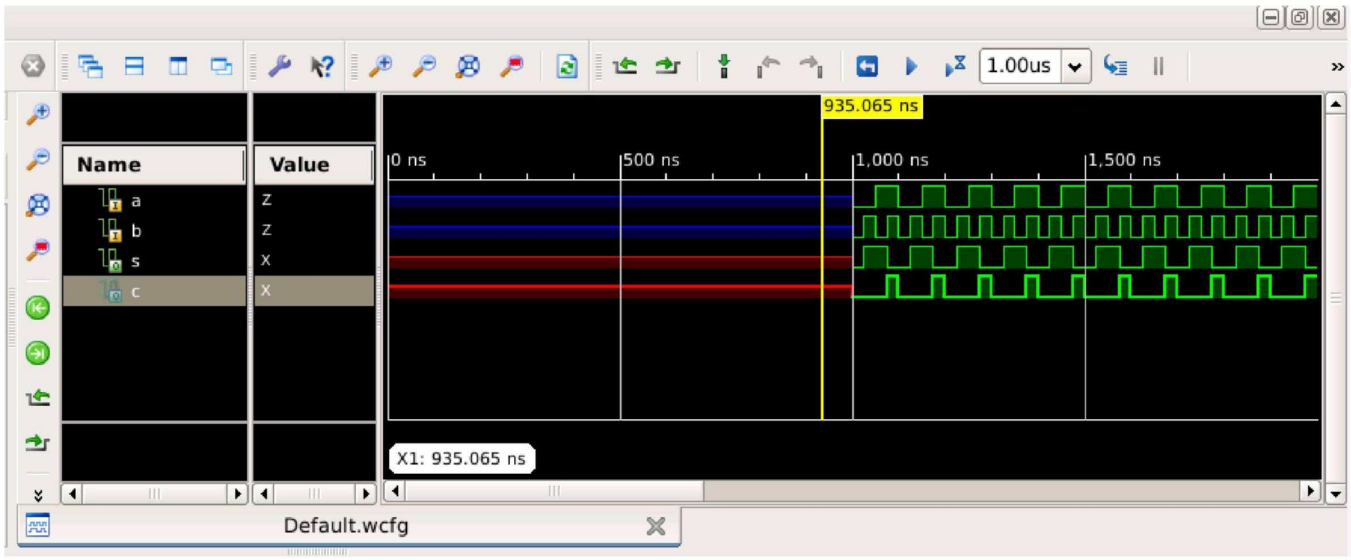

ELABORATED DESIGN - Kria Part
Project Summary
Schematic
all_logic_gates.v
7 Cells
9 I/O Ports
9 Nets
Sources
Netlist
Source File Properties
a
b
y3_i
I0
O
RTL_INV
y3
y1_i
I0
I1
RTL_AND
y4_i
y4
y1
y2_i
RTL_OR
y5_i
y5
y2
y6_i
RTL_XOR
y6
y7_i
y7


LATION - Behavioral Simulation - Functional - sim_1 - testbench
ll_logic_gates.v
testbench.v
Untitled 2
110.000 ns
Name
Value
a
b
y1
y2
y3
y4
y5
y6
y7
0
1
0
1
1
1
0
1
0
0.000 ns
200.000 ns
400.000 ns
600.000 ns
800.000 ns
1,000.000 ns
1,200.000 ns
1,400.000 ns
1,600.000 ns
Tcl Console
Messages
Log

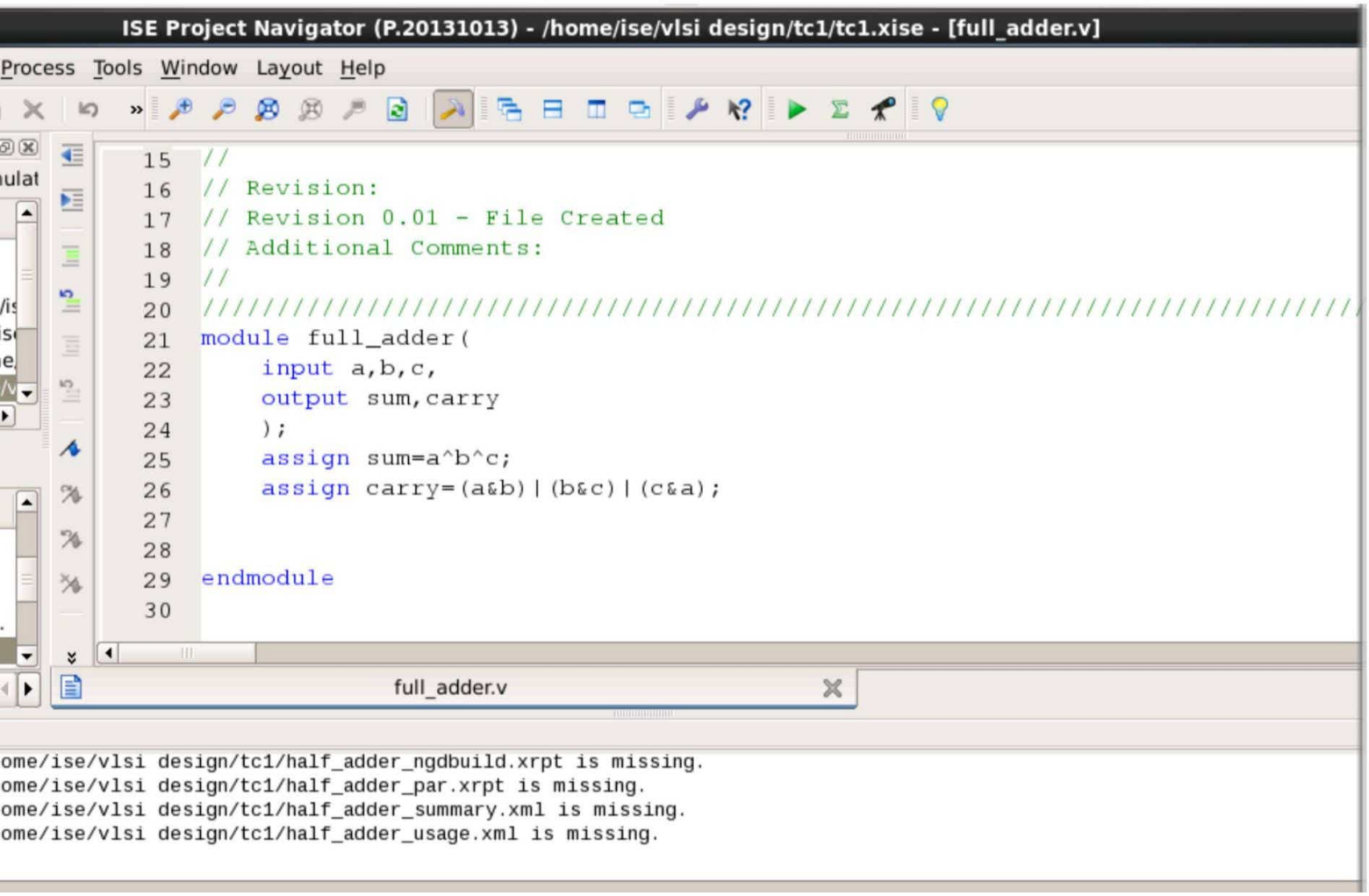
HALF ADDER


ISE Project Navigator (P.20131013) - /home/ise/vlsi design/tc1/tc1.xise - [half_adder.v]
Process Tools Window Layout Help
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //
21 module half_adder(
22 input a,b,
23 output s,c
24);
25 assign s=(a^b);
26 assign c=(a&b);
27
28
29 endmodule
30
Design Summary (Implemented)
half_adder.v
/home/ise/vlsi design/tc1/half_adder_summary.xml is missing.
/home/ise/vlsi design/tc1/half_adder_usage.xml is missing.
leted successfully
ISE Project Navigator (P...

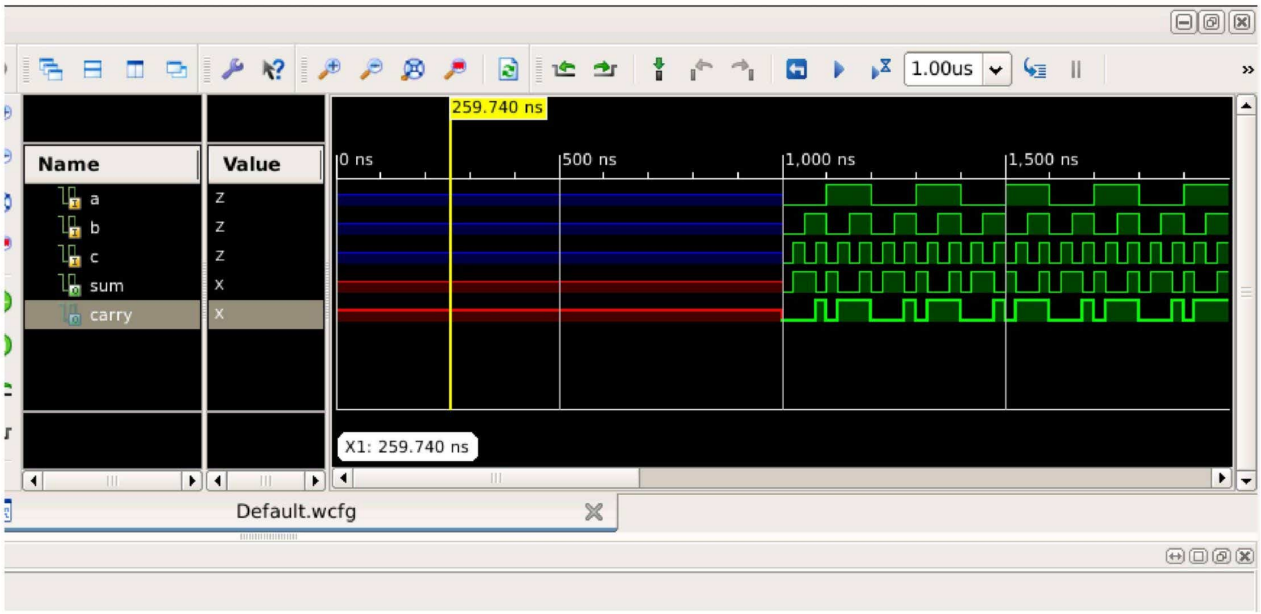
HALF ADDER


1.00us
935.065 ns
Name
Value
a
b
s
c
Z
Z
X
X
0 ns
500 ns
1,000 ns
1,500 ns
X1: 935.065 ns
Default.wcfg

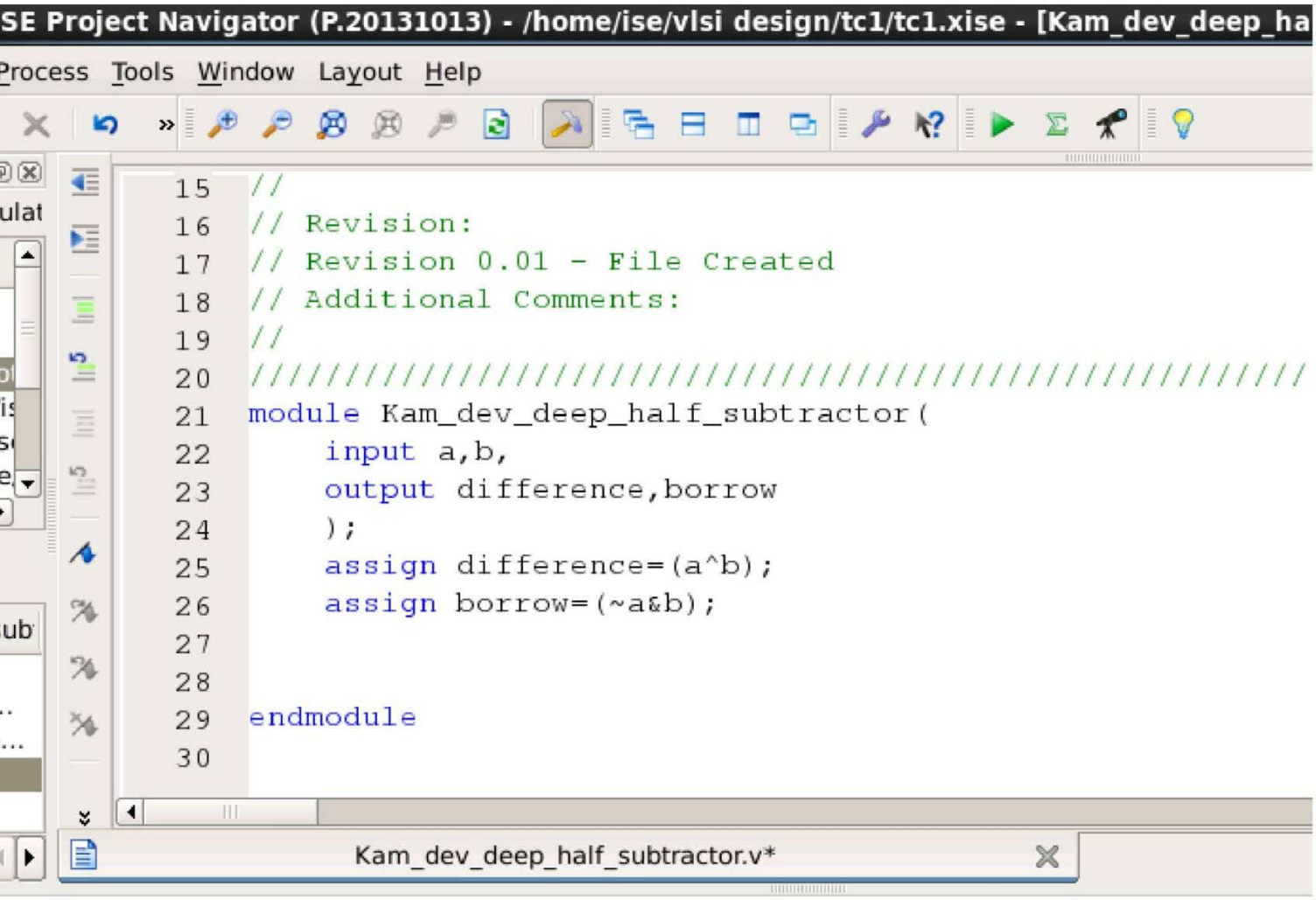
FULL ADDER


ISE Project Navigator (P.20131013) - /home/ise/vlsi design/tc1/tc1.xise - [full_adder.v]
Process Tools Window Layout Help
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //
21 module full_adder(
22 input a,b,c,
23 output sum,carry
24);
25 assign sum=a^b^c;
26 assign carry=(a&b)|(b&c)|(c&a);
27
28
29 endmodule
30
full_adder.v
ome/ise/vlsi design/tc1/half_adder_ngdbuild.xrpt is missing.
ome/ise/vlsi design/tc1/half_adder_par.xrpt is missing.
ome/ise/vlsi design/tc1/half_adder_summary.xml is missing.
ome/ise/vlsi design/tc1/half_adder_usage.xml is missing.

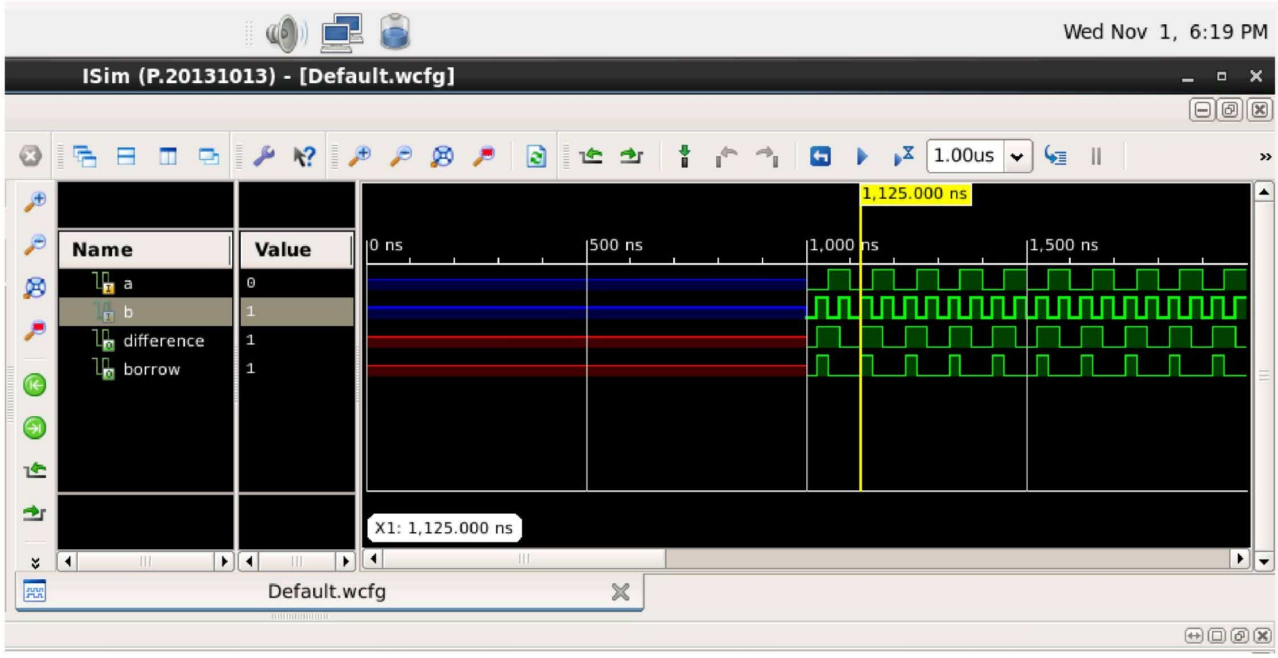
FULL ADDER


1.00us
259.740 ns
Name
Value
a
b
c
sum
carry
z
z
z
x
x
0 ns
500 ns
1,000 ns
1,500 ns
X1: 259.740 ns
Default.wcfg

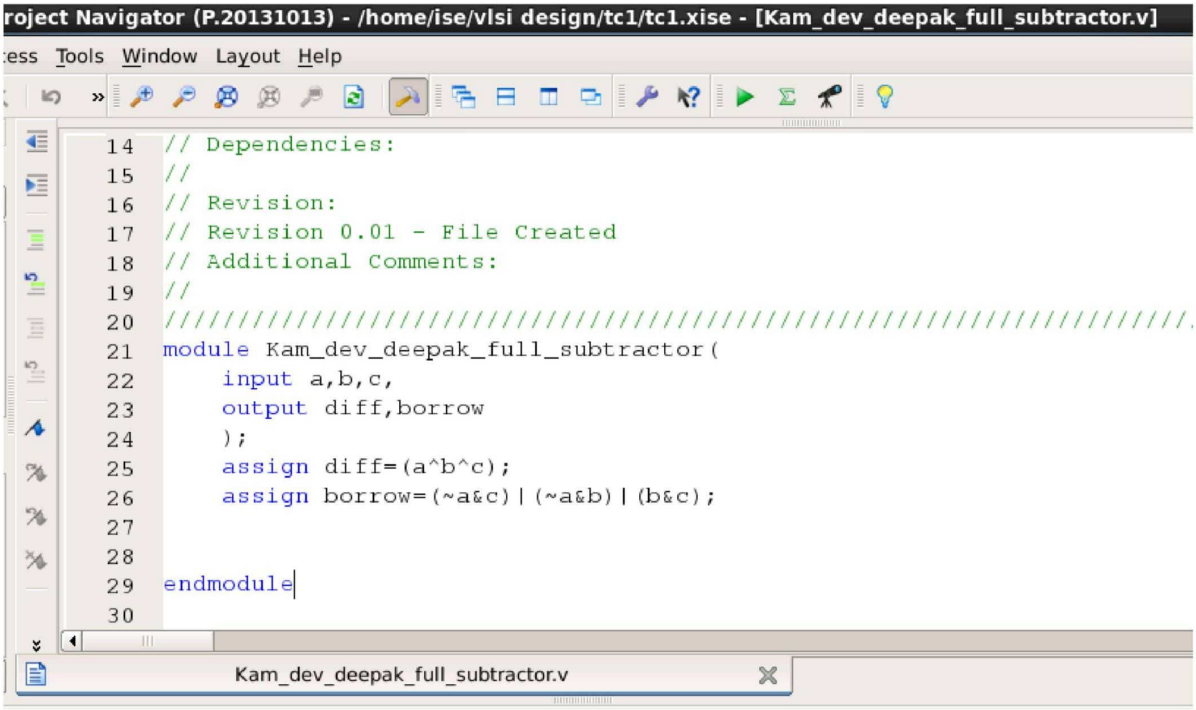
HALF SUBTRACTOR



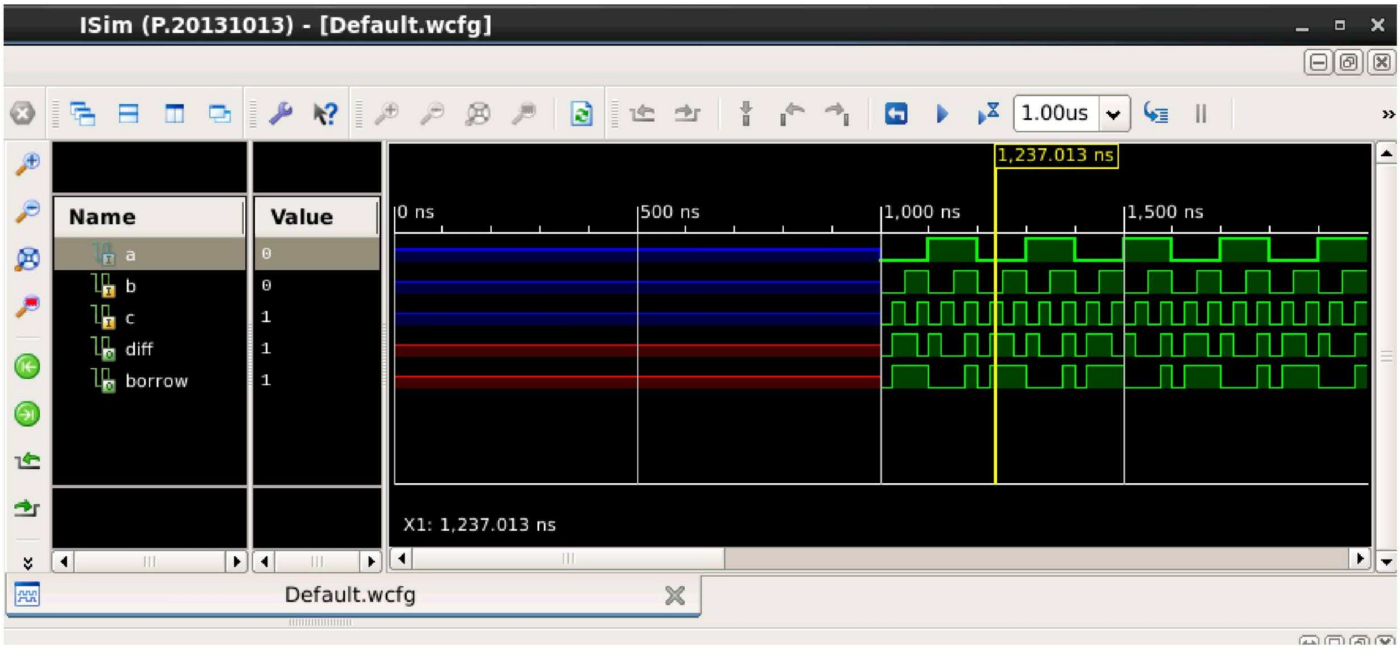
HALF SUBTRACTOR



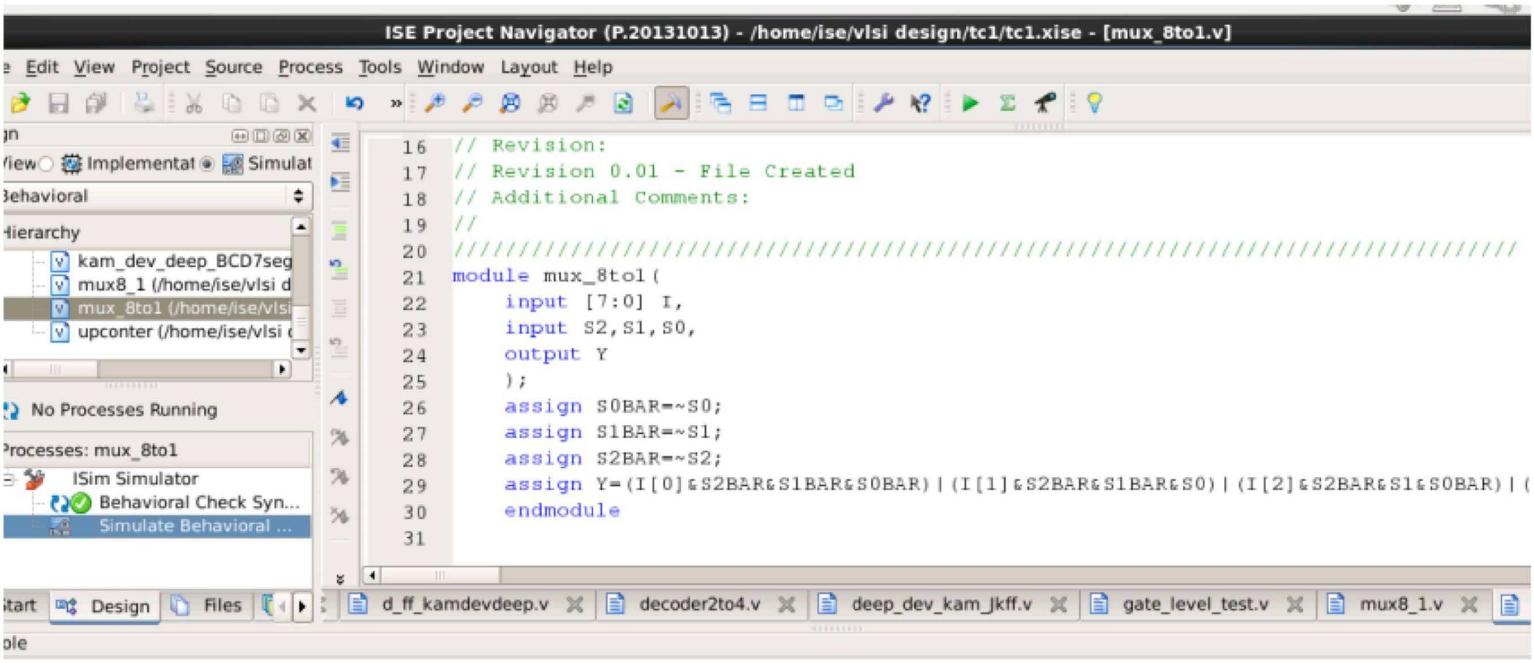
FULL SUBTRACTOR



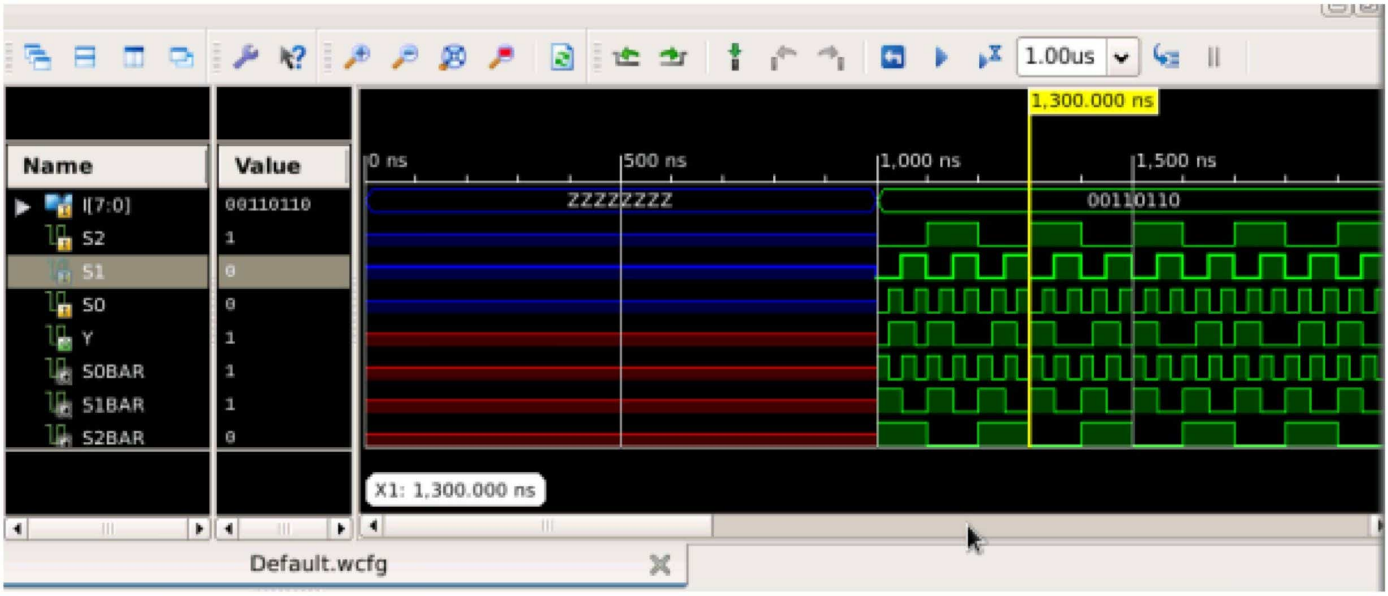
FULL SUBTRACTOR



MUX 8*1


ISE Project Navigator (P.20131013) - /home/ise/vlsi design/tc1/tc1.xise - [mux_8to1.v]
Edit View Project Source Process Tools Window Layout Help
Implementat
Simulat
Behavioral
Hierarchy
kam_dev_deep_BCD7seg
mux8_1 (/home/ise/vlsi d
mux_8to1 (/home/ise/vlsi
upconter (/home/ise/vlsi
No Processes Running
Processes: mux_8to1
ISim Simulator
Behavioral Check Syn...
Simulate Behavioral ...
Design
Files
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //
21 module mux_8to1(
22 input [7:0] I,
23 input S2,S1,S0,
24 output Y
25);
26 assign S0BAR=~S0;
27 assign S1BAR=~S1;
28 assign S2BAR=~S2;
29 assign Y=(I[0]&S2BAR&S1BAR&S0BAR)|(I[1]&S2BAR&S1BAR&S0)|(I[2]&S2BAR&S1&S0BAR)|(
30 endmodule
31
d_ff_kamdevdeep.v
decoder2to4.v
deep_dev_kam_jkff.v
gate_level_test.v
mux8_1.v

MUX 8*1


1.00us
1,300.000 ns
Name
Value
0 ns
500 ns
1,000 ns
1,500 ns
I[7:0]
00110110
ZZZZZZZZ
00110110
S2
1
S1
0
S0
0
Y
1
S0BAR
1
S1BAR
1
S2BAR
0
X1: 1,300.000 ns
Default.wcfg