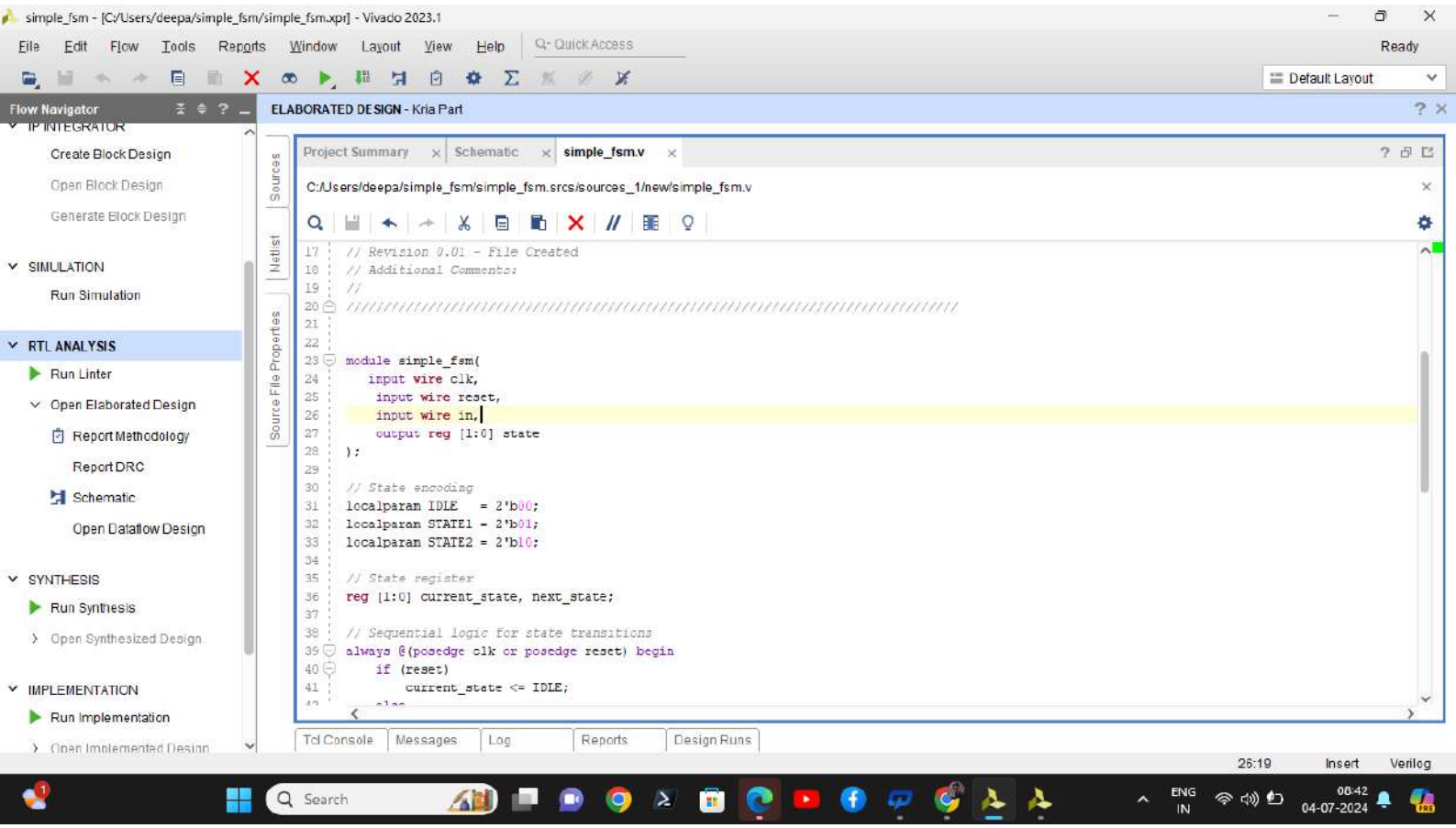
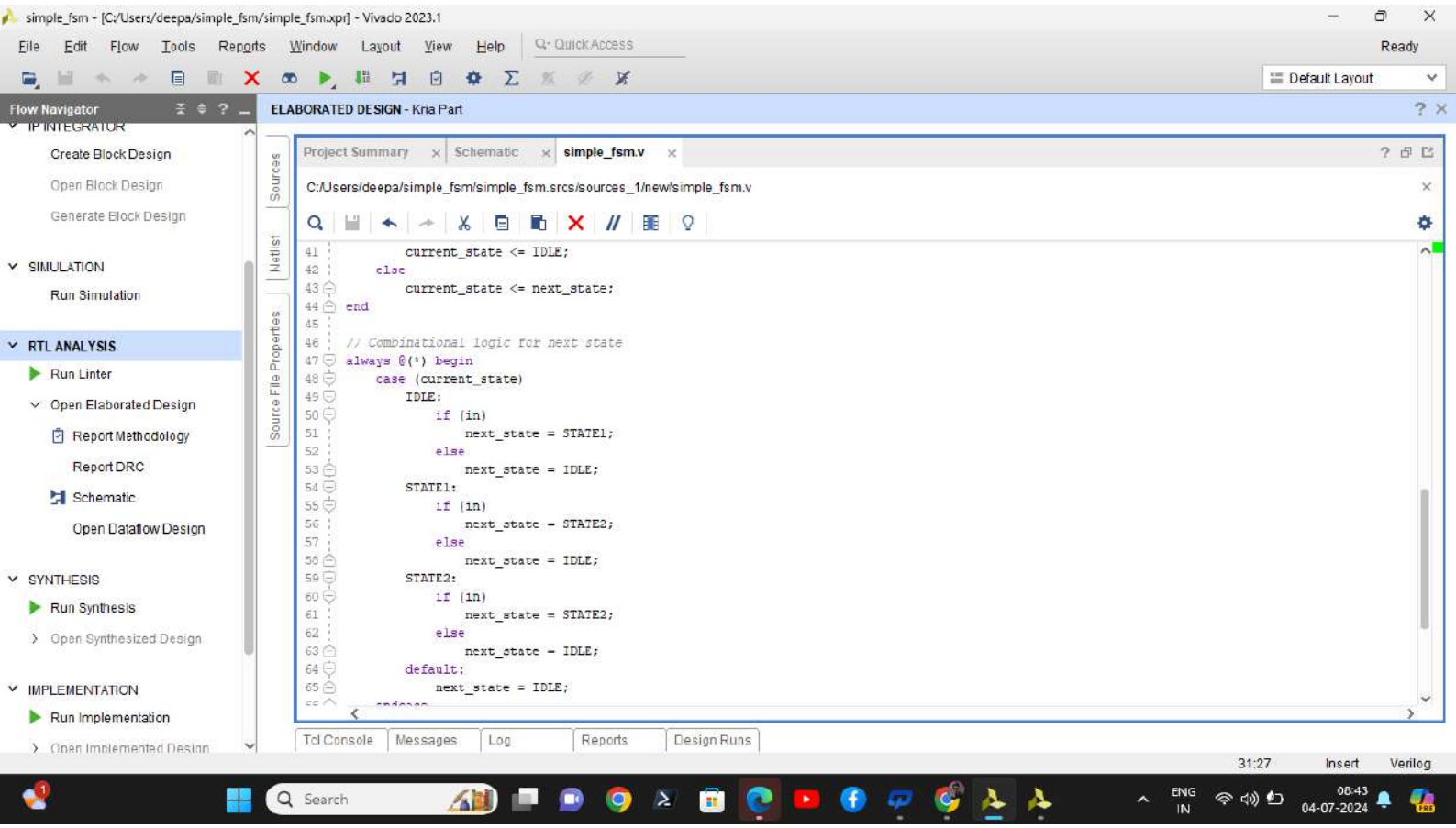
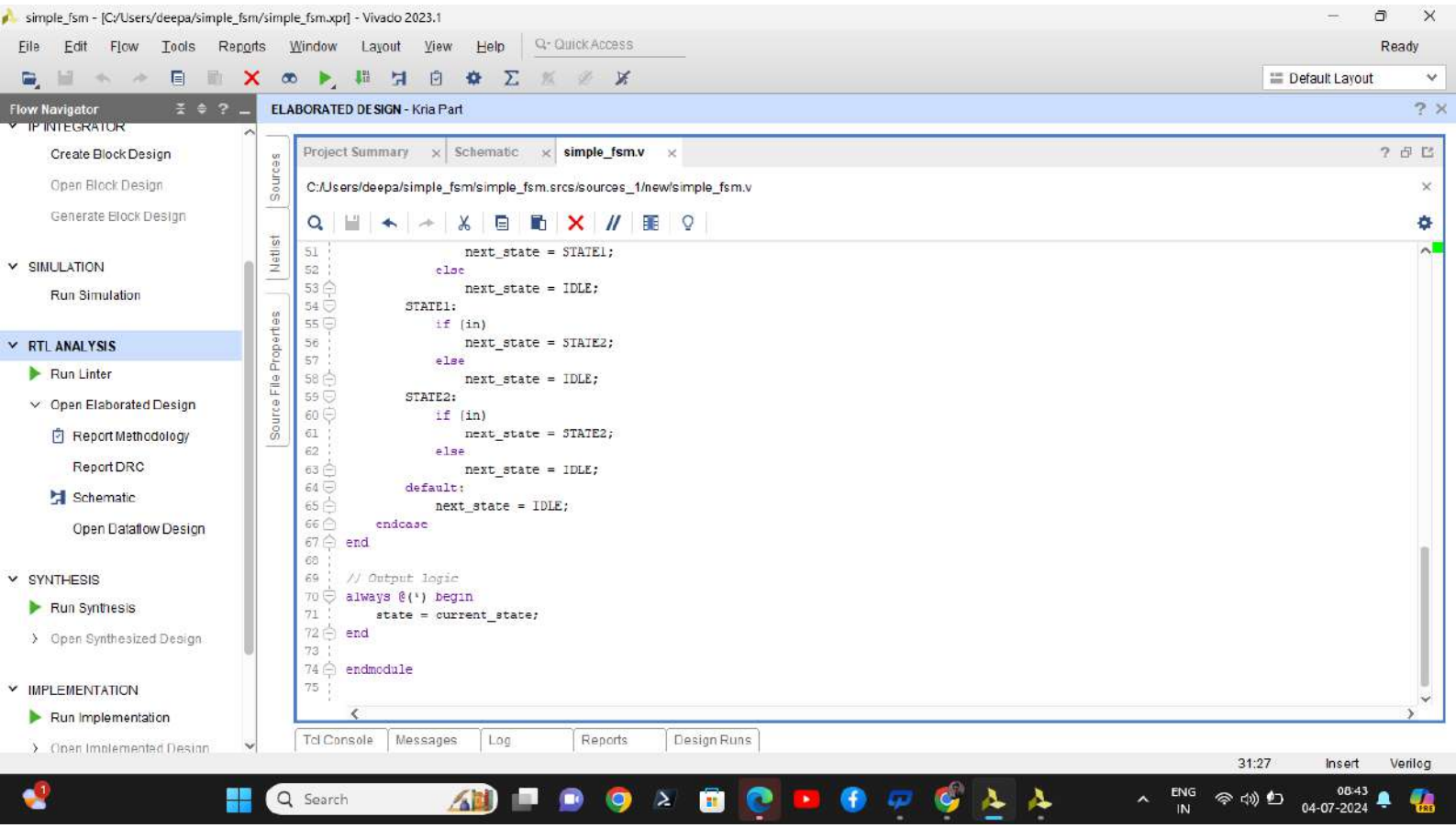
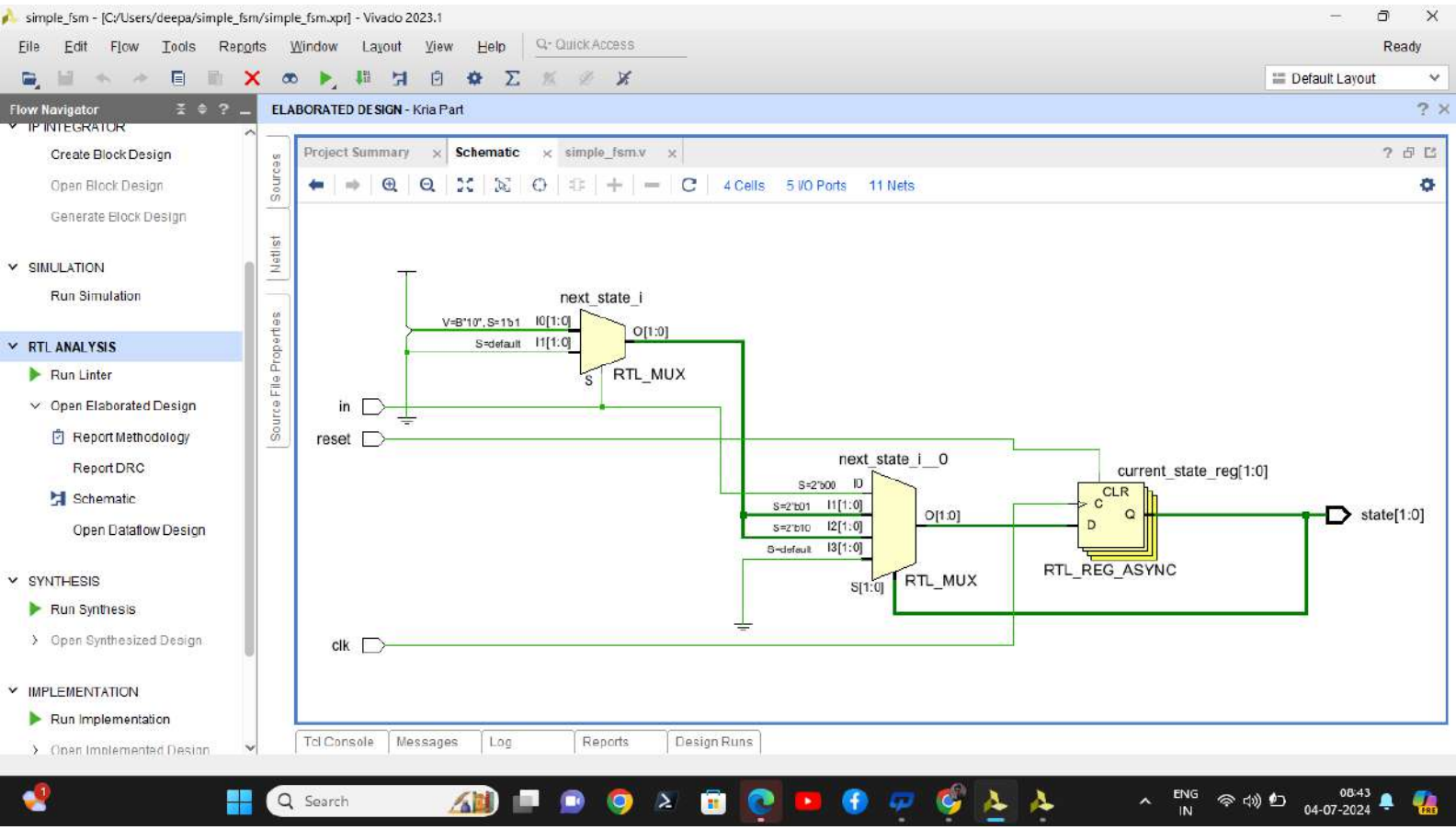
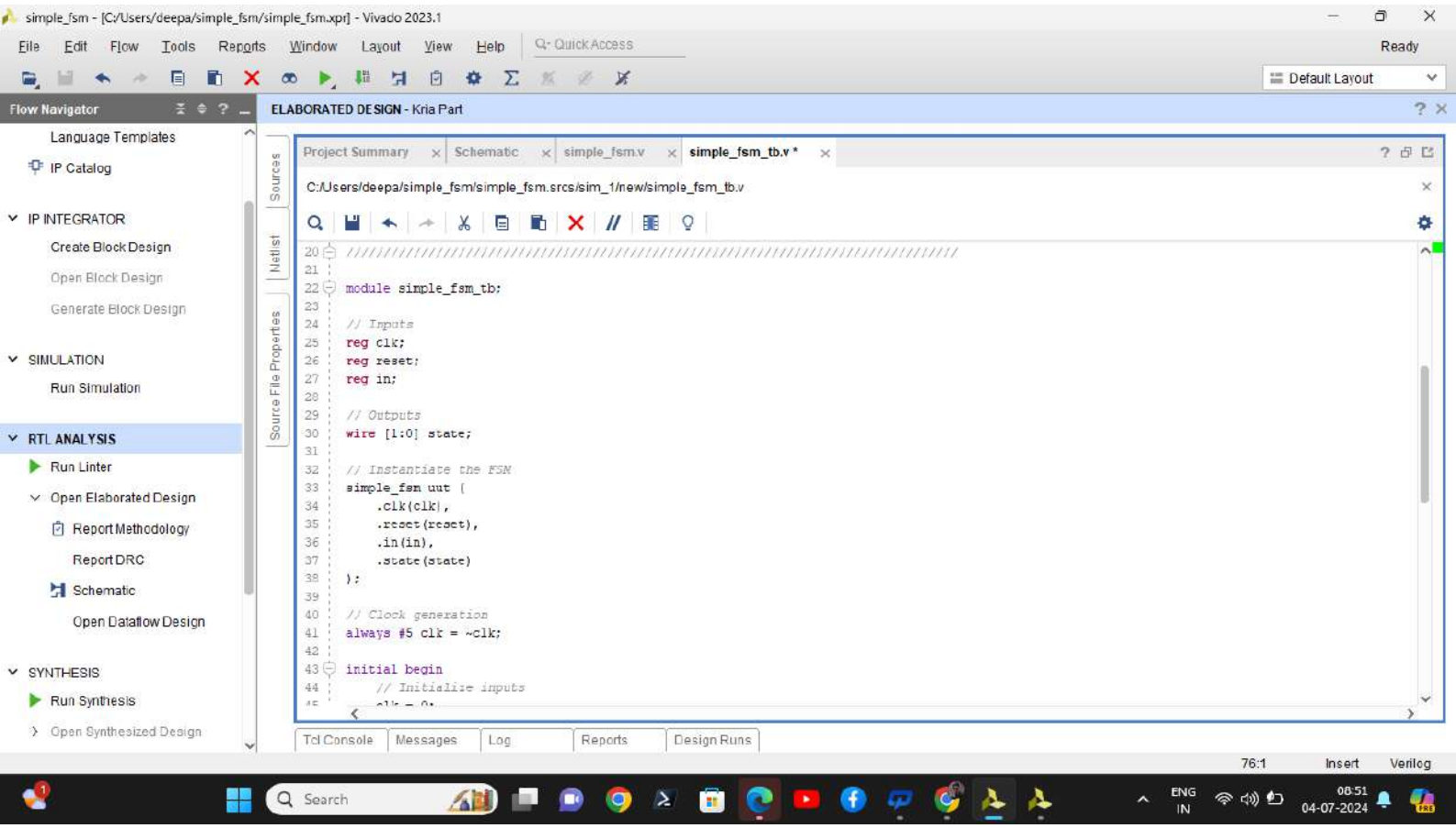
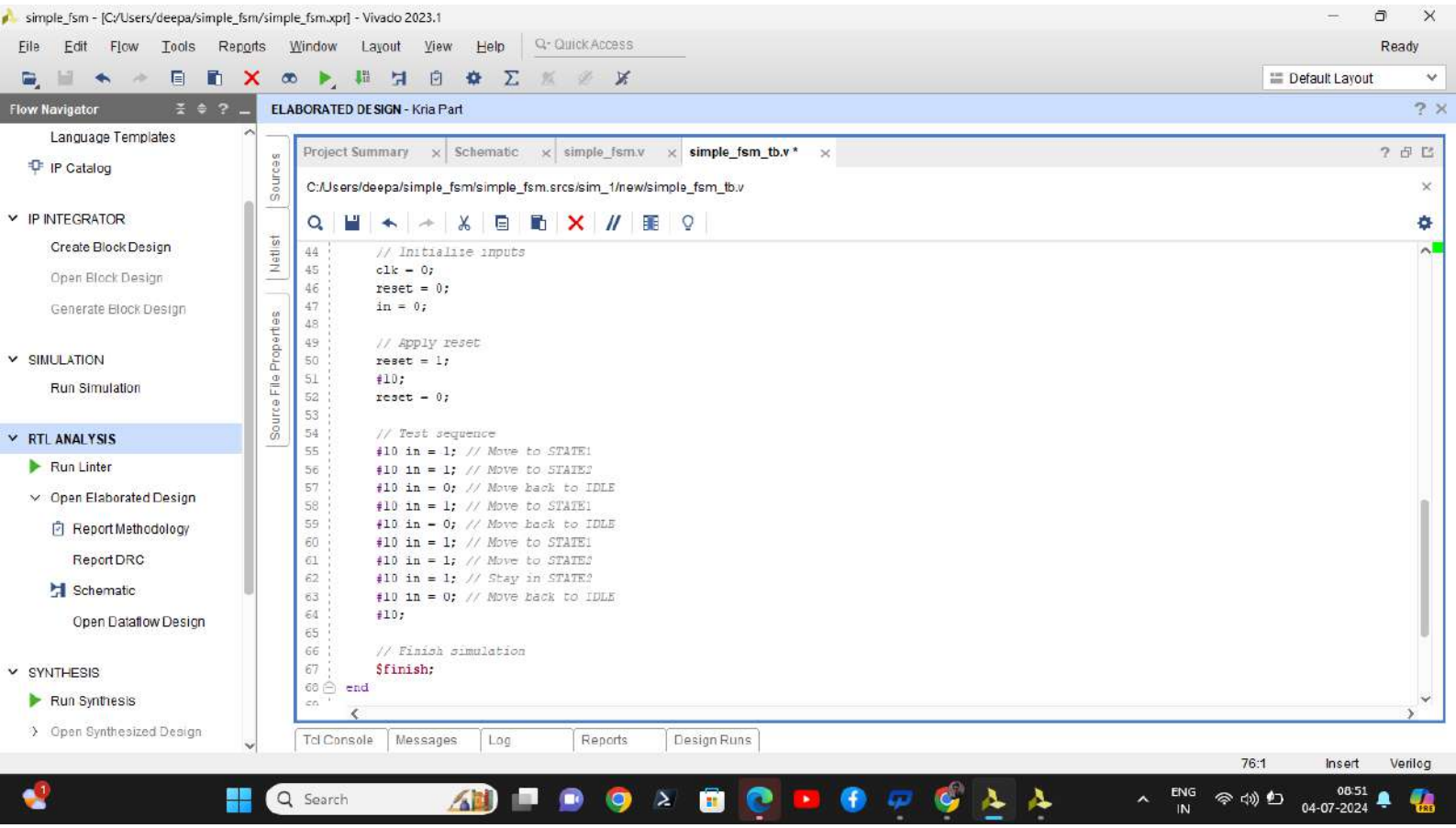

simple_fsm - [C:/Users/deepa/simple_fsm/simple_fsm.xpr] - Vivado 2023.1
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Ready
Default Layout
Flow Navigator
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Run Linter
Open Elaborated Design
Report Methodology
Report DRC
Schematic
Open Dataflow Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
ELABORATED DESIGN - Kria Part
Project Summary
Schematic
simple_fsm.v
C:/Users/deepa/simple_fsm/simple_fsm.srcs/sources_1/new/simple_fsm.v
Sources
Netlist
Source File Properties
// Revision 0.01 - File Created
// Additional Comments:
//
//
module simple_fsm(
input wire clk,
input wire reset,
input wire in,
output reg [1:0] state
);
// State encoding
localparam IDLE = 2'b00;
localparam STATE1 = 2'b01;
localparam STATE2 = 2'b10;
// State register
reg [1:0] current_state, next_state;
// Sequential logic for state transitions
always @(posedge clk or posedge reset) begin
if (reset)
current_state <= IDLE;
Tcl Console
Messages
Log
Reports
Design Runs
26:19
Insert
Verilog
Search
ENG
IN
08:42
04-07-2024

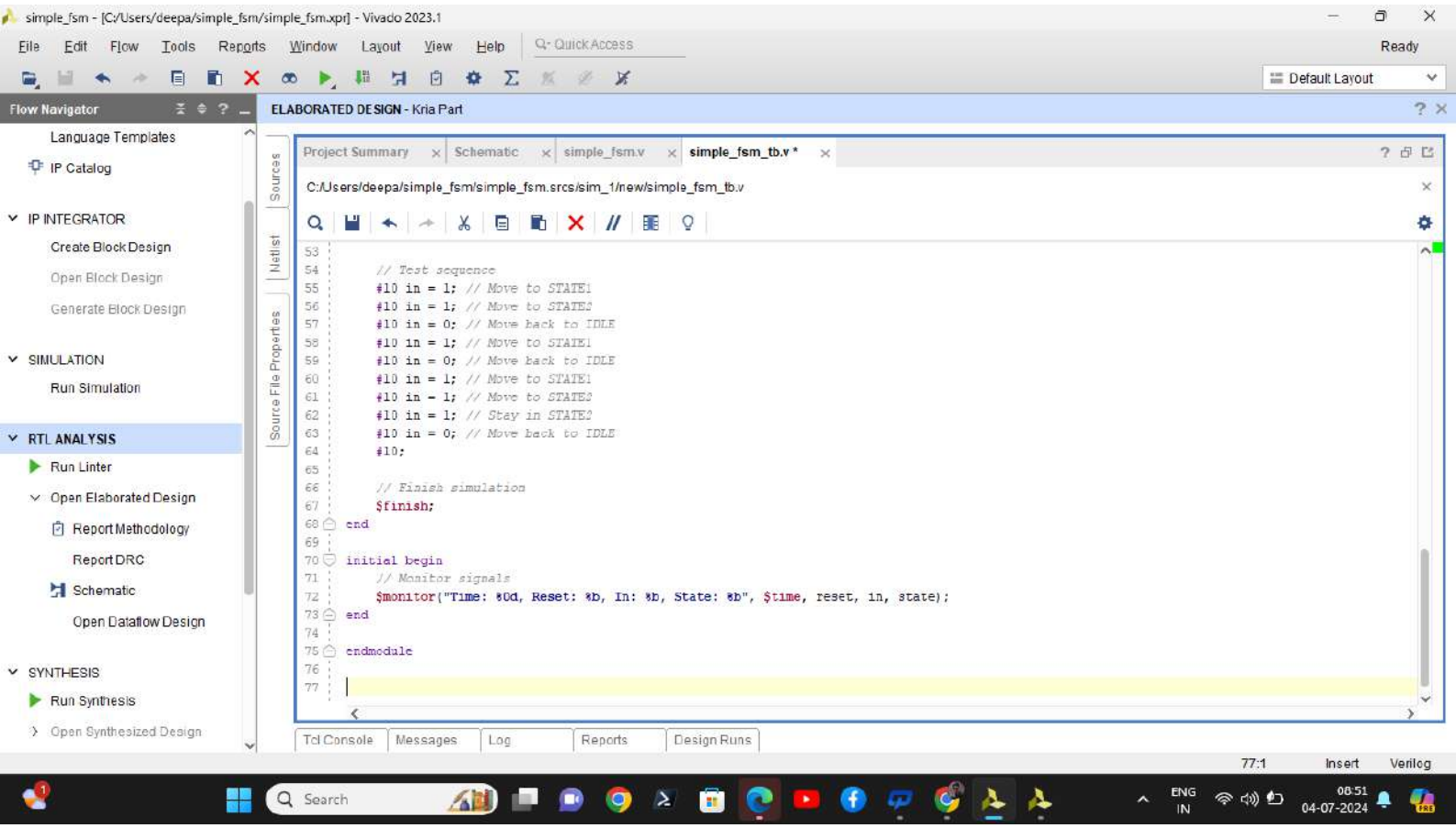

simple_fsm - [C:/Users/deepa/simple_fsm/simple_fsm.xpr] - Vivado 2023.1
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Ready
Default Layout
Flow Navigator
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Run Linter
Open Elaborated Design
Report Methodology
Report DRC
Schematic
Open Dataflow Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
ELABORATED DESIGN - Kria Part
Project Summary
Schematic
simple_fsm.v
C:/Users/deepa/simple_fsm/simple_fsm.srcs/sources_1/new/simple_fsm.v
Sources
Netlist
Source File Properties
41 current_state <= IDLE;
42 else
43 current_state <= next_state;
44 end
45
46 // Combinational logic for next state
47 always @(*) begin
48 case (current_state)
49 IDLE:
50 if (in)
51 next_state = STATE1;
52 else
53 next_state = IDLE;
54 STATE1:
55 if (in)
56 next_state = STATE2;
57 else
58 next_state = IDLE;
59 STATE2:
60 if (in)
61 next_state = STATE2;
62 else
63 next_state = IDLE;
64 default:
65 next_state = IDLE;
Tcl Console
Messages
Log
Reports
Design Runs
31:27
Insert
Verilog
Search
ENG
IN
08:43
04-07-2024

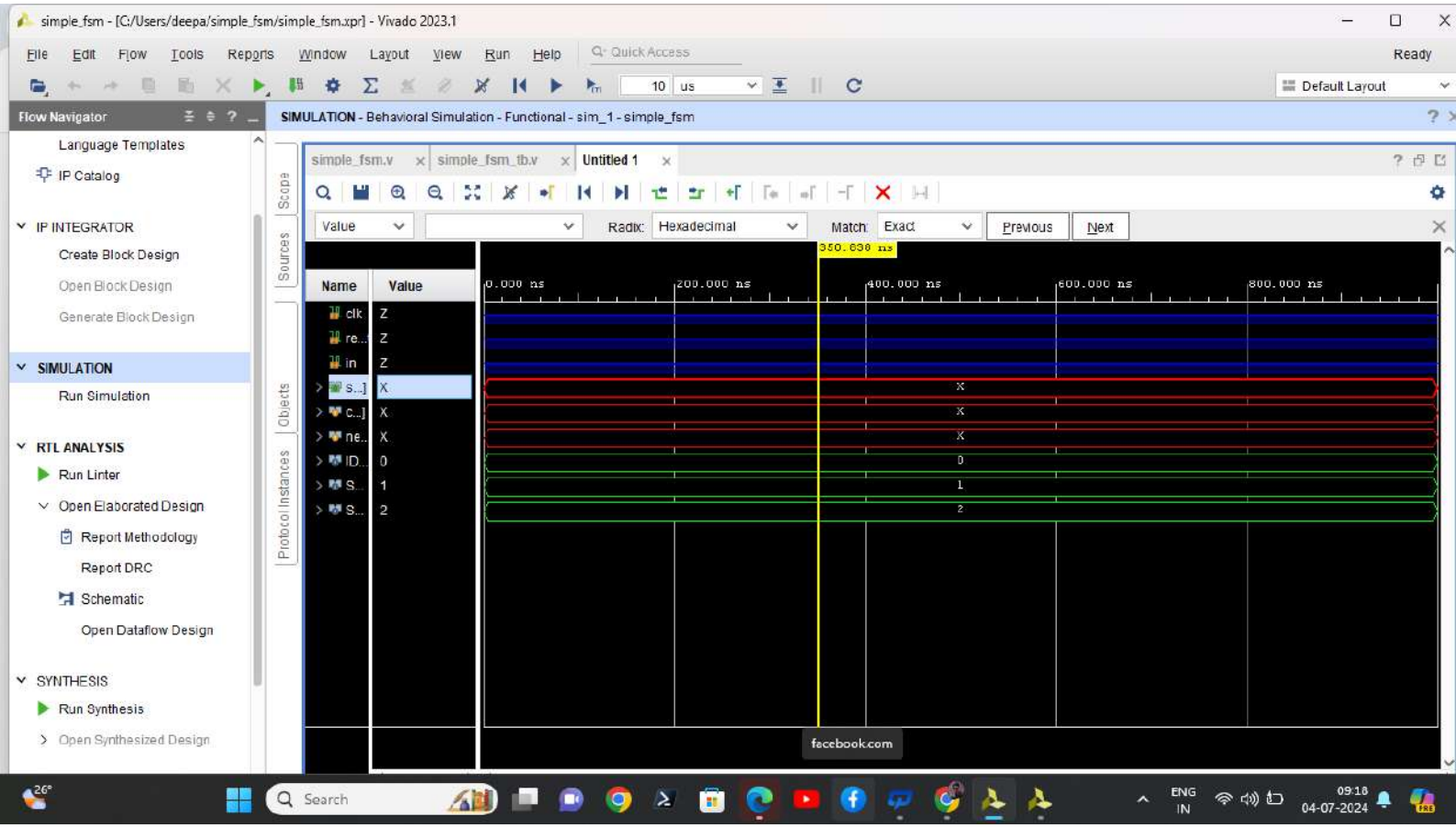

simple_fsm - [C:/Users/deepa/simple_fsm/simple_fsm.xpr] - Vivado 2023.1
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Ready
Default Layout
Flow Navigator
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Run Linter
Open Elaborated Design
Report Methodology
Report DRC
Schematic
Open Dataflow Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
ELABORATED DESIGN - Kria Part
Project Summary
Schematic
simple_fsm.v
C:/Users/deepa/simple_fsm/simple_fsm.srcs/sources_1/new/simple_fsm.v
Sources
Netlist
Source File Properties
next_state = STATE1;
else
next_state = IDLE;
STATE1:
if (in)
next_state = STATE2;
else
next_state = IDLE;
STATE2:
if (in)
next_state = STATE2;
else
next_state = IDLE;
default:
next_state = IDLE;
endcase
end
// Output logic
always @(*) begin
state = current_state;
end
endmodule
Tcl Console
Messages
Log
Reports
Design Runs
31:27
Insert
Verilog
Search
ENG
IN
08:43
04-07-2024


simple_fsm - [C:/Users/deepa/simple_fsm/simple_fsm.xpr] - Vivado 2023.1
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Ready
Default Layout
Flow Navigator
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Run Linter
Open Elaborated Design
Report Methodology
Report DRC
Schematic
Open Dataflow Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
ELABORATED DESIGN - Kria Part
Project Summary
Schematic
simple_fsm.v
4 Cells
5 I/O Ports
11 Nets
Sources
Netlist
Source File Properties
next_state_i
V=B"10",S=1'b1
S=default
I0[1:0]
I1[1:0]
O[1:0]
S
RTL_MUX
in
reset
clk
next_state_i__0
S=2'b00
S=2'b01
S=2'b10
S=default
I0
I1[1:0]
I2[1:0]
I3[1:0]
O[1:0]
S[1:0]
RTL_MUX
current_state_reg[1:0]
CLR
C
D
Q
RTL_REG_ASYNC
state[1:0]
Tcl Console
Messages
Log
Reports
Design Runs
Search
ENG
IN
08:43
04-07-2024


simple_fsm - [C:/Users/deepa/simple_fsm/simple_fsm.xpr] - Vivado 2023.1
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Ready
Default Layout
Flow Navigator
ELABORATED DESIGN - Kria Part
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Run Linter
Open Elaborated Design
Report Methodology
Report DRC
Schematic
Open Dataflow Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
Sources
Netlist
Source File Properties
Project Summary
Schematic
simple_fsm.v
simple_fsm_tb.v *
C:/Users/deepa/simple_fsm/simple_fsm.srcs/sim_1/new/simple_fsm_tb.v
20 //
21
22 module simple_fsm_tb;
23
24 // Inputs
25 reg clk;
26 reg reset;
27 reg in;
28
29 // Outputs
30 wire [1:0] state;
31
32 // Instantiate the FSM
33 simple_fsm uut (
34 .clk(clk),
35 .reset(reset),
36 .in(in),
37 .state(state)
38);
39
40 // Clock generation
41 always #5 clk = ~clk;
42
43 initial begin
44 // Initialize inputs
Tcl Console
Messages
Log
Reports
Design Runs
76:1
Insert
Verilog
Search
ENG
IN
08:51
04-07-2024


simple_fsm - [C:/Users/deepa/simple_fsm/simple_fsm.xpr] - Vivado 2023.1
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Ready
Default Layout
Flow Navigator
ELABORATED DESIGN - Kria Part
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Run Linter
Open Elaborated Design
Report Methodology
Report DRC
Schematic
Open Dataflow Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
Sources
Netlist
Source File Properties
Project Summary
Schematic
simple_fsm.v
simple_fsm_tb.v *
C:/Users/deepa/simple_fsm/simple_fsm.srcs/sim_1/new/simple_fsm_tb.v
44 // Initialize inputs
45 clk = 0;
46 reset = 0;
47 in = 0;
48
49 // Apply reset
50 reset = 1;
51 #10;
52 reset = 0;
53
54 // Test sequence
55 #10 in = 1; // Move to STATE1
56 #10 in = 1; // Move to STATE2
57 #10 in = 0; // Move back to IDLE
58 #10 in = 1; // Move to STATE1
59 #10 in = 0; // Move back to IDLE
60 #10 in = 1; // Move to STATE1
61 #10 in = 1; // Move to STATE2
62 #10 in = 1; // Stay in STATE2
63 #10 in = 0; // Move back to IDLE
64 #10;
65
66 // Finish simulation
67 $finish;
68 end
Tcl Console
Messages
Log
Reports
Design Runs
76:1
Insert
Verilog
Search
ENG
IN
08:51
04-07-2024


simple_fsm - [C:/Users/deepa/simple_fsm/simple_fsm.xpr] - Vivado 2023.1
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Ready
Default Layout
Flow Navigator
ELABORATED DESIGN - Kria Part
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Run Linter
Open Elaborated Design
Report Methodology
Report DRC
Schematic
Open Dataflow Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
Sources
Netlist
Source File Properties
Project Summary
Schematic
simple_fsm.v
simple_fsm_tb.v *
C:/Users/deepa/simple_fsm/simple_fsm.srcs/sim_1/new/simple_fsm_tb.v
// Test sequence
#10 in = 1; // Move to STATE1
#10 in = 1; // Move to STATE2
#10 in = 0; // Move back to IDLE
#10 in = 1; // Move to STATE1
#10 in = 0; // Move back to IDLE
#10 in = 1; // Move to STATE1
#10 in = 1; // Move to STATE2
#10 in = 1; // Stay in STATE2
#10 in = 0; // Move back to IDLE
#10;
// Finish simulation
$finish;
end
initial begin
// Monitor signals
$monitor("Time: %0d, Reset: %b, In: %b, State: %b", $time, reset, in, state);
end
endmodule
Tcl Console
Messages
Log
Reports
Design Runs
77:1
Insert
Verilog
Search
ENG
IN
08:51
04-07-2024


simple_fsm - [C:/Users/deepa/simple_fsm/simple_fsm.xpr] - Vivado 2023.1
File Edit Flow Tools Reports Window Layout View Run Help
Quick Access
Ready
Default Layout
Flow Navigator
SIMULATION - Behavioral Simulation - Functional - sim_1 - simple_fsm
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Run Linter
Open Elaborated Design
Report Methodology
Report DRC
Schematic
Open Dataflow Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
simple_fsm.v
simple_fsm_tb.v
Untitled 1
Value
Radix: Hexadecimal
Match: Exact
Previous
Next
Name
Value
clk
in
0.000 ns
200.000 ns
400.000 ns
600.000 ns
800.000 ns
350.630 ns
facebook.com
Search
ENG
IN
09:18
04-07-2024