

<p>Y. C. Lim, "Single-precision multiplier with reduced circuit complexity for signal processing applications," in IEEE Transactions on Computers, vol. 41, no. 10, pp. 1333-1336, Oct. 1992, doi: 10.1109/12.166611.</p>	<p>Problem Considered When two numbers are multiplied, a double-word length product is produced. In applications where only single precision is required, the circuit introduces complexity.</p> <p>Proposed Solution The least significant part of the product is not computed exactly. It is only necessary to estimate the carries generated in the computation of the least significant part that will ripple into the most significant part of the product.</p> <p>Results Significantly reduced circuit complexity.</p> <p>Demerits The estimation of Least significant part is not sufficiently accurate. Correction introduces complexity.</p>
<p>Lan-Da Van, Shuenn-Shyang Wang and Wu-Shiung Feng, "Design of the lower error fixed-width multiplier and its application," in IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 47, no. 10, pp. 1112-1118, Oct. 2000, doi: 10.1109/82.877155.</p>	<p>Problem Considered Truncation error in existing fixed width multipliers is high</p> <p>Proposed Solution A better error compensation bias is derived to reduce truncation error by properly choosing generalised index.</p> <p>Results 1. A lower error fixed-width multiplier, for VLSI realisation is constructed. 2. FIR for filter for speech processing is designed using the proposed model. The performance for consonant part is better than that using other fixed-width multipliers.</p> <p>Demerits Area requirement was higher</p>
<p>S. -J. Jou, Meng-Hung Tsai and Ya-Lan Tsao, "Low-error reduced-width Booth multipliers for DSP applications," in IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, vol. 50, no. 11, pp. 1470-1474, Nov. 2003, doi: 10.1109/TCSI.2003.817779.</p>	<p>Problem Considered 1. The post-truncation method wastes computation effort in terms of both computation time and hardware area. 2. Number of partial products to be calculated is high in case of Baugh-Wooley multipliers.</p> <p>Proposed Solution 1. A faster low-error reduced-width Booth multiplier using appropriate compensation vector is proposed to improve the limited performance of reduced-width array multipliers. 2. The number of partial products on average is reduced.</p> <p>Results The proposed reduced-width Booth multiplier has similar error performance as the array multiplier. However the operational speed is much faster</p>

	<p>Demerits The area of the proposed reduced-width Booth multiplier is 1.3 times that of the two's complement reduced-width array multiplier.</p>
J. Wang, S. Kuang and S. Liang, "High-Accuracy Fixed-Width Modified Booth Multipliers for Lossy Applications," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 19, no. 1, pp. 52-60, Jan. 2011, doi: 10.1109/TVLSI.2009.2032289.	<p>Problem Considered The mean error in truncation is not distributed symmetrically.</p>
	<p>Proposed Solution An effective error compensation function that makes the error distribution more symmetric and centralised in the error equal to zero, leading the fixed-width modified Booth multiplier to very small mean and mean-square errors.</p>
	<p>Results The proposed error compensation circuits offer at least 12.3% and 6.3% reductions in mean-square error over the previous circuits, respectively</p>
J. Liang, J. Han and F. Lombardi, "New Metrics for the Reliability of Approximate and Probabilistic Adders," in IEEE Transactions on Computers, vol. 62, no. 9, pp. 1760-1771, Sept. 2013, doi: 10.1109/TC.2012.146.	<p>Problem Considered There has been a lack of appropriate metrics to evaluate the efficacy of various inexact designs.</p>
	<p>Proposed Solution Reliability is analysed using sequential probability transition matrices (SPTMs)</p>
	<p>Results New metrics are proposed for evaluating the reliability as well as the power efficiency of approximate and probabilistic adders</p>
H. Jiang, J. Han, F. Qiao and F. Lombardi, "Approximate Radix-8 Booth Multipliers for Low-Power and High-Performance Operation," in IEEE Transactions on Computers, vol. 65, no. 8, pp. 2638-2644, 1 Aug. 2016, doi: 10.1109/TC.2015.2493547.	<p>Problem Considered Power dissipation in multipliers is high</p>
	<p>Proposed Solution The error detection, compensation and recovery circuits of the approximate multiplier is simplified.</p>
	<p>Results The proposed design outperforms the other approximate multipliers in the FIR filter operation, thus this design may be useful for low-power and imprecise operations in error-resilient systems.</p>
	<p>Demerits The error due to the recoding adder is more significant than the one caused by truncation</p>
S. Venkatachalam, E. Adams, H. J. Lee	<p>Problem Considered The existing inexact multipliers have fixed accuracy. So the multipliers have to be designed specific to the needs.</p>

<p>and S. Ko, "Design and Analysis of Area and Power Efficient Approximate Booth Multipliers," in IEEE Transactions on Computers, vol. 68, no. 11, pp. 1697-1703, 1 Nov. 2019, doi: 10.1109/TC.2019.2926275.</p>	<p>Proposed Solution Multiplication technique is mathematically modelled to allow various levels of approximation and performance trade-offs.</p> <p>Results An accuracy-adjustment fixed-width Booth multiplier that compensates the truncation error using a multilevel conditional probability is proposed.</p>
<p>H. Waris, C. Wang, W. Liu and F. Lombardi, "AxBMs: Approximate Radix-8 Booth Multipliers for High-Performance FPGA-Based Accelerators," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 68, no. 5, pp. 1566-1570, May 2021, doi: 10.1109/TCSII.2021.3065333.</p>	<p>Problem Considered The focus of existing designs on approximate radix-8 Booth multipliers has been on ASIC-based platforms. So they cannot achieve comparable performance gains when used for FPGA-based hardware accelerators</p> <p>Proposed Solution Approximation is implemented such that the 6-input lookup table (LUT) and the associated carry chains of the FPGAs are fully utilised</p> <p>Results The proposed multipliers are applied to the application of Sobel edge detection. The proposed solution detected 98.45% edges with energy savings of 26.41%.</p>