CS209 Computer Architecture

Memory (Primary memory)

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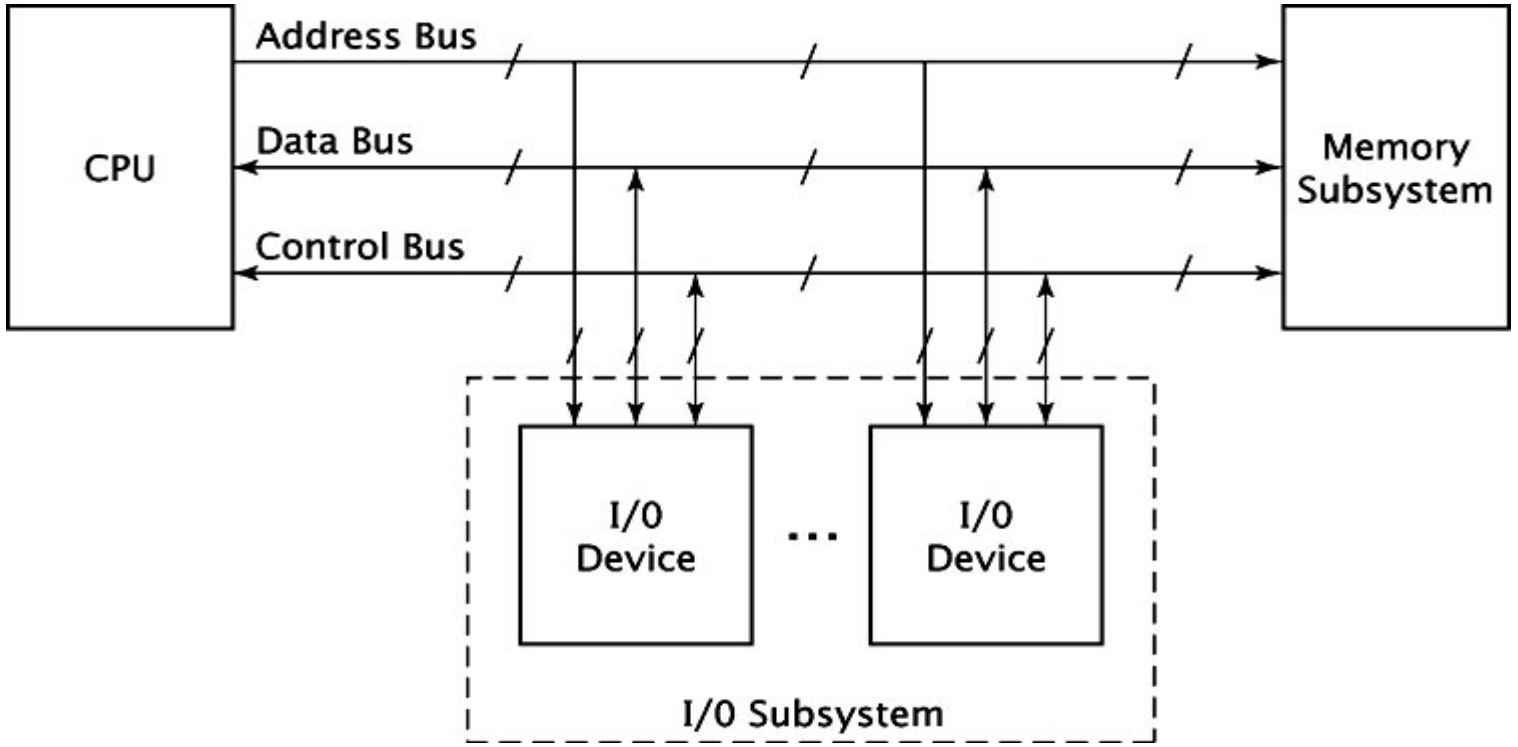
Setting into context

- Tiny CPU (MIPS)
  - ALU



Memory Characteristics

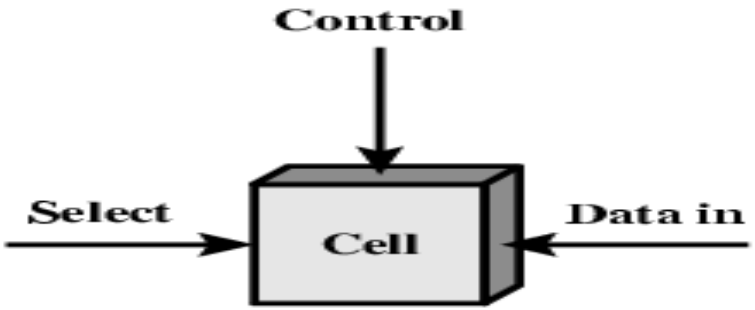
- Location
- Capacity
- Unit of transfer
- Access method
- Performance
- Physical type
- Organisation

Memory Cell Operation

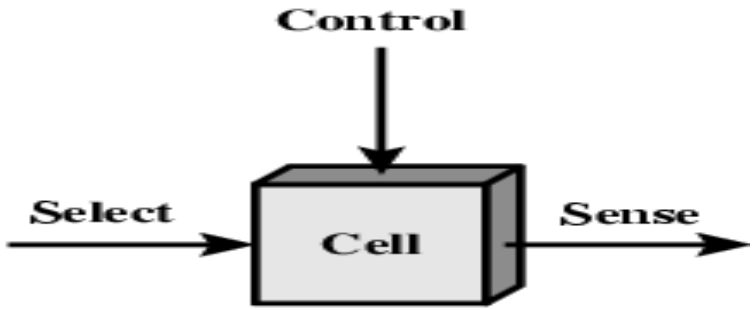
The basic element of Memory is a cell

A cell is capable of storing a bit (1 or 0) to write on it

A cell is capable of being read to sense the state.



(a) Write



(b) Read

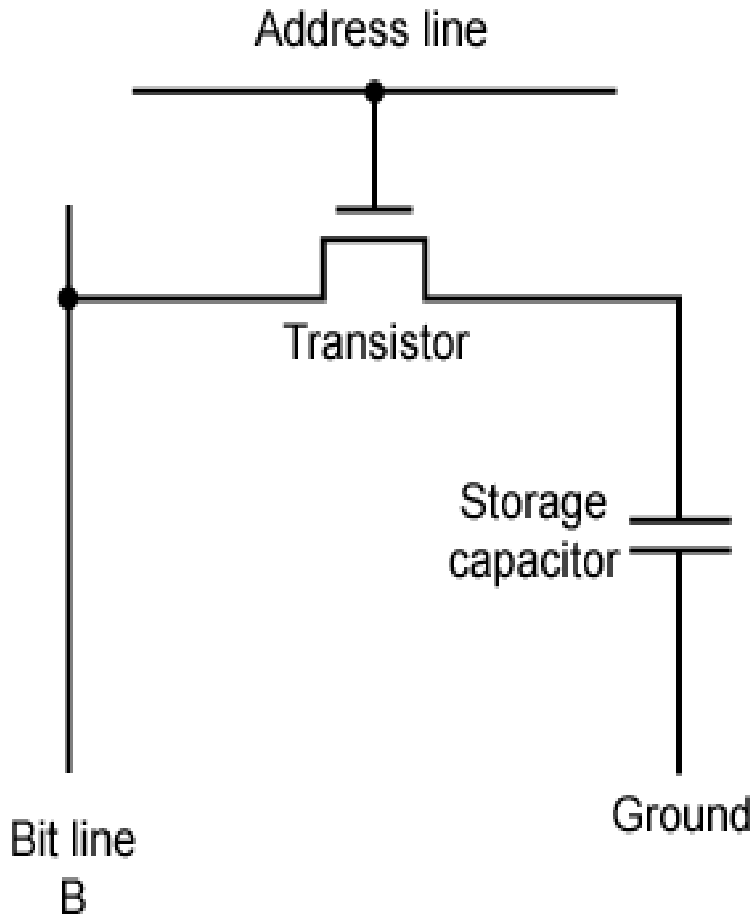
Static RAM Operation

- Transistor arrangement gives stable logic state
- State 1
  - C_1 high, C_2 low
  - T_1 T_4 off, T_2 T_3 on
- State 0
  - C_2 high, C_1 low
  - T_2 T_3 off, T_1 T_4 on
- Address line transistors T_5 T_6 is switch
- Write – apply value to B & compliment to $\overline{B}$
- Read – value is on line B

- Bits stored as on/off switches
- No charges to leak
  - No refreshing needed when powered
- Faster
- Cache
- Digital
  - Uses flip-flops
- More complex construction
- More expensive

DRAM Operation

- Bits stored as charge in capacitors
  - Charges leak
  - Need refreshing even when powered
- Simpler construction
- Smaller per bit
- Less expensive
- Need refresh circuits
- Slower
- Main memory
- Essentially analogue
  - Level of charge determines value
  - Capacitor charge must be restored

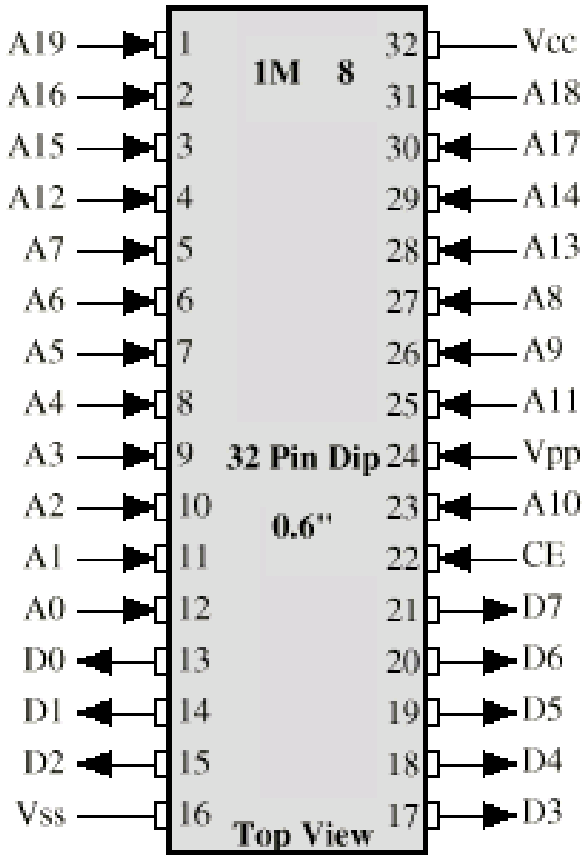


Organisation in detail

- A chip can be organised in different ways
  - 16Mbit memory can be organized as
    - 16M of 1 bit each or
    - 1M of 16 bit words or
    - as a 2048 x 2048 x 4bit array
  - Reduces number of address pins
  - Multiplex row address and column address
  - 11 pins to address (2^{11}=2048)

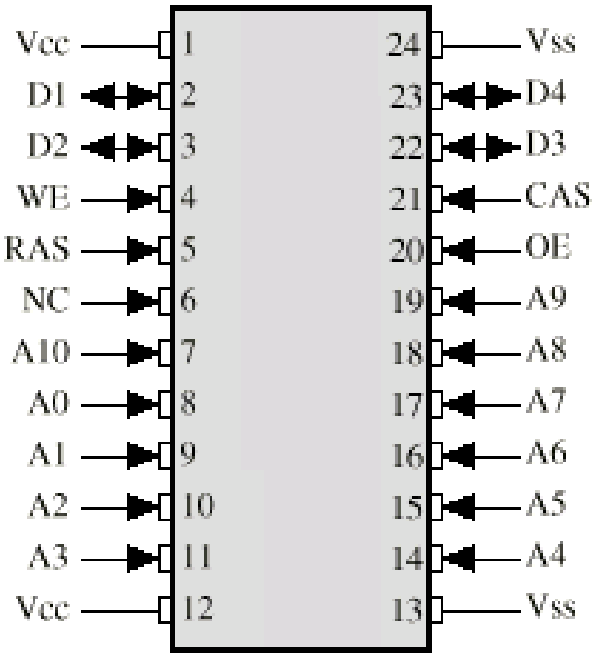
Packaging

1M x 8 =8Mbit EPROM



(a) 8 Mbit EPROM

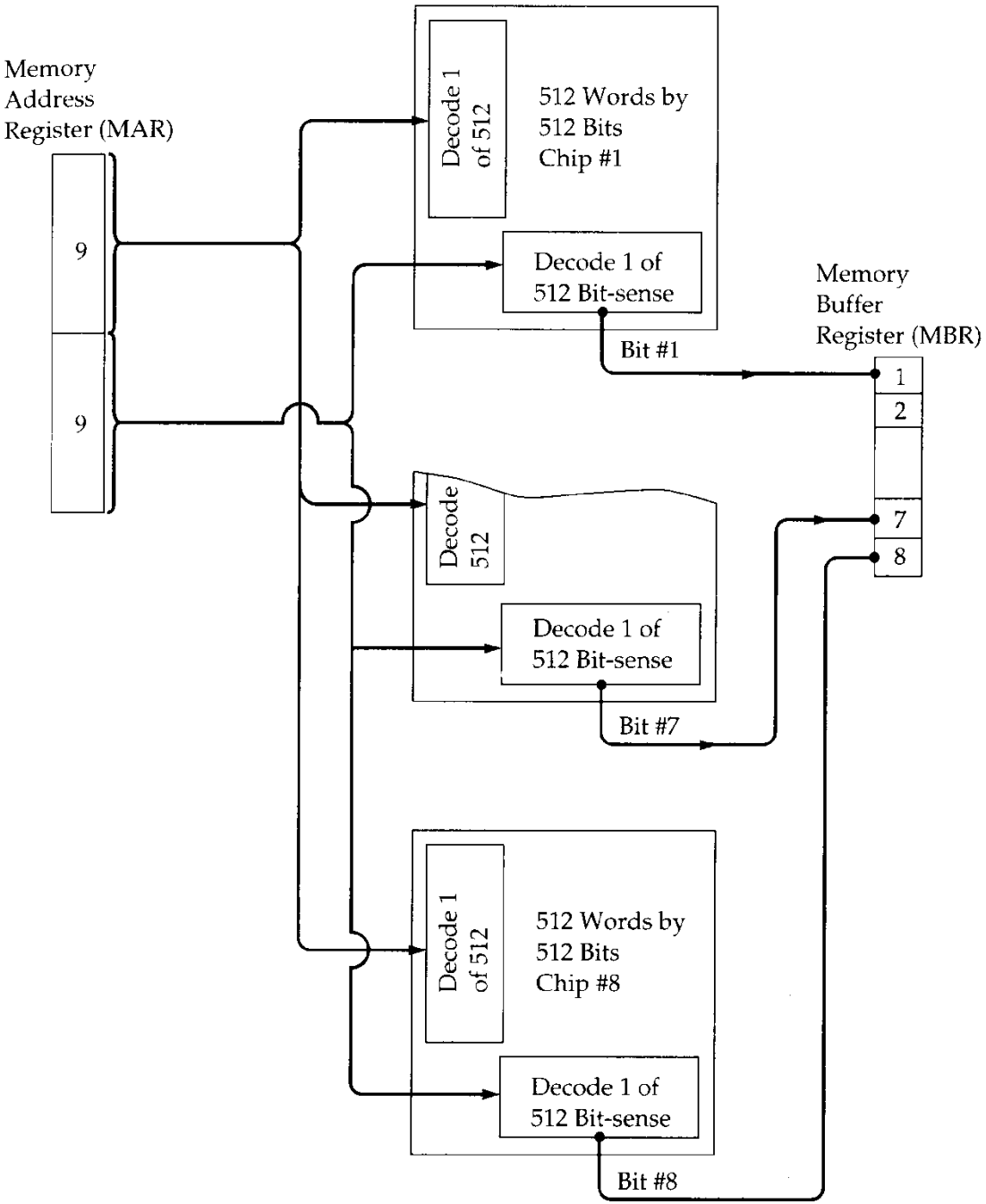
4M x 4 =16Mbit DRAM



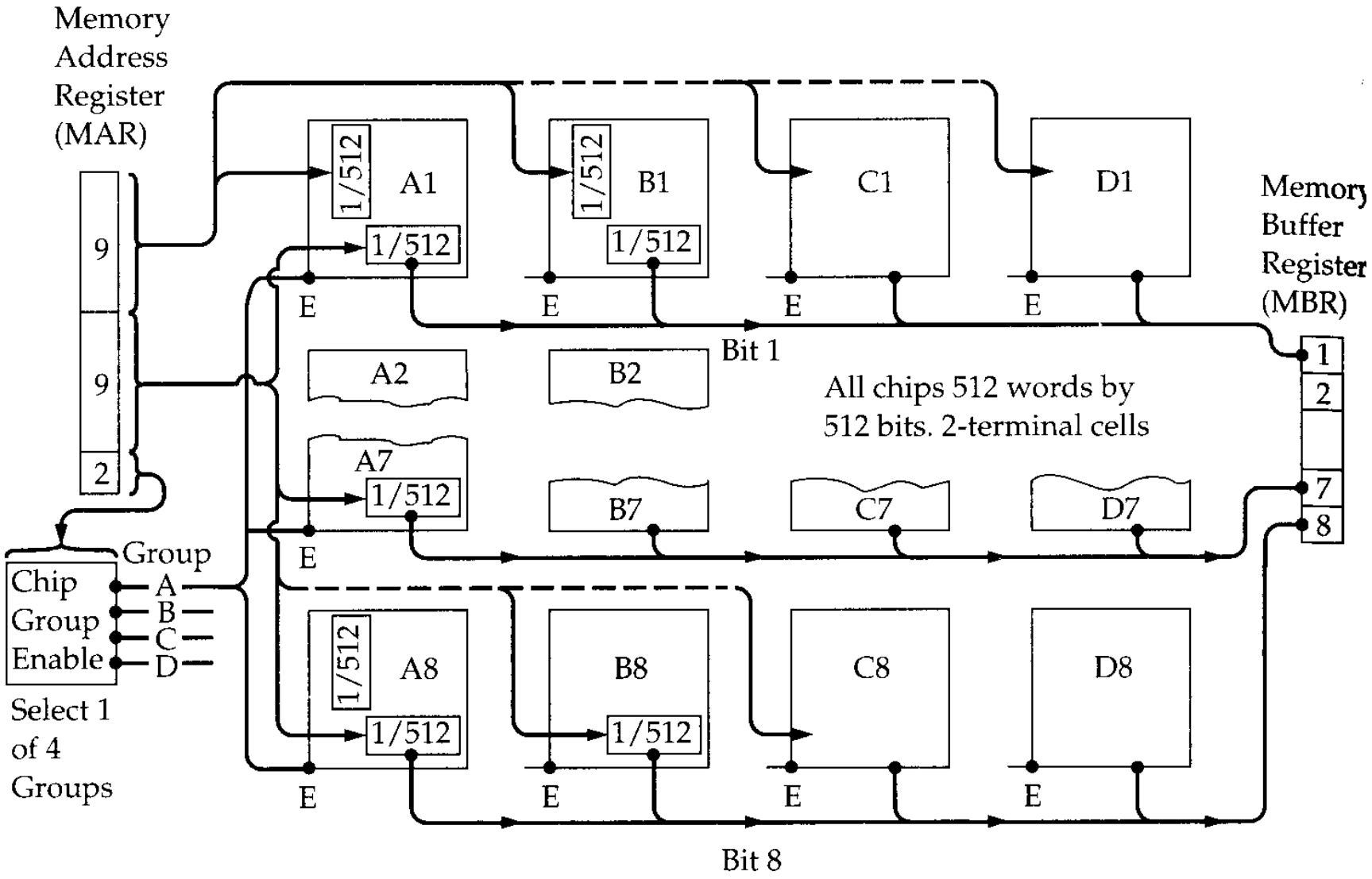
(b) 16 Mbit DRAM

256kByte Module Organisation

Consider A RAM chip contains 1 bit per word



1MByte Module Organisation



Simplified DRAM Read

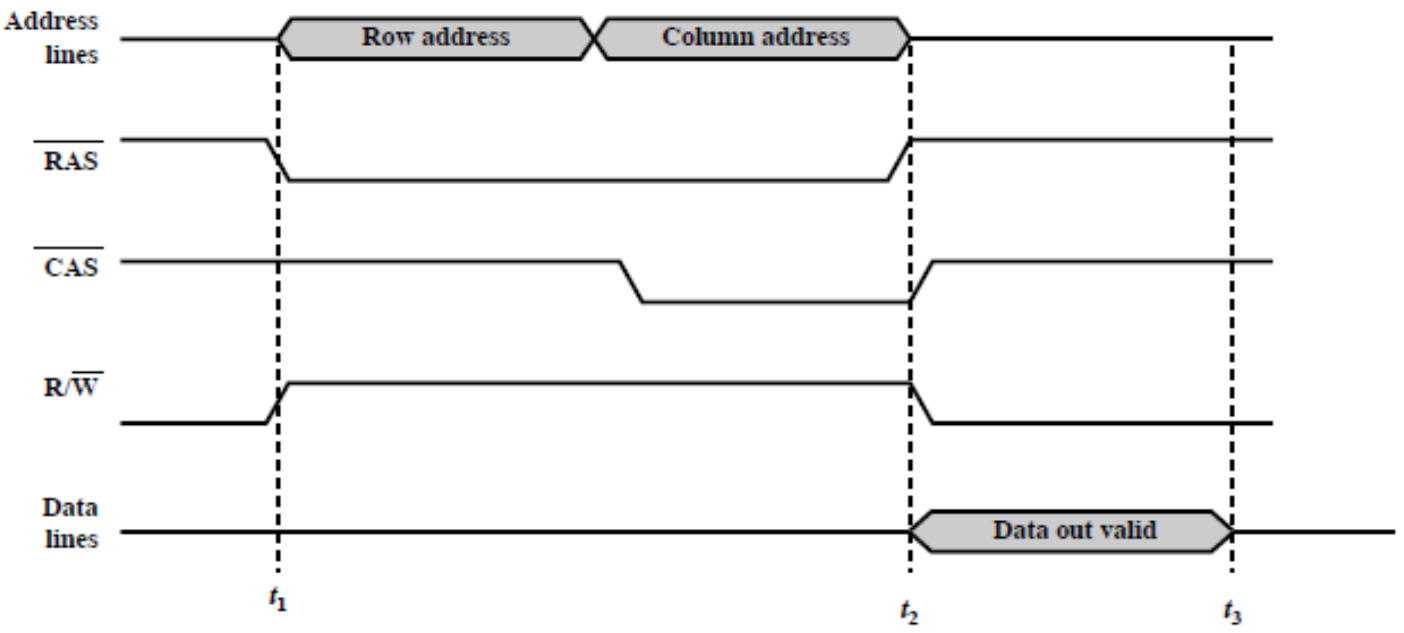


Figure 5.15 Simplified DRAM Read Timing

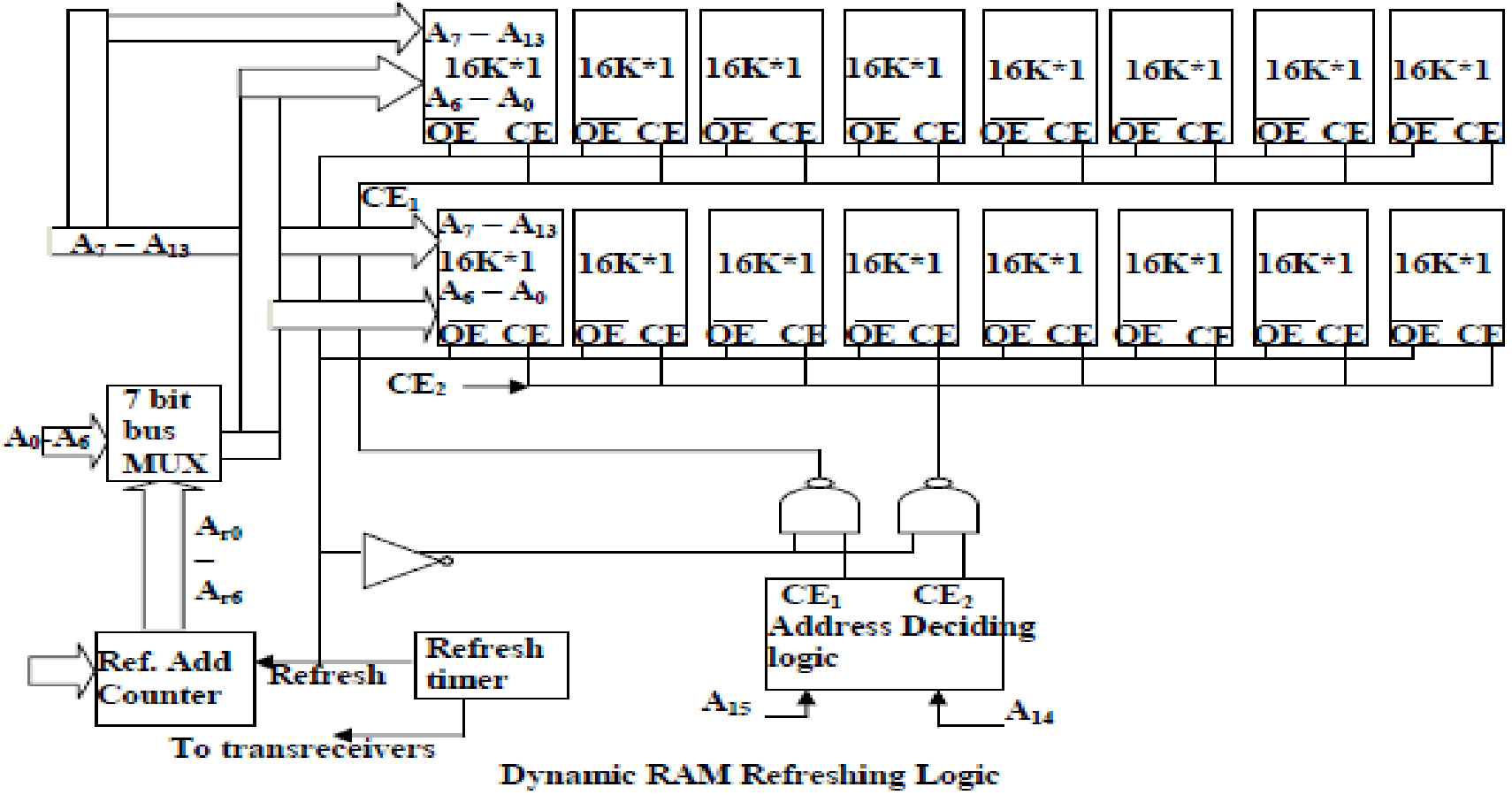
DRAM Refreshing

- A dedicated hardware chip called as dynamic RAM controller is the most important part of the interfacing circuit.

- The ***Refresh cycle is different from the memory read*** cycle in the following aspects.

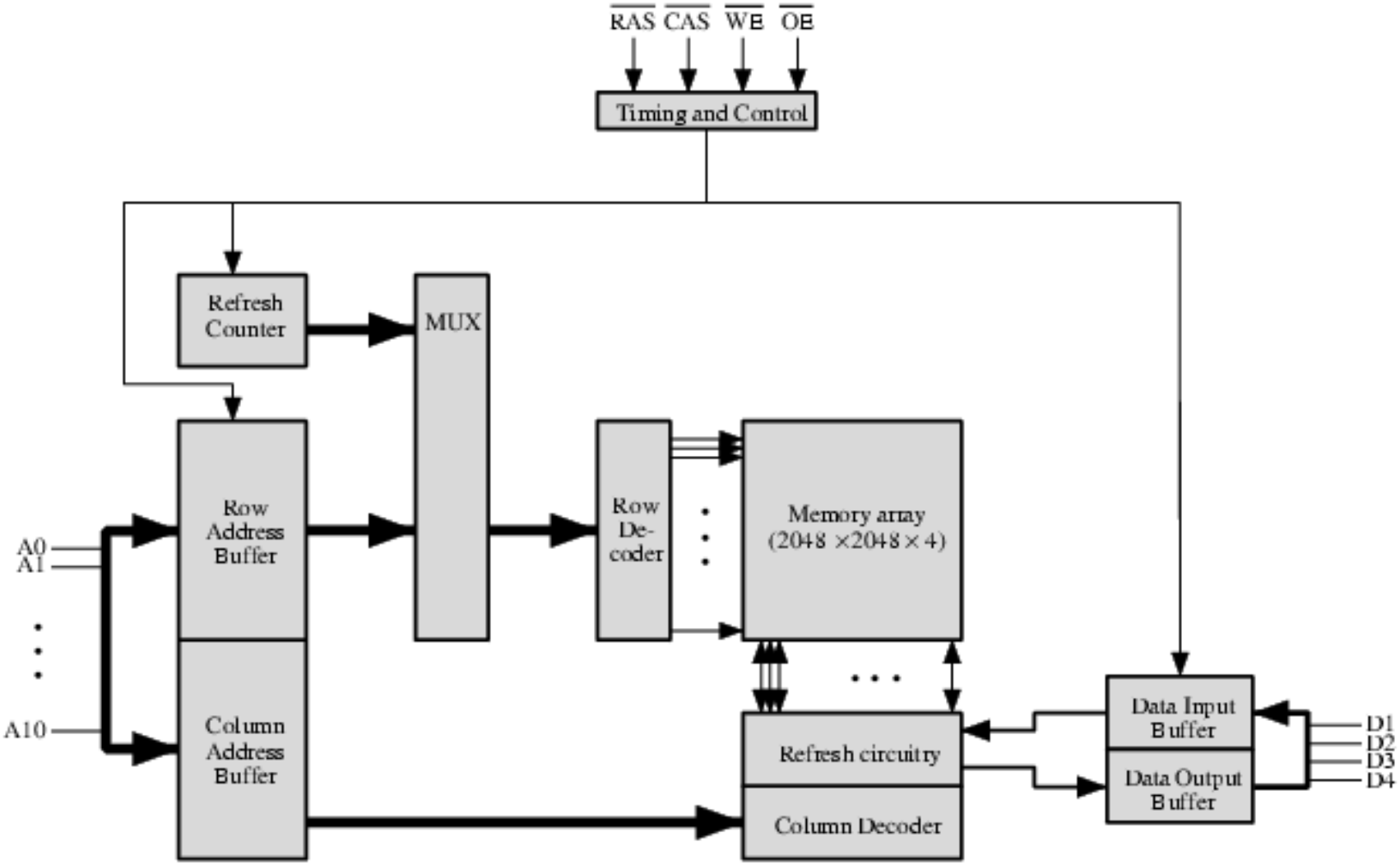
1. The memory address is not provided by the CPU address bus, rather it is generated by a refresh mechanism counter called as refresh counter.
2. Unlike memory read cycle, more than one memory chip may be enabled at a time so as to reduce the number of total memory refresh cycles.
3. The data enable control of the selected memory chip is deactivated, and data is not allowed to appear on the system data bus during refresh, as more than one memory units are refreshed simultaneously. This is to avoid the data from the different chips to appear on the bus simultaneously.

DRAM Refreshing logic



Dynamic RAM Refreshing Logic

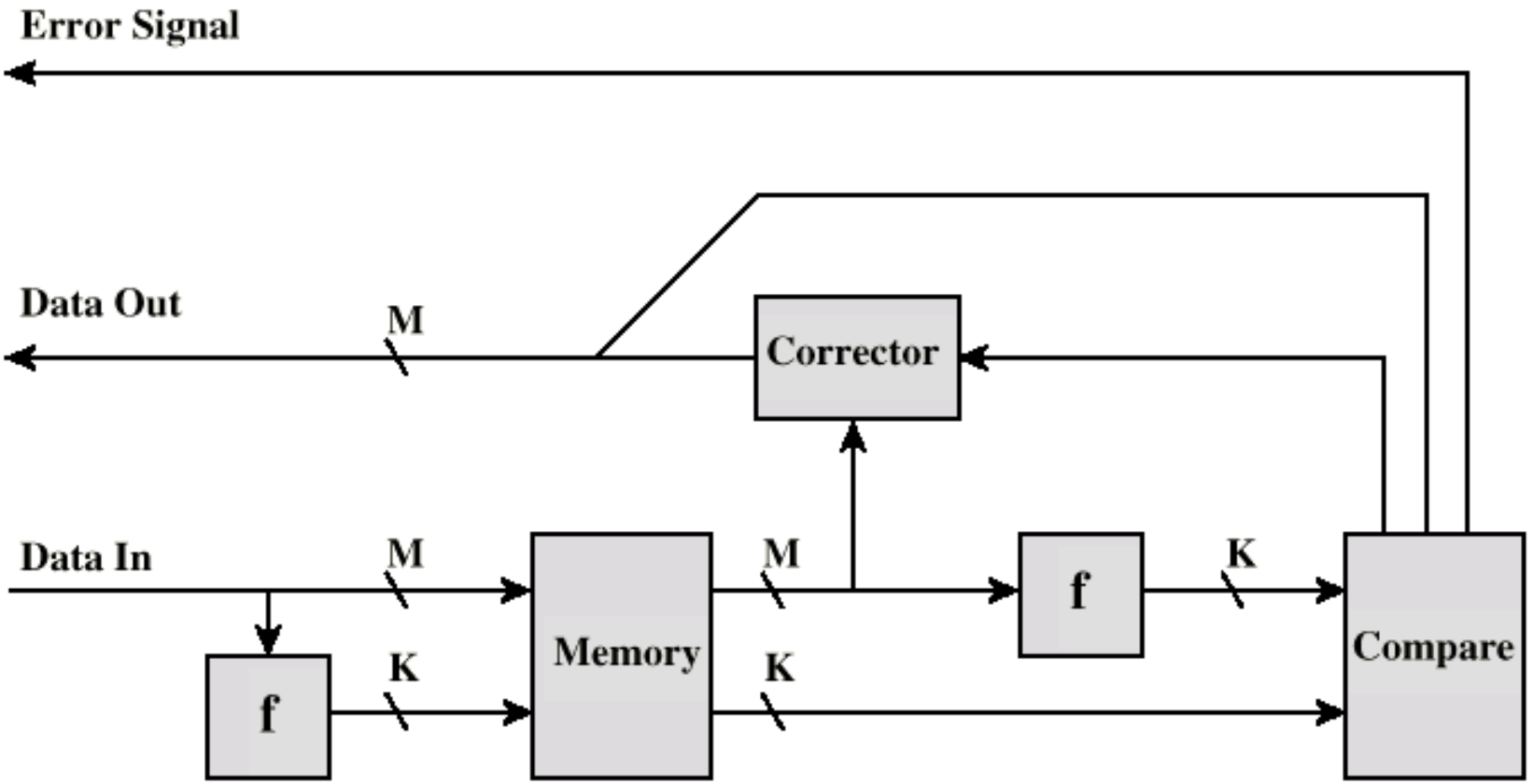
Typical 16 Mb (4M x 4) DRAM



Error Correction

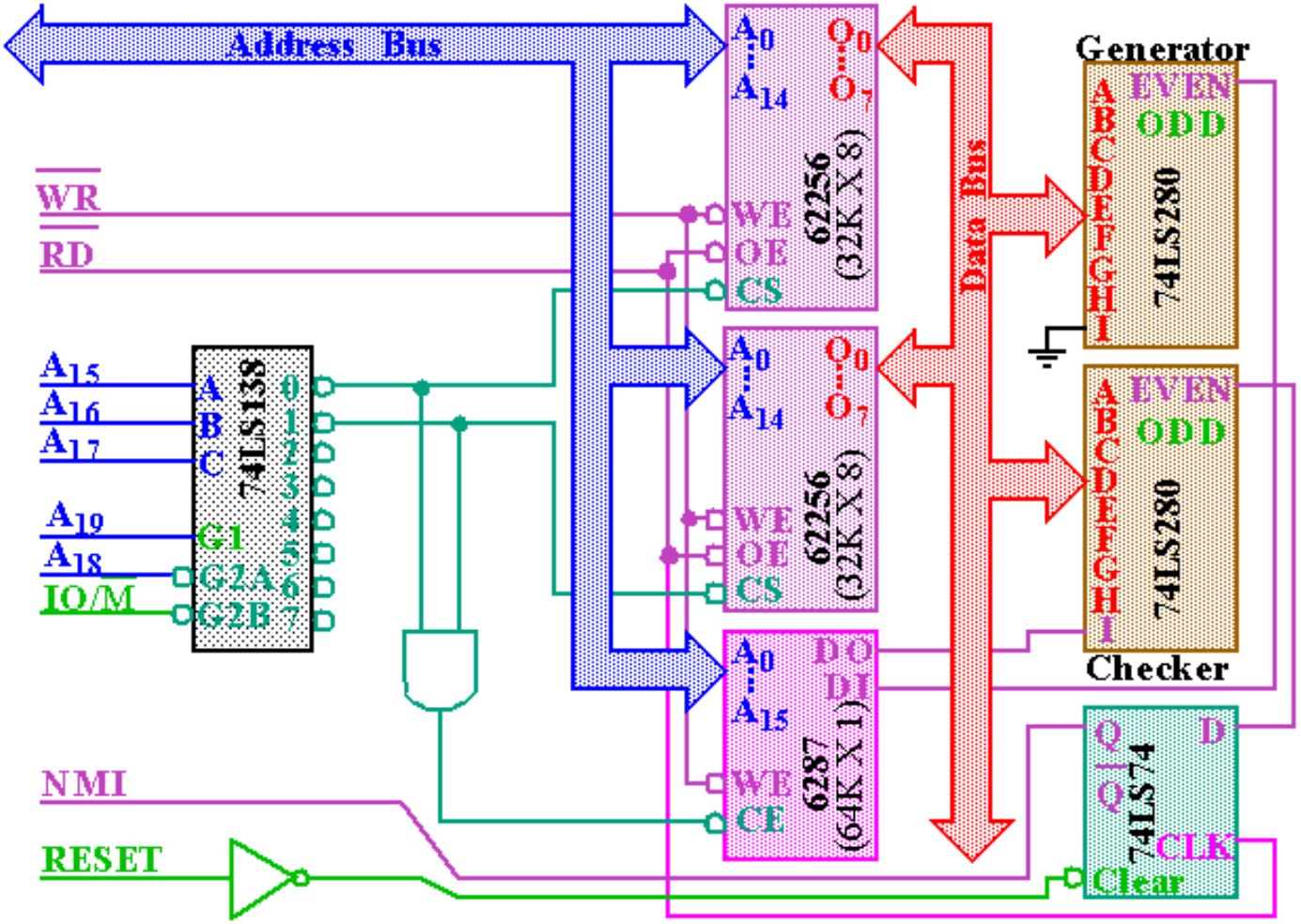
- Error occurs
  - Hard Failure
    - Permanent defect
  - Soft Error
    - Random, non-destructive
    - No permanent damage to memory
- Both form of the errors are undesirable
- Detected using Hamming error correcting code

Error Correcting Code Function



9-bit parity generator checker

Number of inputs A thru I that are HIGH	Outputs EVEN	Outputs ODD
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H


Address Bus
Data Bus
WR
RD
NMI
RESET
A15
A16
A17
A19
A18
IO/M
74LS138
A
B
C
G1
G2A
G2B
0
1
2
3
4
5
6
7
A0
A14
O0
O7
WE
OE
CS
62256
(32K X8)
A0
A15
DO
DI
WE
CE
6287
(64K X1)
Generator
EVEN
ODD
74S280
Checker
Q
D
CLK
Clear
74S74

Hamming Codes: Single Error-correcting

No. of information bits = m

No. of parity check bits, p1, p2, …, pk = k
No. of bits in the code word = m+k

Assign a decimal value to each of the m+k bits: from 1 to MSB to m+k to LSB

Perform k parity checks on selected bits of each code word: record results as 0 or 1

- Form a binary number (called position number), c1c2…ck, with the k parity checks

Hamming Codes (Contd.)

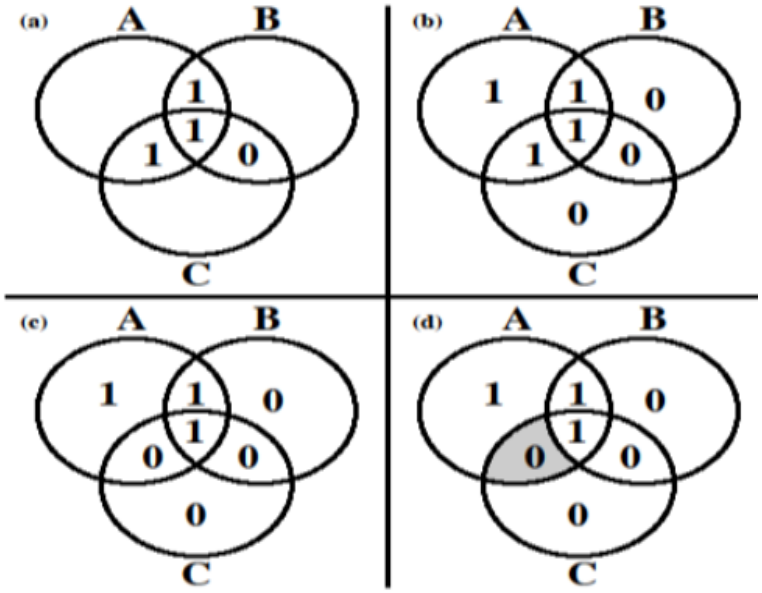
No. of parity check bits, k, must satisfy: $2^k >= m+k+1$

Example: if m = 4 then k =3

Place check bits at the following locations: 1, 2, 4, …, 2^{k-1}

Example code word: 1100110

- Check bits: p1= 1, p2 = 1, p3 = 0
- Information bits: 0, 1, 1, 0



Hamming Code Construction

Select p_1 to establish even parity in positions: 1, 3, 5, 7

Select p_2 to establish even parity in positions: 2, 3, 6, 7

Select p_3 to establish even parity in positions: 4, 5, 6, 7

Error position	Position number		
	c1	c2	c3
0 (no error)	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

Hamming Code Construction (Contd.)

Position:	1 p_1	2 p_2	3 m_1	4 p_3	5 m_2	6 m_3	7 m_4
Original BCD message:			0		1	0	0
Parity Check in positions 1,3,5,7 requires p_1=1	1		0		1	0	0
Parity Check in positions 2,3,6,7 requires p_2=0	1	0	0		1	0	0
Parity Check in positions 4,5,6,7 requires p_3=1	1	0	0	1	1	0	0
Coded message	1	0	0	1	1	0	0