## JALPAIGURI GOVERNMENT ENGINEERING COLLEGE [A GOVERNMENT AUTONOMOUS COLLEGE]

# COE/B.TECH./CSE/ PCC-CS30<u>1</u>/2022-23

### 2023

# Data Structure & Algorithm

Full Marks: 70

Times: 3 Hours

The figures in the margin indicate full marks. Candidates are requested to write their answers in their own words as far as practicable.

### GROUP-A [OBJECTIVE TYPE QUESTIONS] Answer all questions

5x2=10

- What is the worst-case time complexity of merge sort algorithm?
- Why do we need to study the asymptotic notations?

3.	Give an example of a comparison-based sorting algorithm and not comparison-based sorting algorithm.	
4.	What is the difference between Binary Search Tree (BST) and AVL tree?	
5.	What is difference between Tree and Graph data structure?  GROUP-B	
	[LONG ANSWER TYPE QUESTIONS]	
	wer any four questions 4x15	
6.	<ol> <li>Write down an efficient algorithm to find the maximum and minimum element from an array of n integers and analyze its time complexity.</li> </ol>	5
	ii) If $f(n) = 3n^7 + 6n^2 + 13$ , then prove that $f(n)$ is not $O(n^7)$ .	3
	iii) What is a Threaded Binary Tree? What is the need of it? Write down the algorithm for in-order traversal in a threaded binary tree.	7
<b>√</b> 7.	<ul> <li>Suppose a binary tree T with n nodes each containing an integer is represented in memory using linked representation. Write down an algorithm to compute the sum of all the nodes in T.</li> </ul>	6
	ii) Consider a min heap, represented by the array: 40; 30; 20; 10; 15; 16; 17; 8; 4. Now consider that a value 35 is inserted into this heap. What would be the array representation of the heap after the insertion?	6
	iii) Describe drawbacks of the Array Data structure and Link List data structure.	3
±8.	<ul> <li>i) Construct a B-tree of order 5 with the following keys, A G F B K D H M J E S I R X C L N T U P in order, where A &lt; B &lt; C &lt; : : &lt; Z. Show the steps clearly.</li> </ul>	7
	ii) What do you mean by Internal path length (LI) and External path length (LE) of an Extended binary tree. Prove that LE = LI + 2I, where I is the number of Internal nodes.	5
	iii) If only one traversal (inorder or postorder or preorder) of binary tree is given, is it possible to come up with the unique binary tree? Justify your answer.	3
9.	i) A single array A[1 : : :MAXSIZE] is used to implement two stacks. The two stacks grow from opposite ends of the array. Variables top 1 and top 2 (top 1 < top 2) point to the location of the topmost element in each of the stacks. Write down the procedures to push() and pop() element in the stacks mentioning clearly the condition for "stack full" and "stack empty".	6
	ii) Write down the Breadth First Search (BFS) algorithm of a graph with suitable example.	5
	iii) Convert the following infix expression Q into equivalent postfix expression: (show all the steps) $Q: A + (B*C - (D/F)*G)*H$	4
₹10.	i) What is Graph? Explain the representation of a Graph data structure.	4
	ii) Write down an efficient procedure/algorithm to delete the middle element from a linked list?	5
	iii) What is hashing? What are the properties a good hash function should possess?	3
	iv) State the difference between the B-Tree and B+Tree with suitable diagram.	3

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yl.	<ul> <li>i) What is Abstract Data Type (ADT)?</li> <li>ii) Write an algorithm to implement binary search algorithm using array data structure.</li> <li>iii) Derive the average case time complexity of linear search algorithm.</li> <li>iv) What are the advantages and disadvantages of array data structure over link list?</li> <li>v) What is sparse matrix? Give an example of sparse matrix.</li> </ul>	2 4 3 4 2
12/	<ul> <li>i) Define the relationship between the Abstract Data Type (ADT) and Data Structure.</li> <li>ii) Is it possible to apply the binary search algorithm to sorted link list? Justify your answer.</li> <li>iii) Which searching algorithm will you prefer among linear search and binary search? Explain your answer.</li> </ul>	2 2 3
	iv) Consider the following array in C language (Turbo C Complier):	2
	$char\ a[5][10];$ Find out the address of the action to the bound of the amount is 2000.	
	<ul> <li>Find out the address of the a[3][7], where the base address of the array a is 2000.</li> <li>v) Discuss the similarity and dissimilarity of searching operation of binary search tree and binary search algorithm.</li> <li>vi) Write your first name in capital letters and arrange the list of characters using selection sort algorithm. (Show all steps in detail)</li> </ul>	3
13.	i) How can you implement a binary tree using array?	2
	ii) Define tree with the help of Graph.	2
	iii) Write in-order, pre-order and post-order traversal algorithms.	6
	iv) Consider the following list of numbers. 40, 30, 50, 22, 60, 55, 77, 65 Create the max BST (show only the stepwise diagram).	4
	v) Draw all possible non-empty binary trees, whose in-order, pre-order and post-order traversals are same.	1
14	<ul> <li>Write short notes on any three of the following topics:</li> <li>a) Radix Sort</li> <li>b) B- Tree</li> <li>c) Hashing</li> <li>d) Heap Sort</li> <li>e) Circular Queue</li> </ul>	3x5=15

# JALPAIGURI GOVERNMENT ENGINEERING COLLEGE [A GOVERNMENT AUTONOMOUS COLLEGE] COE/B.TECH./CSE/PCC-CS301/2022-23 2023

COMPUTER ORGANIZATION

Full Marks: 70

Times: 3 Hours

The figures in the margin indicate full marks.

Candidates are requested to write their answers in their own words as far as practicable.

# GROUP-A<sup>™</sup> [OBJECTIVE TYPE QUESTIONS]

Answer all questions

5x2=10

- 1. What is biased exponent? Give an example.
- 2. What are the functions of MAR and MBR.
- 3. What is Booth's recoding? Give one example.
- 4. What is the range of signed numbers of a 8 bit 2's complement signed binary numbers?
- 5. Add (+12) and (-10) by signed 2's complement addition.

# GROUP-B [LONG ANSWER TYPE QUESTIONS]

Answer any four questions 4x15=60 i) With a wheel/clock like diagram show all signed 2's complement 4 bit binary numbers and its decimal 4 6. ii) Explain the smallest, largest denormalized and normalized floating point numbers in 32 bit precision. iii) Suppose in a 8 bit floating point representation, there are 4 exponent bits and 3 fraction bits. Show the representable de-normalized and normalized range of values. 7. i) Suppose a modern memory addressing mechanism having 4 bit in MAR and each address is used to refer to only a single bit among 16 bit of data. You are given two 2-to-22 decoders to design the system. Draw the diagram for the above system. ii) You are given a 16K-by-4 ROM unit. Convert it to 64K-by-1 ROM unit. Treat the 16K-by-4 ROM as one unit that you cannot alter. Only logic external to this 16K-by-4 ROM unit is to be shown and explained. iii) Describe spatial locality and temporal locality with suitable examples. 5 i) Define 'write back' and 'write through' schemes and compare them. 8. ii) Explain the mechanism of fully associative mapping in cache memory with diagram showing different 5 components. iii) a) Convert (-13.6875)10 into IEEE single precision format. into equivalent decimal number. i) Draw the block diagram of a single BCD adder and explain the working mechanism. ii) Discuss the principle of carry look ahead adder and design a 4 bit CLA adder and estimate the speed enhancement with respect to ripple carry adder. iii) Design a 4 bit binary Adder-Subtractor composite unit with overflow detection mechanism and explain with sample numbers.

2

1010

PTO

10 ->

0 0 1

10010

- i) Subtract (1111)<sub>2</sub> from (10100)<sub>2</sub> without using 2's complement technique and show the borrow bits 4 clearly with explanation.
   ii) Describe Booth's encoding technique for (-24)<sub>10</sub> and show two cases where Booth's multiplication is 5
  - faster and same respectively in speed with conventional multiplication algorithm.

    iii) Show the step by step multiplication process using Booth algorithm when the following binary numbers 6 are multiplied, (+7) as multiplicand and (-13) as multiplier.
- 11. i) Sometimes in the last step of non-restoring method of division (when all quotient bits are ready) to get 4 remainder it is necessary to add with divider (a restoring step). In which circumstances this is required describe with proper examples.
  - ii) Write an algorithm for restoring method of division with an example.
  - iii) Apply non restoring division to divide 27 by 6. Clearly explain each step.
- 12. i) Explain memory hierarchy with typical speed and size.

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ii) A direct mapped cache consists of 64 lines. Main memory contains 4K blocks of 128 words each. Split the main memory address into tag, set and word offset.

5

iii) Consider a 32 bit microprocessor that has an on-chip 16KB four-way set associative cache. Assume that that the cache has a line size of four 32 bit words. Show how the different address fields are used 8 to determine a cache hit/miss. Where in the cache is the word from memory location AB5DE8F2 mapped?

# JALPAIGURI GOVERNMENT ENGINEERING COLLEGE [A GOVERNMENT AUTONOMOUS COLLEGE] JGEC/B.TECH/ CSE/ BS-CH301/ 2022-23 2023

## BIOLOGY FOR ENGINEERS

Full Marks: 70

Times: 3 Hours

The figures in the margin indicate full marks. Candidates are instructed to write the answers in their own words as far as practicable. GROUP-A

### [OBJECTIVE TYPE QUESTIONS]

Answer all questions

5X2=10

- 1. Write two examples of basic amino acids.
- 2. What do you mean by exergonic reaction?
- 3. What do you mean by gram positive bacteria?
- 4. What is peptide bond?
- 5. What is nucleotide?

#### GROUP-B

### [LONG ANSWER TYPE QUESTIONS]

Answer any four questions

15X4=60

- 6. Classify carbohydrate with suitable examples.
- 7. Describe the dihybrid cross experiment of Mendel. Define test cross with a suitable example,

(10+5=15)

8. Describe the molecular structure of DNA described by Watson and Crick. Write three differences

between DNA and RNA.

(12+3=15)

9. Describe the classification of bacteria.

15

10. Describe the microbial growth curve. Classify different types enzyme.

(5+10=15)

11. Describe the different types of protein structure.

15

12. Describe different theories of enzyme action. Enumerate various types of enzyme inhibition.

(10+5=15)

# JALPAIGURI GOVERNMENT ENGINEERING COLLEGE [A GOVERNMENT AUTONOMOUS COLLEGE] COE/B.TECH./CSE/ESC301/2022-23 2023

# DIGITAL ELECTRONICS

Full Marks: 70

Times: 3 Hours

The figures in the margin indicate full marks.

Candidates are requested to write their answers in their own words as far as practicable.

	GROUP-A	
	[OBJECTIVE TYPE QUESTIONS] 5x2=10	
	wer all questions  Draw a full adder circuit with NAND Gate only.	
1.	Convert the binary [100101101] <sub>2</sub> to Gray code and Gray Code [11101011] <sub>G</sub> to binary form.	
3.	White two and liestings of country	
	Write two applications of counter.	
4.	Prove the DeMorgan's theorem with example.	
5.	Define universal logic gate? Give example.  GROUP-B	
	[LONG ANSWER TYPE QUESTIONS]	
Ano	wer any four questions 4x15=60	
7.	i) What is the difference between latch and flip flop? Draw a circuit diagram of JK flip flop and state the truth table.  ii) A combinational logic circuit has 3 inputs A. B. C and output F. F is true for following input	1+4
	combinations: a) A is false, B is true b) A is false, C is true c) A, B, C are true d) A, B, C are false.  Now answer the following  a) Write truth table for F. Use the convention, true =1 and false =0  b) Write the simplified expression for F in SOP and POS form. c) Draw the circuit with NAND gate.	10
8.	<ul> <li>i) Draw the circuit of a Mod-32 synchronous counter. How many logic gates are used in this device?</li> <li>ii) Draw the circuit of a serial in-serial out shift register and explain its working. Data 11010 is entered in</li> </ul>	6
	to 5 bit serial-in serial out shift register. Show the status of registers after 1,2,3,4,5 clock pulses.	6
	iii) What are the differences between asynchronous and synchronous counter?	3
9.	<ul> <li>i) Design a combinational circuit that accepts a three-bit number and generates an output binary number equal to the square of the input number.</li> </ul>	5
	ii) Design a combinational circuit whose input is a four bit number and whose output is the 2's complement of the input number.	5
	iii) Find the maximum frequency of ripple counter having (a) 3 bits (b) 5 bits. Assume tpd of each flip flop as 20 ns.	5 .
10.	<ul> <li>i) What is race around condition? Draw logic diagram (showing all gates) of a master-slave flip-flop using NAND gates only and explain the working pinciple.</li> </ul>	2+5
	ii) What is excitation table? State the excitation table of SR, JK, D flip flops. Convert a SR flip flop into JK flip flop.	1+3+
11.	<ul> <li>i) Implement the following function with an 8 to 1 multiplexer. (A=S2, C=S1, D=S0)</li> <li>F(A, B, C, D) = ∑(0, 2, 4, 5, 7, 8, 10, 12, 13, 15)</li> </ul>	5
	ii) Construct a 5 x 32 decoder with 3 x 8 decoder and 2 x 4 decoder only.  iii) Design a combinational circuit that compares two 4-bit numbers A and B to check if they are equal.	5
10	The circuit has one output x, so that $x = 1$ if $A = B$ and $x = 0$ if A is not equal to B.	5
12.	i) What is Boolean Algebra? What is its utility in digital circuit design? Explain different laws of Boolean Algebra.	5
	<ul> <li>ii) What is the standard form of a Boolean function? Obtain the canonical sum of product form of the F</li> <li>iii) Use K-map to simple for the following and Work to Canonical product of sum form.</li> </ul>	5
	iii) Use K-map to simplify the following a)Y(A,B,C,D)= $\sum m(0,2,3,6,8,9,14,15)$ b) F(A,B,C,D)= $\prod M(0,4,6,8,10,12,14)$	5

AB