NC State University

Department of Electrical and Computer Engineering

ECE 463/521: Spring 2010 (Rotenberg)

Project #1: Cache Design, Memory Hierarchy Design

by

<< Mistry Deep Dilipkumar >>

NCSU Honor Pledge: "I have neither given nor received unauthorized aid on this test or assignment."

Student's electronic signature: Mistry Deep Dilipkumar
(sign by typing your name)

Course number: _____521_____
(463 or 521 ?)

Sample cover page for Project #1. Created 2/1/10.

Introduction

In this project, our main aim is to design computer memory hierarchy. The Computer hierarchy is divided into Cache's, Main memory and Hard Discs. Here I have simulated a two level Cache. I have designed a generic cache module which can be reconfigured according to different input parameters of size, blocksize and associativity. The memory hierarchy which I have simulated is shown below.

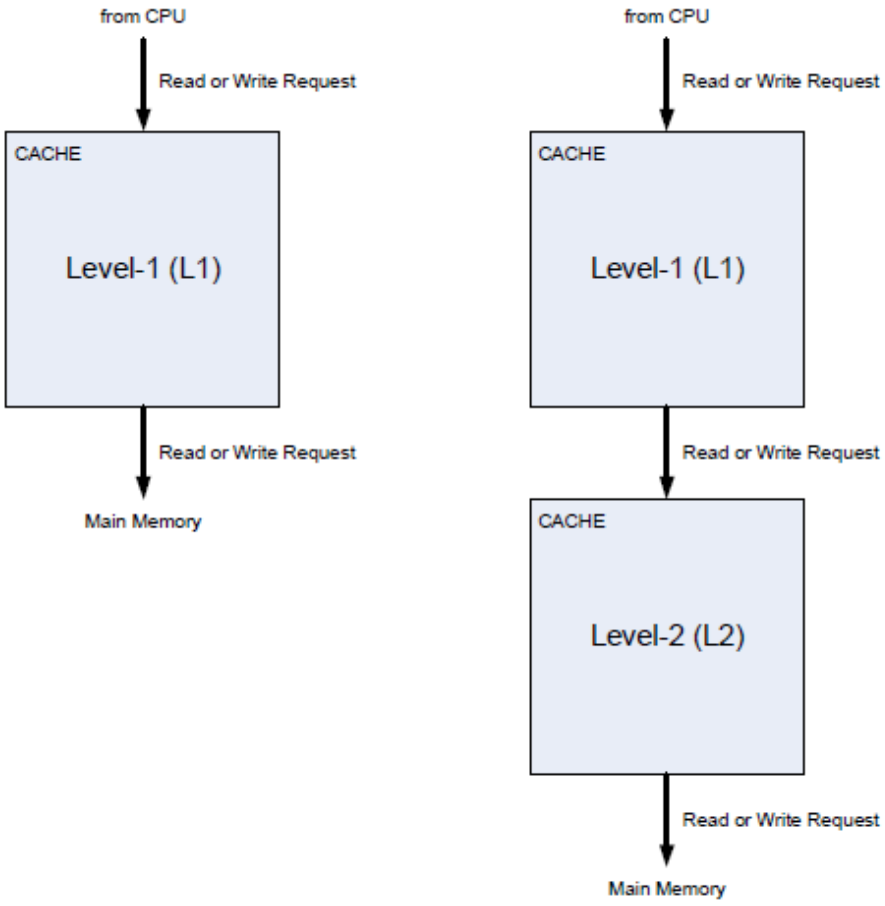


Figure 1. Memory Hierarchy Configurations
(Courtesy: Project #1 specifications, ECE 521)

Experiments and design space exploration
The design relies of these fixed parameters to be considered.

1. Miss_Penalty (in ns) = 10 ns + 0.1*(BLOCKSIZE / 16 B/ns)
2. E_{mem} = 0.05 nJ
3. Area Budget = 1.7 mm^2

Misses:- in this project, I have used the concept of on the fly classification. Of L1 and L2 misses.

I have created a generic cache which can be used to define any cache module.
That is that from a single module of cache you can create both set associative and the FA cache.

You can disable or enable the L2 caches, by setting L1.nextlevel = null; in the sim_cache.

Outputs for the configurations tested :-

1)

```
===== Simulator configuration =====
BLOCKSIZE:  16
L1_SIZE: 1024
L1_ASSOC:   1
L1_PSEUDO-ASSOC-EN:  0
L2_SIZE: 0
L2_ASSOC:   0
L2_PSEUDO-ASSOC-EN:  0
trace_file: gcc_trace.txt
===== L1 contents =====
set   0:  1000c5
set   1:  100147 D
set   2:  100147 D
set   3:  100147 D
set   4:  1000c5
set   5:  1000c5
set   6:  100147 D
set   7:  1000c5
set   8:  1000c5
set   9:  1000bd D
set   10:  1000bd
set   11:  1000c5
set   12:  1000d9 D
set   13:  1000c5
set   14:  1000d6
set   15:  1000d9 D
```

```
set   16:  1ec0ce D
set   17:  10007d
set   18:  10007d
set   19:  1000d9 D
set   20:  10007d
set   21:  10010a
set   22:  1000d5
set   23:  10009d
set   24:  1000f9
set   25:  1000d5
set   26:  100146 D
set   27:  10009d
set   28:  10009d
set   29:  10009d
set   30:  100146 D
set   31:  1000fc D
set   32:  100146 D
set   33:  100146 D
set   34:  1000e0 D
set   35:  100146 D
set   36:  100111 D
set   37:  1000e0
set   38:  100146 D
set   39:  100146 D
set   40:  1000c7 D
set   41:  1000c7
set   42:  100146 D
set   43:  100004
set   44:  100004
set   45:  100004
set   46:  100004
set   47:  100004
set   48:  100004
set   49:  100004
set   50:  100004
set   51:  100004
set   52:  100004
set   53:  100004
set   54:  100004
set   55:  1000d5
set   56:  1000c7 D
set   57:  1000d5
set   58:  100146 D
set   59:  100146 D
set   60:  100146 D
set   61:  1000c6 D
set   62:  1000c6 D
set   63:  1000c6 D
===== Simulation results (raw) =====
a. number of L1 reads: 63640
b. number of L1 read misses: 10728
c. number of L1 writes: 36360
d. number of L1 write misses: 8493
e. L1 miss rate: 0.1922
f. number of searches of alternate set S' within L1: 0
g. number of swaps within L1: 0
h. number of spills within L1: 0
```

```
i. L1 primary-set miss rate: 0.0000
j. number of writebacks from L1: 9802
k. number of cold misses in L1: 4713
l. number of capacity misses in L1: 8304
m. number of conflict misses in L1: 6204
n. number of L2 reads: 0
o. number of L2 read misses: 0
p. number of L2 writes: 0
q. number of L2 write misses:   0
r. L2 miss rate: 0.0000
s. number of searches of alternate set S' within L2: 0
t. number of searches of alternate set S' within L2 (instigated by L2
reads only): 0
u. number of swaps within L2: 0
v. number of spills within L2: 0
w. L2 primary-set miss rate: 0.0000
x. number of writebacks from L2:   0
y. number of cold misses in L2: 0
z. number of capacity misses in L2: 0
aa. number of conflict misses in L2: 0
bb. total memory traffic: 29023
===== Simulation results (performance) =====
L1 cacti results: Accesstime=0.1203, Energy=0.0015, Area=0.0126
1. Total Access Time (ns):  206159.2031
2. Average Access Time (ns): 2.0616
3. Total Energy (nJ): 1626.6469
4. Energy-Delay Product (nJ*ns): 335348218.4826
5. Area (mm^2): 0.0126
```

2)

```
===== Simulator configuration =====
BLOCKSIZE:  16
L1_SIZE: 1024
L1_ASSOC:   2
L1_PSEUDO-ASSOC-EN:  0
L2_SIZE: 0
L2_ASSOC:   0
L2_PSEUDO-ASSOC-EN:  0
trace_file: gcc_trace.txt
===== L1 contents =====
set   0:  20028d D 20018a
set   1:  20028d D 20028e D
set   2:  2001c1 D 200153 D
set   3:  20028d D 20013b
set   4:  200223 D 20028d
set   5:  2001c1    200149
set   6:  20028d D 20028e D
set   7:  20018a    2001ac D
set   8:  20018f D 20018a
set   9:  20018f D 2000f9
set   10:  20017a    2000fa
set   11:  200009    20018a
set   12:  200009    20028d D
set   13:  200009    2000f9
set   14:  200009    2001ac
```

```
set   15:  200009    2001b2 D
set   16:  200009    3d819c D
set   17:  200009    20017b D
set   18:  200009    2000fa
set   19:  200009    2001b2 D
set   20:  200009    2000fa
set   21:  200009    200214
set   22:  200009    20023f
set   23:  2001ab    20013a
set   24:  20018f D 2001f2
set   25:  2001aa    2001ab
set   26:  20028d D 20018d D
set   27:  20028d D 20018d D
set   28:  20013a    20028d D
set   29:  20013a    20018d D
set   30:  20028c D 20018d D
set   31:  2001f8 D 20028c D
===== Simulation results (raw) =====
a. number of L1 reads: 63640
b. number of L1 read misses: 8322
c. number of L1 writes: 36360
d. number of L1 write misses: 7680
e. L1 miss rate: 0.1600
f. number of searches of alternate set S' within L1: 0
g. number of swaps within L1: 0
h. number of spills within L1: 0
i. L1 primary-set miss rate: 0.0000
j. number of writebacks from L1: 8696
k. number of cold misses in L1: 4713
l. number of capacity misses in L1: 8382
m. number of conflict misses in L1: 2907
n. number of L2 reads: 0
o. number of L2 read misses: 0
p. number of L2 writes: 0
q. number of L2 write misses:   0
r. L2 miss rate: 0.0000
s. number of searches of alternate set S' within L2: 0
t. number of searches of alternate set S' within L2 (instigated by L2
reads only): 0
u. number of swaps within L2: 0
v. number of spills within L2: 0
w. L2 primary-set miss rate: 0.0000
x. number of writebacks from L2:   0
y. number of cold misses in L2: 0
z. number of capacity misses in L2: 0
aa. number of conflict misses in L2: 0
bb. total memory traffic: 24698
===== Simulation results (performance) =====
L1 cacti results: Accesstime=0.1544, Energy=0.0018, Area=0.0094
1. Total Access Time (ns):  177057.1094
2. Average Access Time (ns): 1.7706
3. Total Energy (nJ): 1442.8022
4. Energy-Delay Product (nJ*ns): 255458395.0931
5. Area (mm^2): 0.0094
```

3)

```
===== Simulator configuration =====
BLOCKSIZE:  16
L1_SIZE: 1024
L1_ASSOC:   1
L1_PSEUDO-ASSOC-EN:  0
L2_SIZE: 8192
L2_ASSOC:   4
L2_PSEUDO-ASSOC-EN:  0
trace_file: gcc_trace.txt
===== L1 contents =====
set   0:  1000c5
set   1:  100147 D
set   2:  100147 D
set   3:  100147 D
set   4:  1000c5
set   5:  1000c5
set   6:  100147 D
set   7:  1000c5
set   8:  1000c5
set   9:  1000bd D
set   10:  1000bd
set   11:  1000c5
set   12:  1000d9 D
set   13:  1000c5
set   14:  1000d6
set   15:  1000d9 D
set   16:  1ec0ce D
set   17:  10007d
set   18:  10007d
set   19:  1000d9 D
set   20:  10007d
set   21:  10010a
set   22:  1000d5
set   23:  10009d
set   24:  1000f9
set   25:  1000d5
set   26:  100146 D
set   27:  10009d
set   28:  10009d
set   29:  10009d
set   30:  100146 D
```

```
set   31:  1000fc D
set   32:  100146 D
set   33:  100146 D
set   34:  1000e0 D
set   35:  100146 D
set   36:  100111 D
set   37:  1000e0
set   38:  100146 D
set   39:  100146 D
set   40:  1000c7 D
set   41:  1000c7
set   42:  100146 D
set   43:  100004
set   44:  100004
set   45:  100004
set   46:  100004
set   47:  100004
set   48:  100004
set   49:  100004
set   50:  100004
set   51:  100004
set   52:  100004
set   53:  100004
set   54:  100004
set   55:  1000d5
set   56:  1000c7 D
set   57:  1000d5
set   58:  100146 D
set   59:  100146 D
set   60:  100146 D
set   61:  1000c6 D
set   62:  1000c6 D
set   63:  1000c6 D
===== L2 contents =====
set   0:  80066 D 800a3 D 800ac D 800ab D
set   1:  80066 D 8007d D 800a3 D 800ac D
set   2:  80066 D 8007e D 8006d D 800a3 D
set   3:  80066 D 800a3 D 800aa D 800a7 D
set   4:  80066 D 800a3 D 800aa D 800ac D
set   5:  80066 D 800a3 D 800aa D 800ac D
set   6:  800a3 D 800ac D 800ab D 800a6 D
set   7:  8006b D 8006c D 800a3 D 800ac D
set   8:  800a3 D 8006b D 800ac D 800ab D
set   9:  800a3 D 8003e    800ac D 800ab D
set   10:  800a3 D 800ac D 800ab D 800aa D
set   11:  800a3 D 800ac D 800ab D 800aa D
set   12:  8006b D 800a3 D 800ac D 800ab D
set   13:  800a3 D 80079 D 8006f D 800ac D
set   14:  8006b    800a3 D 800ac D 800ab D
set   15:  800a3 D 800ac D 800ab D 800aa D
set   16:  f6067 D 800a3 D 800ac D 800ab D
set   17:  800a3 D 8007f D 800ac D 800ab D
set   18:  800a3 D 800ac D 800ab D 800aa D
set   19:  f6067 D 800a3 D 800ac D 800a8 D
set   20:  8007f D 80085 D 800a3 D 800ac D
set   21:  80085 D 800a3 D 800ac D 800a8 D
set   22:  80085 D 800a3 D 800ac D 800ab D
```

```
set   23:  800a3 D f6067 D 800ac D 800a7 D
set   24:  800a3 D 8003e    800ac D 800a7 D
set   25:  800a3 D 8007d D 800ac D 800ab D
set   26:  800a3    800ac D 800ab D 800aa D
set   27:  800a3 D 800ac D 800ab D 800aa D
set   28:  800a3 D 800ac D 8007f D 800ab D
set   29:  800a3 D 8006a D 80074 D 800ac D
set   30:  800a3    800ac D 800ab D 8007f D
set   31:  8007e D 800a3 D 800ac D 800ab D
set   32:  800a3 D 80074 D f6067 D 800ac D
set   33:  800a3 D 80074 D 800ac D 800ab D
set   34:  80070    800a3 D 80074 D 800ac D
set   35:  800a3 D 800ac D 800a9 D 800a8 D
set   36:  800a3 D 80090    80070 D 800ac D
set   37:  80070 D 80052    800a3 D 8007f D
set   38:  800a3    80070 D 8006f D 8007f D
set   39:  800a3    80070 D 800ac D 800a9 D
set   40:  80052    800a3 D 8005a D 800a9 D
set   41:  8003e    800a3 D 800ac D 8006b D
set   42:  800a3 D 8006b D 800ab D 800aa D
set   43:  80002    800a3 D 800ab D 80070 D
set   44:  80002    800a3 D 8006b D 800ab D
set   45:  80002    8003e    800a3 D 800ab D
set   46:  80002    80052    800a3 D 8003e
set   47:  80002    800a3 D 8003e    800ab D
set   48:  80002    8003e    800a3 D 800ab D
set   49:  80002    80052    800a3 D 8005e D
set   50:  80002    8003e    800a3 D 800ab D
set   51:  80002    800a3 D 8007f D 8006d
set   52:  80002    800a3 D 800a9 D 800a8 D
set   53:  80002    800a3 D 800a9 D 800a8 D
set   54:  80002    800a3 D 800ab D 800a2 D
set   55:  800a3 D 80063 D 800ab D 800a2 D
set   56:  800a3 D 80063 D 80062 D 8006b D
set   57:  800a3 D 80063 D 80062    800ab D
set   58:  800a3    80063 D 80074 D 8006f D
set   59:  800a3    80063 D 80074 D 8007d D
set   60:  800a3    80063 D 8006b D 8007f D
set   61:  80063 D 800a3 D 8007d D 8006b D
set   62:  80063    800a3 D 800ab D 800a2 D
set   63:  80063    800a3 D 8006a D 80074 D
set   64:  80062    800a3 D 8005e D 800ab D
set   65:  800a3    800ab D 800a2 D 800aa D
set   66:  800a3    800ab D 800a2 D 800aa D
set   67:  800a3    800a8 D 800ab D 800a7 D
set   68:  80062    800a3 D 800a8 D 800ab D
set   69:  80062    800a3 D 800a8 D 800ab D
set   70:  800a3    800ab D 800a2 D 800aa D
set   71:  80062    800a3 D 8005e D 800a8 D
set   72:  80062    800a3 D 800a8 D 800ab D
set   73:  8005e D 800a3 D 800ab D 800a2 D
set   74:  8005e    8003e    800a3 D 80062
set   75:  80062    8006c D 800ab D 800a2 D
set   76:  8006c    800ab D 800a2 D 800aa D
set   77:  80062    8006c D 800ab D 800a2 D
set   78:  8003e    8006c D 8007d D 8005e
set   79:  8006c    8003e    800ab D 800a2 D
```

Sample cover page for Project #1. Created 2/1/10.

```
set   80:  8006c D 800ab D 800a2 D 800aa D
set   81:  8003e    8006c D 8006a    800ab D
set   82:  8003e    8006c D 8006a    800ab D
set   83:  8006c    8006a    800a6 D 800a9 D
set   84:  8003e    8006a    8006c D 800a9 D
set   85:  8006a    8006b    800a9 D 800a8 D
set   86:  8006a    800ab D 800a2 D 800aa D
set   87:  8004e    8006a    800a9 D 800a8 D
set   88:  8007c    80062 D 8004e    8006a
set   89:  8006a    800ab D 800a2 D 8007c
set   90:  8006c D 800a2 D 800ab D 800aa D
set   91:  8004e    8007f D 80088 D 800a2 D
set   92:  8004e    800a2 D 800ab D 800aa D
set   93:  8004e    8006c D 800a2 D 800ab D
set   94:  80088 D 800a2 D 800ab D 800aa D
set   95:  8004e    80088 D 800a2 D 800ab D
set   96:  80073    800a2 D 800ab D 800aa D
set   97:  8006a    80088 D 800a2 D 800ab D
set   98:  80054 D 8004e    8003e    800a2 D
set   99:  8004e    800a2 D 800a8 D 800ab D
set   100:  80088 D 8007d D 800a2 D 800a8 D
set   101:  8004e    800a2 D 800a8 D 800ab D
set   102:  800a2 D 800ab D 800aa D 800a9 D
set   103:  800a2 D 800ab D 800aa D 800a5 D
set   104:  80063 D 8008f    8007c D 800a2 D
set   105:  80063 D 8008f    800a9 D 800a2 D
set   106:  8008f    80063 D 800a2 D 800ab D
set   107:  8008f    80063 D 800a2 D 800ab D
set   108:  8008f    80088 D 800a2 D 8007f D
set   109:  8008f    800a2 D 800ab D 80073 D
set   110:  8008f    800a2 D 800ab D 800aa D
set   111:  8008f    8006e D 8005e D 8006b D
set   112:  8008f    8005e D 8006e D 800a2 D
set   113:  8005e D 8008f    8007d D 800a2 D
set   114:  8008f    800a2 D 8003d    800ab D
set   115:  8008f    8005e D 800a6 D 800a2 D
set   116:  8008f    80063 D 800a2 D 8003d
set   117:  8008f    8006a D 80063 D 800a2 D
set   118:  8008f    800a2 D 800ab D 80039
set   119:  8006a    8008f    800a2 D 800ab D
set   120:  80063    8008f    8006b D 800a2 D
set   121:  8006a    800a2 D 800ab D 80039
set   122:  8006c D 8006a D 8006b D 800a2 D
set   123:  8006c D 800a2 D 8003d    800ab D
set   124:  80069 D 800a2 D 8006c D 8003d
set   125:  800a2 D 80039    800ab D 800aa D
set   126:  80065 D 80069 D 800a2 D 80039
set   127:  80065 D 800a2 D 800ab D 800aa D
===== Simulation results (raw) =====
a. number of L1 reads: 63640
b. number of L1 read misses: 10728
c. number of L1 writes: 36360
d. number of L1 write misses: 8493
e. L1 miss rate: 0.1922
f. number of searches of alternate set S' within L1: 0
g. number of swaps within L1: 0
h. number of spills within L1: 0
```

```
i. L1 primary-set miss rate: 0.0000
j. number of writebacks from L1: 9802
k. number of cold misses in L1: 4713
l. number of capacity misses in L1: 8304
m. number of conflict misses in L1: 6204
n. number of L2 reads: 19221
o. number of L2 read misses: 5945
p. number of L2 writes: 9802
q. number of L2 write misses:   0
r. L2 miss rate: 0.3093
s. number of searches of alternate set S' within L2: 0
t. number of searches of alternate set S' within L2 (instigated by L2
reads only): 0
u. number of swaps within L2: 0
v. number of spills within L2: 0
w. L2 primary-set miss rate: 0.0000
x. number of writebacks from L2:   4050
y. number of cold misses in L2: 4713
z. number of capacity misses in L2: 915
aa. number of conflict misses in L2: 317
bb. total memory traffic: 9995
===== Simulation results (performance) =====
L1 cacti results: Accesstime=0.1203, Energy=0.0015, Area=0.0126
L2 cacti results: Accesstime=0.2290, Energy=0.0067, Area=0.0665
1. Total Access Time (ns):  76474.1562
2. Average Access Time (ns): 0.7647
3. Total Energy (nJ): 909.9084
4. Energy-Delay Product (nJ*ns): 69584476.1018
5. Area (mm^2): 0.0791
```

4)

```
===== Simulator configuration =====
BLOCKSIZE:  16
L1_SIZE: 1024
L1_ASSOC:   2
L1_PSEUDO-ASSOC-EN:  0
L2_SIZE: 8192
L2_ASSOC:   4
L2_PSEUDO-ASSOC-EN:  0
trace_file: gcc_trace.txt
===== L1 contents =====
set   0:  20028d D 20018a
set   1:  20028d D 20028e D
set   2:  2001c1 D 200153 D
set   3:  20028d D 20013b
set   4:  200223 D 20028d
set   5:  2001c1    200149
set   6:  20028d D 20028e D
set   7:  20018a    2001ac D
set   8:  20018f D 20018a
set   9:  20018f D 2000f9
set   10:  20017a    2000fa
set   11:  200009    20018a
set   12:  200009    20028d D
set   13:  200009    2000f9
```

```
set   14:  200009    2001ac
set   15:  200009    2001b2 D
set   16:  200009    3d819c D
set   17:  200009    20017b D
set   18:  200009    2000fa
set   19:  200009    2001b2 D
set   20:  200009    2000fa
set   21:  200009    200214
set   22:  200009    20023f
set   23:  2001ab    20013a
set   24:  20018f D 2001f2
set   25:  2001aa    2001ab
set   26:  20028d D 20018d D
set   27:  20028d D 20018d D
set   28:  20013a    20028d D
set   29:  20013a    20018d D
set   30:  20028c D 20018d D
set   31:  2001f8 D 20028c D
===== L2 contents =====
set   0:  80066 D 800a3 D 800ac D 800ab D
set   1:  80066 D 8007d D 800a3 D 800ac D
set   2:  80066 D 8007e D 8006d D 800a3 D
set   3:  80066 D 800a3 D 800aa D 800a7 D
set   4:  80066 D 800a3 D 800aa D 800ac D
set   5:  80066 D 800a3 D 800aa D 800ac D
set   6:  800a3 D 800ac D 800ab D 800a6 D
set   7:  8006b    8006c D 800a3 D 800ac D
set   8:  800a3 D 8006b D 800ac D 800ab D
set   9:  800a3 D 8003e    800ac D 800ab D
set   10:  800a3 D 800ac D 800ab D 800aa D
set   11:  800a3 D 800ac D 800ab D 800aa D
set   12:  8006b D 800a3 D 800ac D 800ab D
set   13:  800a3 D 80079 D 8006f D 800ac D
set   14:  8006b    800a3 D 800ac D 800ab D
set   15:  800a3 D 800ac D 800ab D 800aa D
set   16:  800a3 D f6067    800ac D 800ab D
set   17:  800a3 D 8007f D 800ac D 800ab D
set   18:  800a3 D 800ac D 800ab D 800aa D
set   19:  f6067 D 800a3 D 800ac D 800a8 D
set   20:  8007f D 80085 D 800a3 D 800ac D
set   21:  80085 D 800a3 D 800ac D 800a8 D
set   22:  80085 D 800a3 D 800ac D 800ab D
set   23:  800a3 D f6067 D 800ac D 800a7 D
set   24:  800a3 D 8003e    800ac D 800a7 D
set   25:  800a3 D 8007d D 800ac D 800ab D
set   26:  800a3 D 800ac D 800ab D 800aa D
set   27:  800a3 D 800ac D 800ab D 800aa D
set   28:  800a3 D 800ac D 8007f D 800ab D
set   29:  800a3 D 8006a D 80074 D 800ac D
set   30:  800a3    800ac D 800ab D 8007f D
set   31:  8007e D 800a3 D 800ac D 800ab D
set   32:  800a3 D 80074 D f6067 D 800ac D
set   33:  80074 D 800a3    800ac D 800ab D
set   34:  80070    800a3 D 80074 D 800ac D
set   35:  800a3 D 800ac D 800a9 D 800a8 D
set   36:  800a3 D 80090    80070 D 800ac D
set   37:  80070 D 80052    800a3 D 8007f D
```

Sample cover page for Project #1. Created 2/1/10.

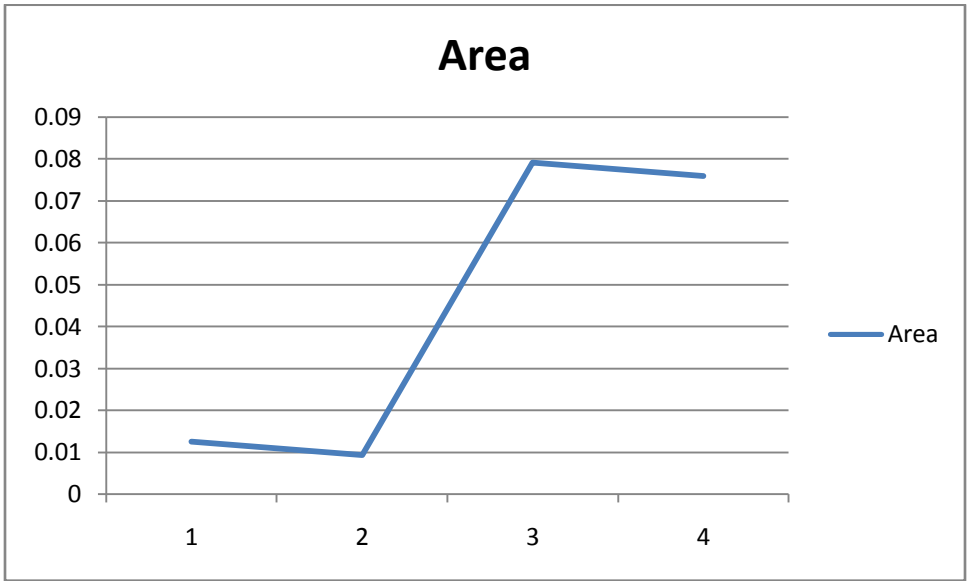
```
set   38:  80070 D 800a3    8006f D 8007f D
set   39:  800a3 D 80070 D 800ac D 800a9 D
set   40:  800a3 D 80052    8005a D 800a9 D
set   41:  8003e    800a3 D 800ac D 8006b D
set   42:  800a3 D 8006b D 800ab D 800aa D
set   43:  80002    800a3 D 800ab D 80070 D
set   44:  80002    800a3    8006b D 800ab D
set   45:  80002    8003e    800a3 D 800ab D
set   46:  80002    800a3 D 80052    800ab D
set   47:  80002    800a3 D 8003e    800ab D
set   48:  80002    8003e    800a3 D 800ab D
set   49:  80002    800a3 D 80052    8005e D
set   50:  80002    800a3 D 8003e    800ab D
set   51:  80002    800a3 D 8007f D 800a6 D
set   52:  80002    800a3 D 800a9 D 800a8 D
set   53:  80002    800a3 D 800a9 D 800a8 D
set   54:  80002    800a3 D 800ab D 800a2 D
set   55:  800a3 D 80063 D 800ab D 800a2 D
set   56:  800a3 D 80063 D 80062 D 8006b D
set   57:  800a3 D 80063 D 80062    800ab D
set   58:  800a3    80063    80074 D 8006f D
set   59:  800a3    80063    80074 D 8007d D
set   60:  80063 D 800a3    8006b D 8007f D
set   61:  800a3 D 80063 D 8007d D 8006b D
set   62:  80063    800a3 D 800ab D 800a2 D
set   63:  80063 D 800a3 D 8006a D 80074 D
set   64:  80062    800a3 D 8005e D 800ab D
set   65:  800a3    800ab D 800a2 D 800aa D
set   66:  800a3 D 800ab D 800a2 D 800aa D
set   67:  800a3 D 800a8 D 800ab D 800a7 D
set   68:  80062    800a3 D 800a8 D 800ab D
set   69:  80062    800a3 D 800a8 D 800ab D
set   70:  800a3    800ab D 800a2 D 800aa D
set   71:  80062    800a3 D 8005e D 800a8 D
set   72:  80062    800a3 D 800a8 D 800ab D
set   73:  8005e D 800a3 D 800ab D 800a2 D
set   74:  8005e    800a3 D 8003e    80062
set   75:  80062    8006c D 800ab D 800a2 D
set   76:  8006c D 800ab D 800a2 D 800aa D
set   77:  80062    8006c D 800ab D 800a2 D
set   78:  8003e    8006c D 8007d D 8005e
set   79:  8006c    800ab D 800a2 D 8003e
set   80:  8006c D 800ab D 800a2 D 800aa D
set   81:  8003e    8006c D 8006a    800ab D
set   82:  8003e    8006c D 8006a    800ab D
set   83:  8006c    8006a    800a6 D 800a9 D
set   84:  8003e    8006a    8006c D 800a9 D
set   85:  8006a    8006b    800a9 D 800a8 D
set   86:  8006a    800ab D 800a2 D 800aa D
set   87:  8006a    8004e    800a9 D 800a8 D
set   88:  80062 D 8007c    8004e    8006a
set   89:  8006a    800ab D 800a2 D 8007c
set   90:  8006c D 800a2 D 800ab D 800aa D
set   91:  8004e    8007f D 80088 D 800a2 D
set   92:  8004e    800a2 D 800ab D 800aa D
set   93:  8004e    8006c D 800a2 D 800ab D
set   94:  80088 D 800a2 D 800ab D 800aa D
```

Sample cover page for Project #1. Created 2/1/10.

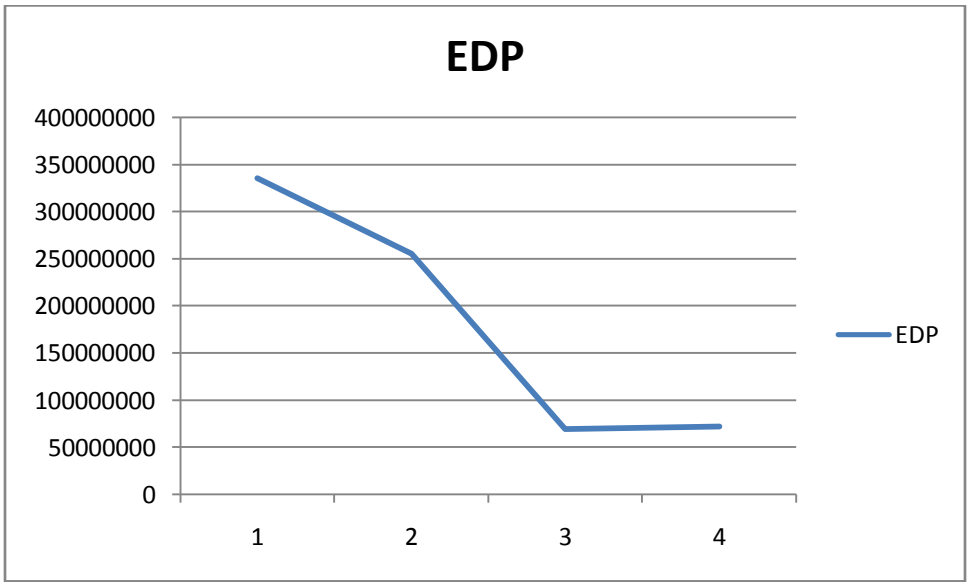
```
set   95:  8004e    80088 D 800a2 D 800ab D
set   96:  80073    800a2 D 800ab D 800aa D
set   97:  8006a    80088 D 800a2 D 800ab D
set   98:  80054 D 8004e    8003e    800a2 D
set   99:  8004e    800a2 D 800a8 D 800ab D
set   100:  80088 D 8007d D 800a2 D 800a8 D
set   101:  8004e    800a2 D 800a8 D 800ab D
set   102:  800a2 D 800ab D 800aa D 800a9 D
set   103:  800a2 D 800ab D 800aa D 800a5 D
set   104:  80063 D 8008f    8007c D 800a2 D
set   105:  80063 D 8008f    800a9 D 800a2 D
set   106:  8008f    80063 D 800a2 D 800ab D
set   107:  8008f    80063 D 800a2 D 800ab D
set   108:  8008f    80088 D 800a2 D 800ab D
set   109:  8008f    800a2 D 800ab D 80073 D
set   110:  8008f    800a2 D 800ab D 800aa D
set   111:  8008f    8006e D 8005e D 8006b D
set   112:  8008f    8005e D 8006e D 800a2 D
set   113:  8005e    8008f    8007d D 800a2 D
set   114:  8008f    800a2 D 800ab D 800aa D
set   115:  8008f    8005e D 800a6 D 800a2 D
set   116:  8008f    80063 D 800a2 D 8003d
set   117:  8008f    8006a D 80063 D 800a2 D
set   118:  8008f    800a2 D 800ab D 800aa D
set   119:  8006a    8008f    800a2 D 800ab D
set   120:  80063    8008f    8006b D 800a2 D
set   121:  8006a    800a2 D 800ab D 8006b D
set   122:  8006c D 8006a D 8006b D 800a2 D
set   123:  8006c D 800a2 D 800ab D 8003d
set   124:  80069 D 800a2 D 8006c D 8003d
set   125:  800a2 D 800ab D 80039    800aa D
set   126:  80065 D 80069 D 800a2 D 800ab D
set   127:  80065 D 800a2 D 800ab D 800aa D
===== Simulation results (raw) =====
a. number of L1 reads: 63640
b. number of L1 read misses: 8322
c. number of L1 writes: 36360
d. number of L1 write misses: 7680
e. L1 miss rate: 0.1600
f. number of searches of alternate set S' within L1: 0
g. number of swaps within L1: 0
h. number of spills within L1: 0
i. L1 primary-set miss rate: 0.0000
j. number of writebacks from L1: 8696
k. number of cold misses in L1: 4713
l. number of capacity misses in L1: 8382
m. number of conflict misses in L1: 2907
n. number of L2 reads: 16002
o. number of L2 read misses: 5943
p. number of L2 writes: 8696
q. number of L2 write misses:   9
r. L2 miss rate: 0.3714
s. number of searches of alternate set S' within L2: 0
t. number of searches of alternate set S' within L2 (instigated by L2
reads only): 0
u. number of swaps within L2: 0
v. number of spills within L2: 0
```

```
w. L2 primary-set miss rate: 0.0000
x. number of writebacks from L2:   4041
y. number of cold misses in L2: 4713
z. number of capacity misses in L2: 904
aa. number of conflict misses in L2: 335
bb. total memory traffic: 9993
===== Simulation results (performance) =====
L1 cacti results: Accesstime=0.1544, Energy=0.0018, Area=0.0094
L2 cacti results: Accesstime=0.2290, Energy=0.0067, Area=0.0665
1. Total Access Time (ns):  79126.4453
2. Average Access Time (ns): 0.7913
3. Total Energy (nJ): 913.2368
4. Energy-Delay Product (nJ*ns): 72261178.1812
5. Area (mm^2): 0.0759
```

Comparison of the Area in mm^2 for 4 different simulated configuration.



- As we can observe from the graph, the area measurement given by the cacti tool varies dramatically as we change from one level to multiple levels.
- As we can see, the runs 1 and 2 donot have the L2 cache in the hierarchy.
- The runs 3 and 4 contain L2 cache in addition to L1 thereby increasing area.



The energy delay product, as given by the simulation results, is plotted above. As we observe from the graph , as we go on increasing associativity , the EDP drops linearly. Addition of L2 cache results in a sudden drop of EDP values. This is due to the fact that on addition of more modules in the hierarchy, while on one hand, the delay to search contents increases, the miss rates reduce and thereby reduce the delay dramatically. Thus overall EDP is reduced.

2. **From your thorough design space exploration, find the Best Memory Hierarchy for EDP**
(for Area ≤ Area Budget):

I have simulated 4 configurations above. From the results of these configurations, we observe that, the best memory hierarchy for the EDP would be the 3rd one that is the one with the following parameters.

```
===== Simulator configuration =====
BLOCKSIZE:  16
L1_SIZE: 1024
L1_ASSOC:   1
L1_PSEUDO-ASSOC-EN:  0
L2_SIZE: 8192
L2_ASSOC:   4
L2_PSEUDO-ASSOC-EN:  0
```

The reason behind this is simple. While the 1st configuration has no L2 cache, it has a higher missrate than the rest. Thus the delay in mem access is very high resulting in higher EDP.
In the second configuration, we increase the assoc to 2. This results in the increase of conflict misses on one hand, but on the other hand, because the blocks have two possible places to map to in a set, the net number of misses decrease. Thus the mem accesses also reduce thereby resulting in the decrease of delay. Thus the EDP decreases.

In the last config the EDP slightly increases. The reason behind this is that when we increase the assoc of L1 from 1 to 2, the number of misses reduce on one hand, but on the otherhand, the mapping function from the L1 to L2 changes, this results in the failure to correctly map conflict misses as would have been the case with a FA cache.

3. **From your thorough design space exploration, find the Best Memory Hierarchy for AAT**

Calculation of AAT:-

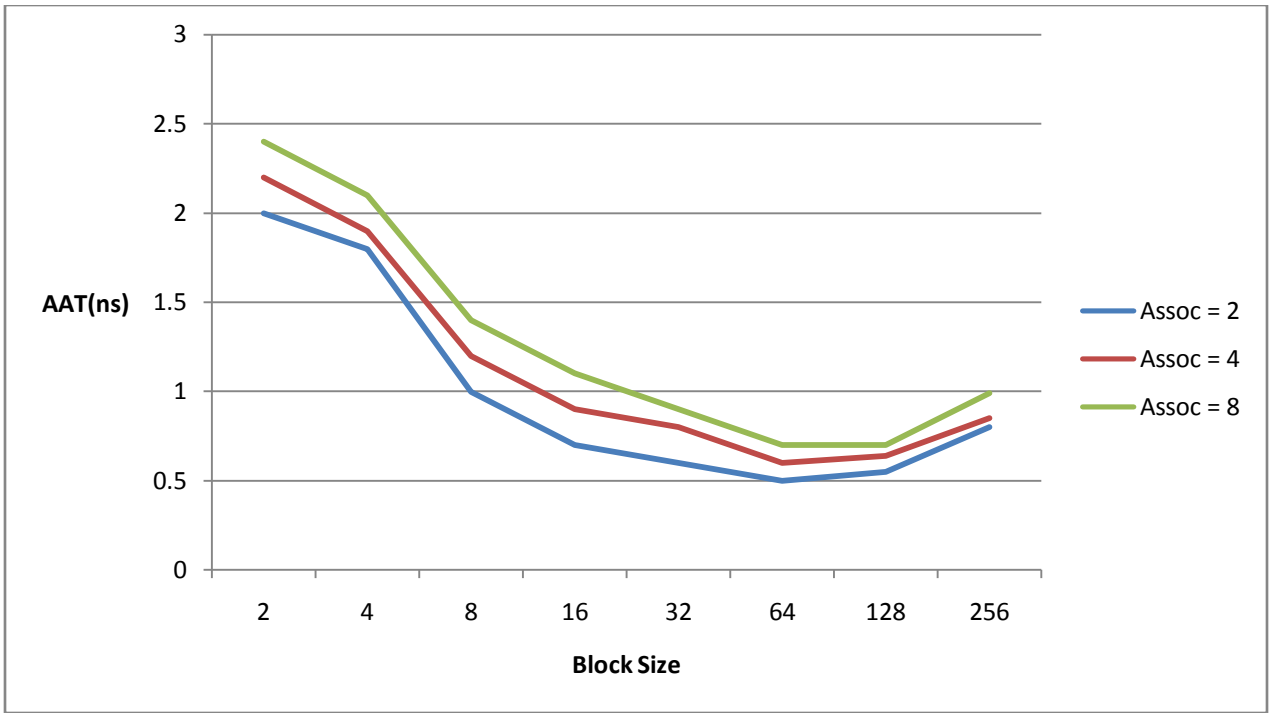
AAT(Average Access Time) for L1 only configuration is calculated as follows:-

$$\text{Total access time} = (\text{L1 reads} + \text{L1 writes}) \cdot HT_{L1} + (\text{alternate searches in L1}) \cdot HT_{L1} + (\text{L1 read misses} + \text{L1 write misses}) \cdot \text{Miss\_Penalty}$$

$$\text{Average access time (AAT)} = \frac{\text{Total access time}}{(\text{L1 reads} + \text{L1 writes})}$$

$$\begin{aligned} AAT &= HT_{L1} + \left(\frac{\text{alternate searches in L1}}{\text{L1 reads} + \text{L1 writes}}\right) \cdot HT_{L1} + \left(\frac{\text{L1 read misses} + \text{L1 write misses}}{\text{L1 reads} + \text{L1 writes}}\right) \cdot \text{Miss\_Penalty} \\ &= HT_{L1} + pMR_{L1} \cdot HT_{L1} + MR_{L1} \cdot \text{Miss\_Penalty} \\ &= (1 + pMR_{L1}) \cdot HT_{L1} + MR_{L1} \cdot \text{Miss\_Penalty} \end{aligned}$$

L1 cache performance for different values of associativity and block sizes
Consider an L1 cache of size 1024KB with LRU replacement policy. Following data shows the performance of such a cache for different block sizes and different associativity values. This data is for the traces given in “gcc_trace.txt”. As shown in the figure, the Average Access Time for CPU decreases rapidly as block size increases. At a certain block size, AAT gets minimum value and tends to increase slowly if block size is further increased. From the chart, we observe that when the block size is about 128, then values of AAT start to increase gradually and further increase in block sizes result in increase of AAT. Also we observe that as assoc increases from 2 to 8, the AAT increases by an insignificant amount indicating that the assoc doesn’t affect the AAT that much.



Thus the best possible configuration for AAT would be the one with the block size = 64 and the associativity as high as possible.

Compare and contrast the Best Memory Hierarchy for EDP vs. the Best Memory Hierarchy for AAT:

The best configurations for the EDP vs AAT are kind of similar. The only difference between the two is the point at which the graphs curve.
For EDP, at associativity = 1 for L1 and 4 for L2, the curve is at minimum thereby it being the best configuration.
For AAT, the best configuration happens at very high values of associativity.