STM32MP1

Hardware design made easy

STM32 MP1

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Agenda

Presentation

15 min

- Main Challenge for HW
- Package optimized to ease HW
- Power Management IC companion STPMIC1
- DDR ROUTING
- Documents
- Reference Boards

Main challenges for HW

Platform HW definition should be simple

- ...

PCB routing should allow low complexity PCB stackup and technology

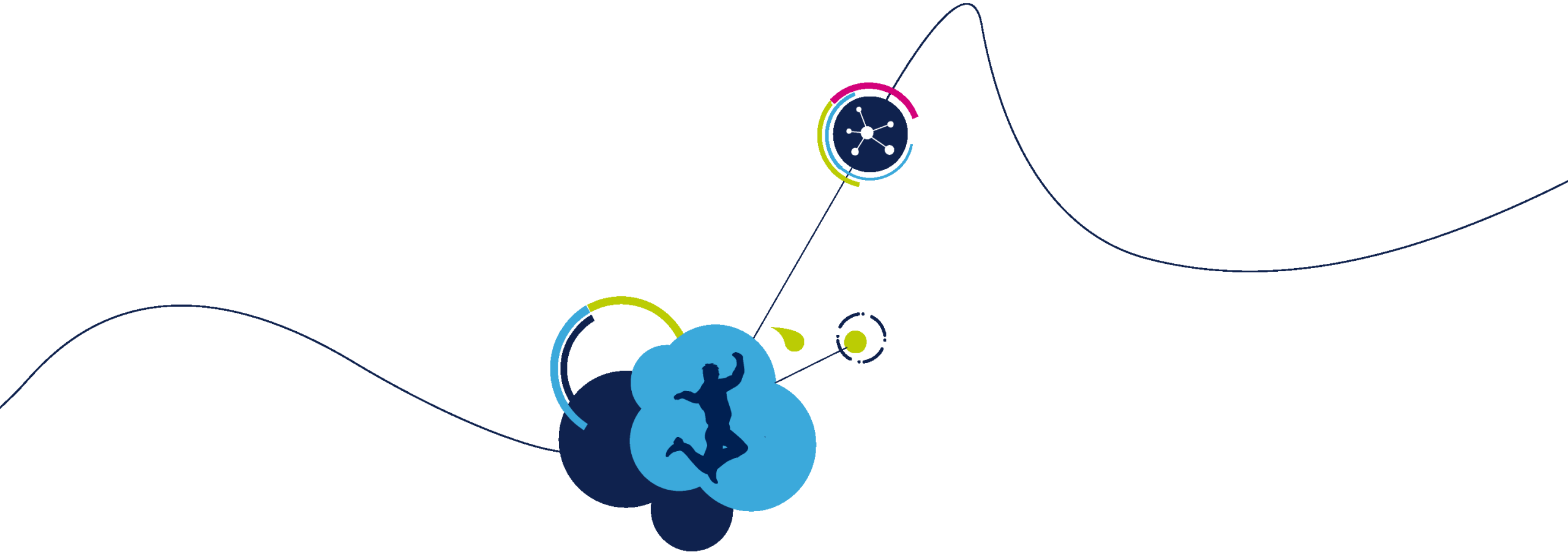
- ...

Platform supplies definition should be as simple as possible

- ...

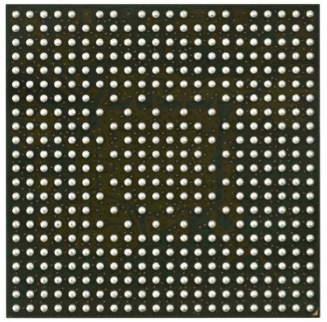
Signal integrity should be easy to manage / test

- ...



Package optimized to ease HW

Packages

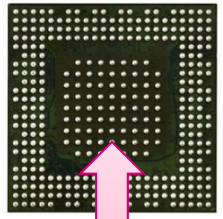


Consumer / DDR3/3L:

Full Features:

LFBGA448 18x18mm pitch 0.8
DDR3/3L 32-bits I/F
176 GPIOs
6 layers PTH PCB

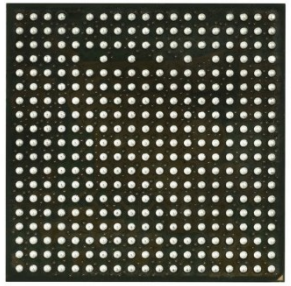
Consumer / LPDDR2/3 & DDR3/3L:



TFBGA361 12x12mm pitch 0.5
LPDDR2/3, DDR3/3L 32-bits I/F
148 GPIOs
4 layers PTH + laser via PCB

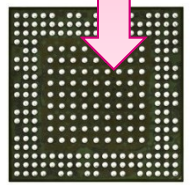
Pitch 0.65 on inner ball matrix to ease PCB supply routing

Low cost:



LFBGA354 16x16mm pitch 0.8
DDR3/3L 16-bits I/F
98 GPIOs
4 layers PTH PCB

TFBGA257 10x10mm pitch 0.5
LPDDR2/3, DDR3/3L 16-bits I/F
98 GPIOs
4 layers PTH PCB



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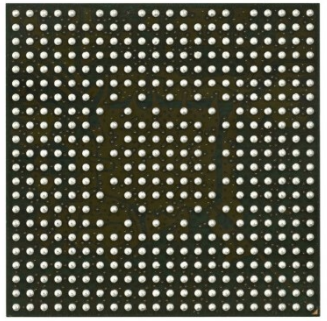
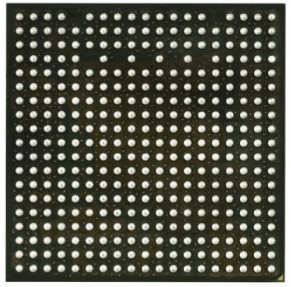
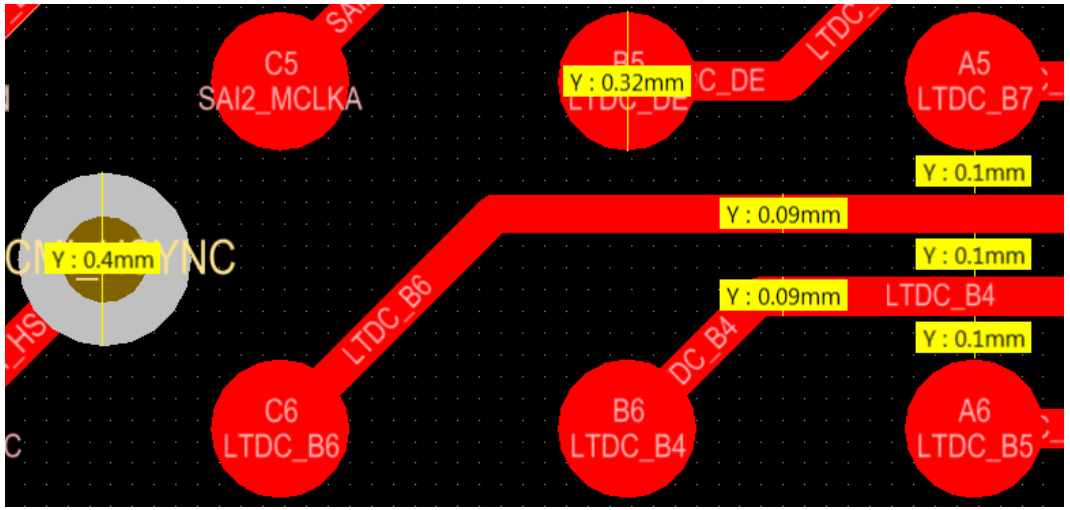
PCB techno for 0.8mm pitch packages

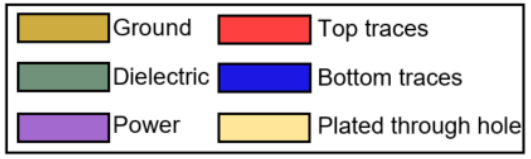


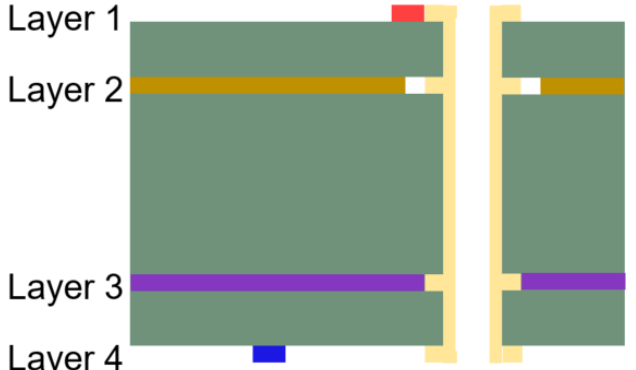


Package	PCB layers	VIA	Trace width / isolation
LFBGA448 18x18	6	Plated Through Hole ø 400 µm	90µm / 100µm
LFBGA354 16x16	4	Plated Through Hole ø 400 µm	90µm / 100µm



2 traces between 2 balls





Printed Circuit Board

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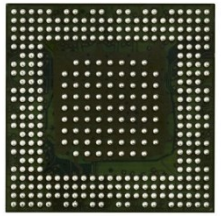
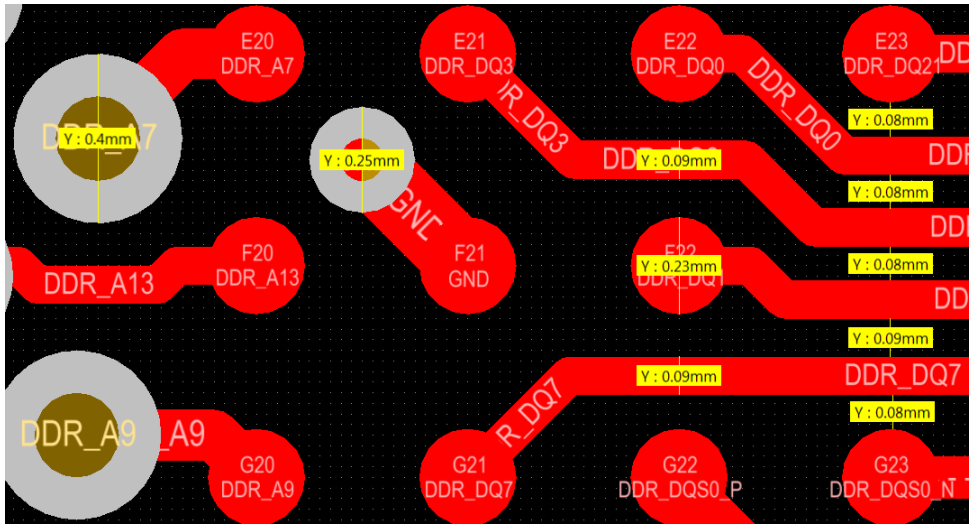
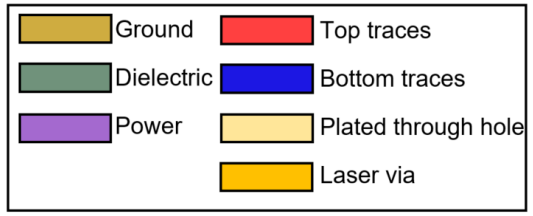
PCB techno for 0.5/0.65mm pitch 12x12 package

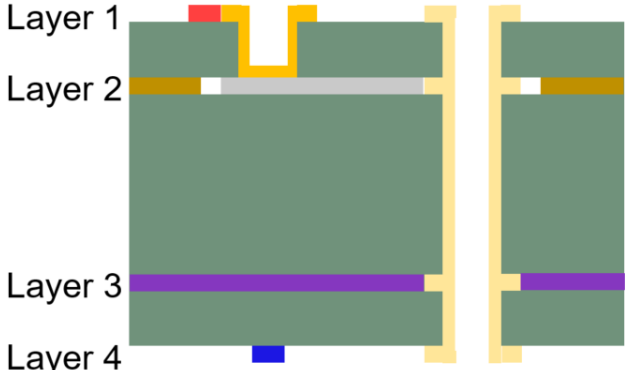


Package	PCB layers	VIA	Trace width / isolation
TFBGA361 12x12	4	Plated Through Hole ø 400 µm and Laser via ø 250 µm	90µm / 80µm



4 outer peripheral rings
One ball removed to escape 4 traces
Some balls are escaped with laser via on top layer





Printed Circuit Board

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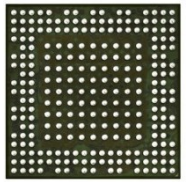
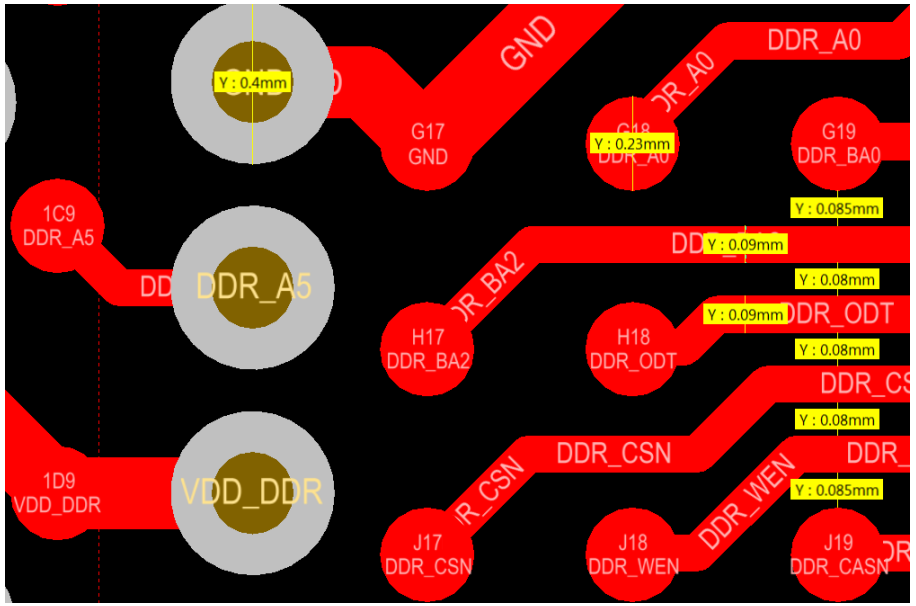
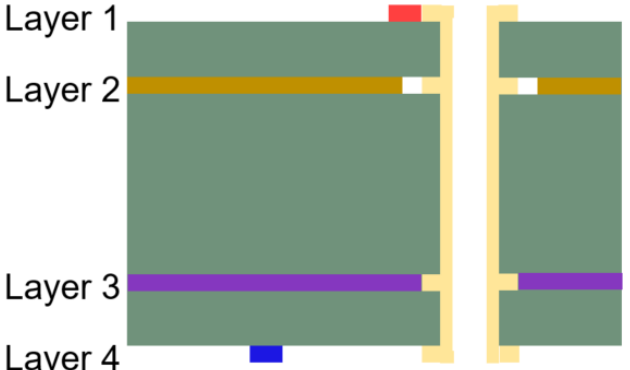
PCB techno for 0.5/0.65mm pitch 10x10 package

Package	PCB layers	VIA	Trace width / isolation
TFBGA257 10x10	4	Plated Through Hole ø 400 µm	90µm / 80µm

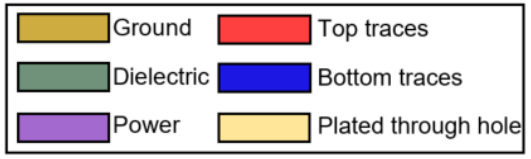




3 outer peripheral rings. One ball removed to escape 4 traces
The 3rd outer peripheral ring can be escape without laser via



Printed Circuit Board



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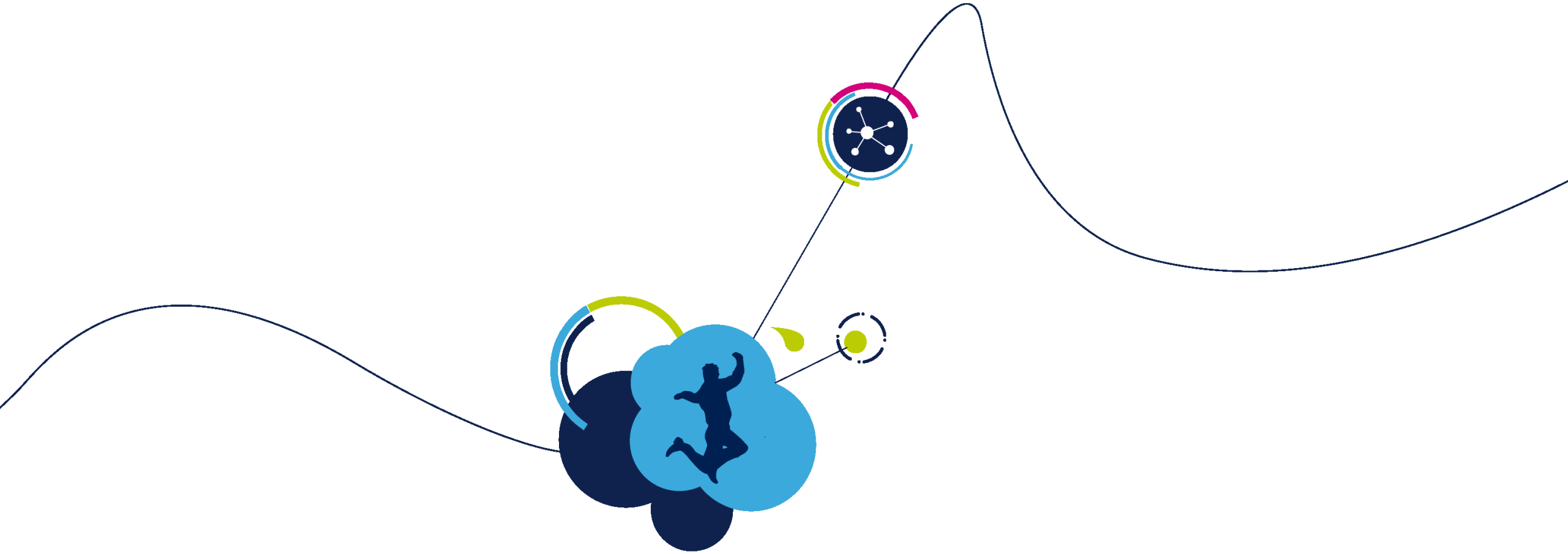
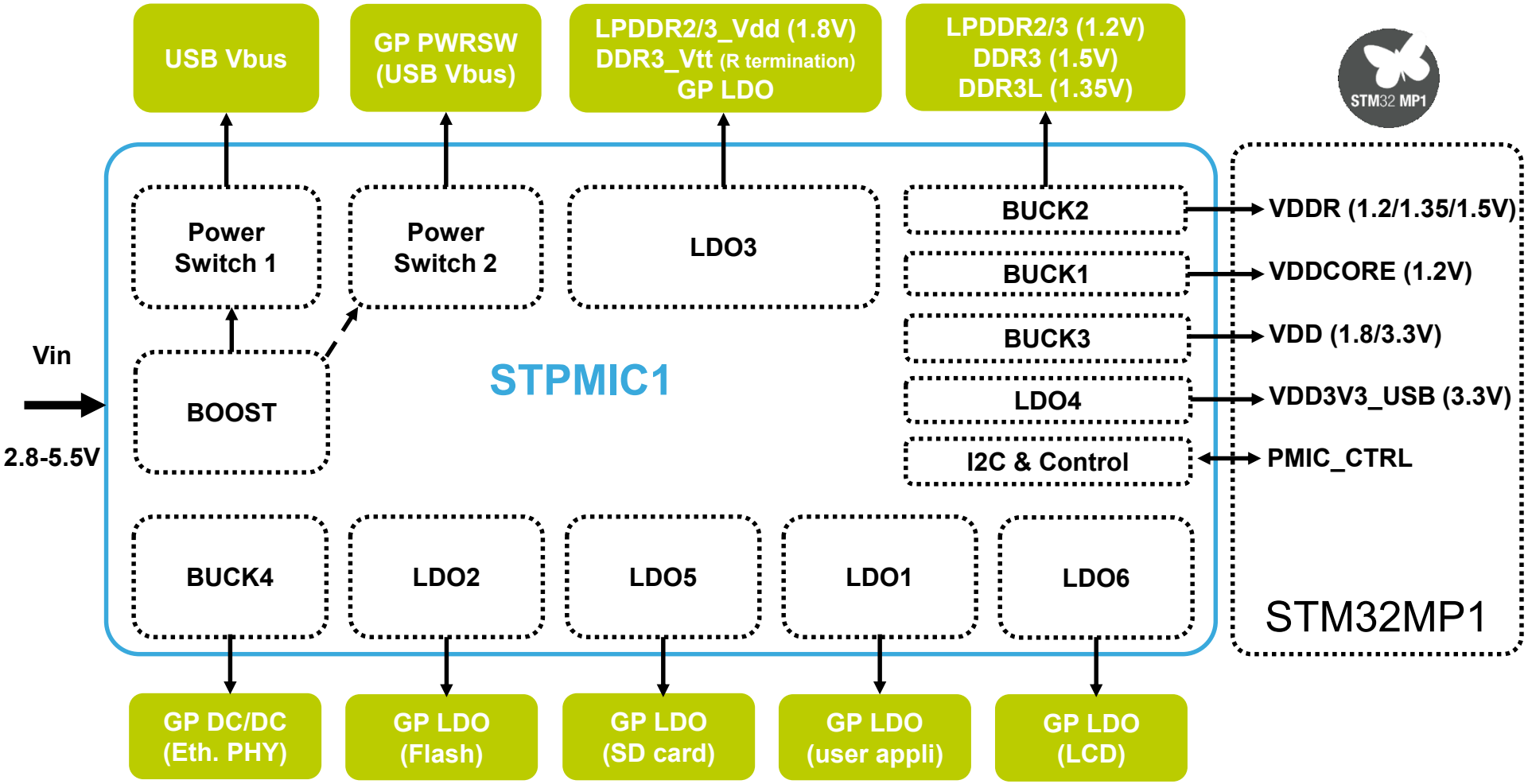


Power Management IC companion STPMIC1

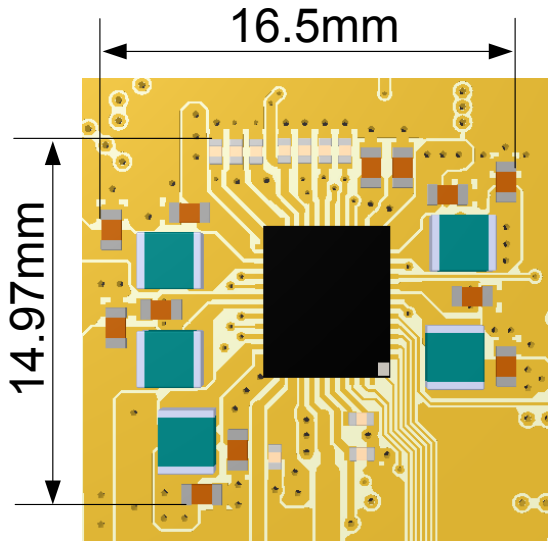
STM32MP1 with STPMIC1

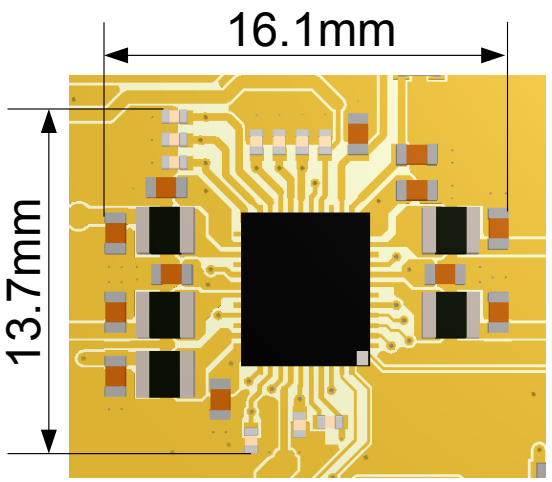


➔ STPMIC1 save external Bucks and LDOs on PCB for Typical Applications

STPMIC1 BOM options

STPMIC1 components	Number of different Passive References	Area	Relative Cost
Industrial profile (**full** buck converter performance and 2,5mm x 2,0mm inductors package)	7	247 mm²	*reference*
*Consumer profile / **low cost*** *(half buck converter performance and 2,5mm x 2,0mm inductors package)*	*6*	*247 mm²*	***- 40%***
Consumer profile / **high integration** (half buck converter performance and 2,0mm x 1,6mm inductors package)	6	**220** mm²	- 20%





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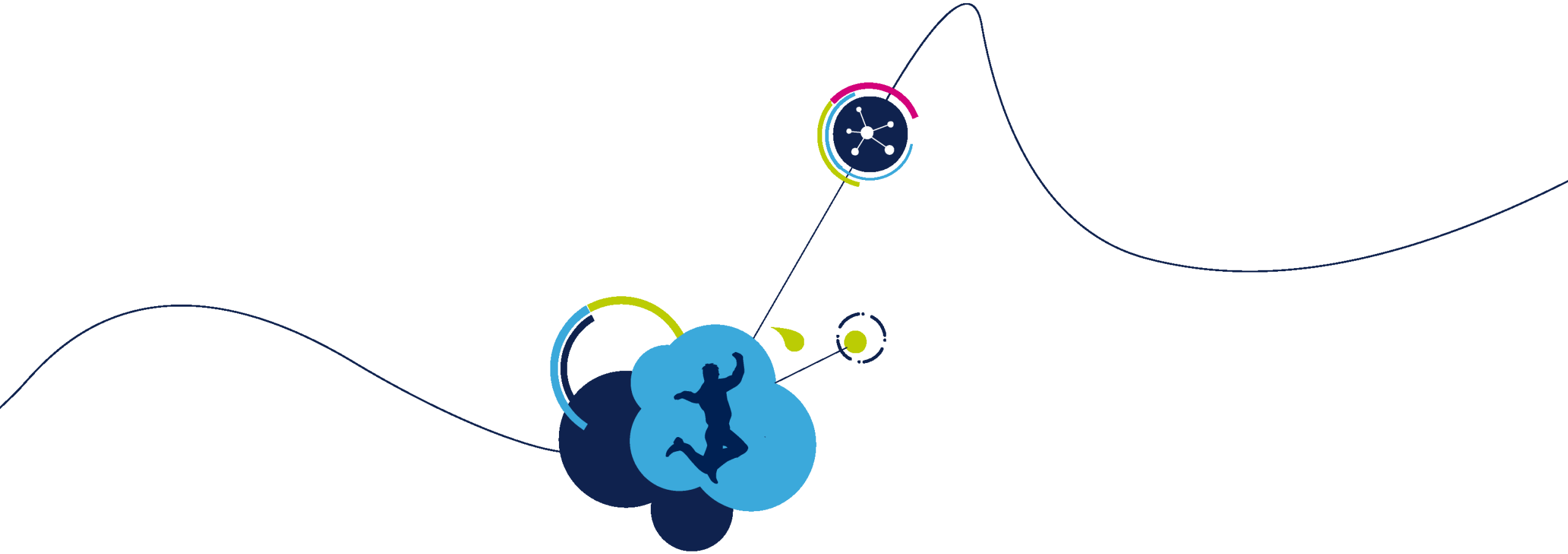
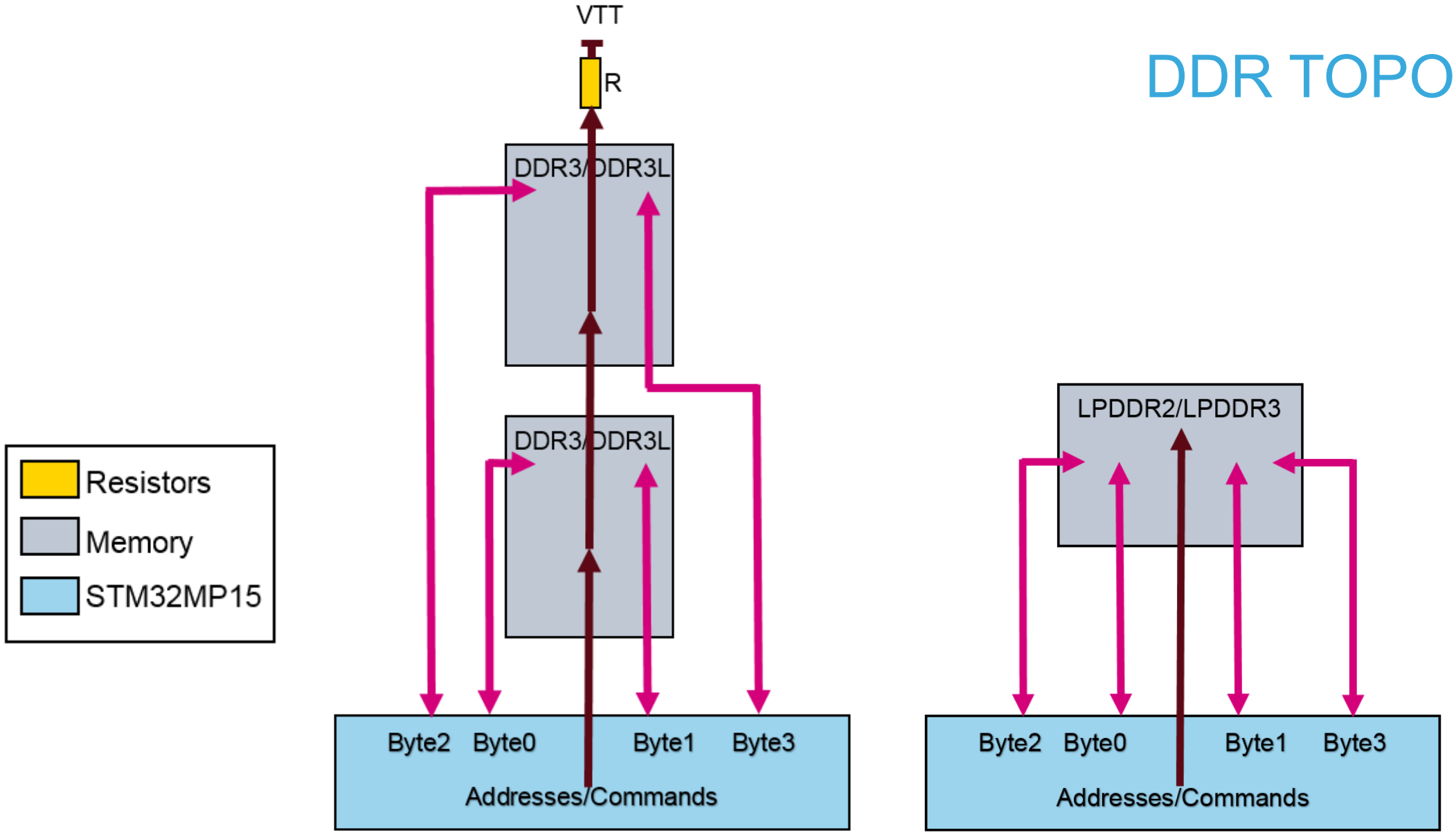


DDR ROUTING

DDR TOPOLOGY



FLY-BY

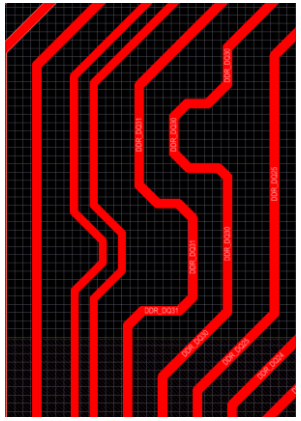
POINT TO POINT

DDR length equalization

- Timing constraints request trace length equalization including package and PCB trace lengths

- In order to facilitate the layout of DDR traces, a excel file is proposed. It calculates the total length *based on information from package and PCB*. It verifies that rules are respected

https://www.st.com/resource/en/board_manufacturing_specification/stm32mp1_seriesddrmemory_routing_guidelines_examples.zip



	NET NAME	STM32MP15XXAD LENGTH (mm)	STM32MP15XXAD to memory (mm)	TOTAL LENGTH (mm)	DELTA WITH ((DQSn_P+DQSn_N)/2) MAX: +/- 1.016 mm	DELTA WITH ((CLK_P+CLK_N)/2): from -15 to 0 mm
Byte 0	DQ0	4.03	43.34	47.37	0.195	
	DQ1	4.29	42.26	46.55	-0.625	
	DQ2	4.99	41.55	46.54	-0.635	
	DQ3	4.93	41.4	46.33	-0.845	
	DQ4	3.65	42.93	46.58	-0.595	
	DQ5	3.38	43.35	46.73	-0.445	
	DQ6	3.81	42.6	46.41	-0.765	
	DQ7	4.35	42.08	46.43	-0.745	
	DQM0	3.79	42.97	46.76	-0.415	
	DQS0_P	4.49	42.56	47.05		-0.105
	DQS0_N	4	43.3	47.3		
Byte 1	DQ8	3.47	43.42	46.89	-0.02	
	DQ9	3.68	42.79	46.47	-0.44	
	DQ10	3.44	43.17	46.61	-0.3	
	DQ11	3.94	42.62	46.56	-0.35	
	DQ12	3.83	42.75	46.58	-0.33	
	DQ13	3.23	43.23	46.46	-0.45	
	DQ14	4.41	42.21	46.62	-0.29	
	DQ15	3.44	42.96	46.4	-0.51	
	DQM1	4.7	41.83	46.53	-0.38	
	DQS1_P	4.12	43.08	47.2		-0.37
	DQS1_N	3.4	43.22	46.62		

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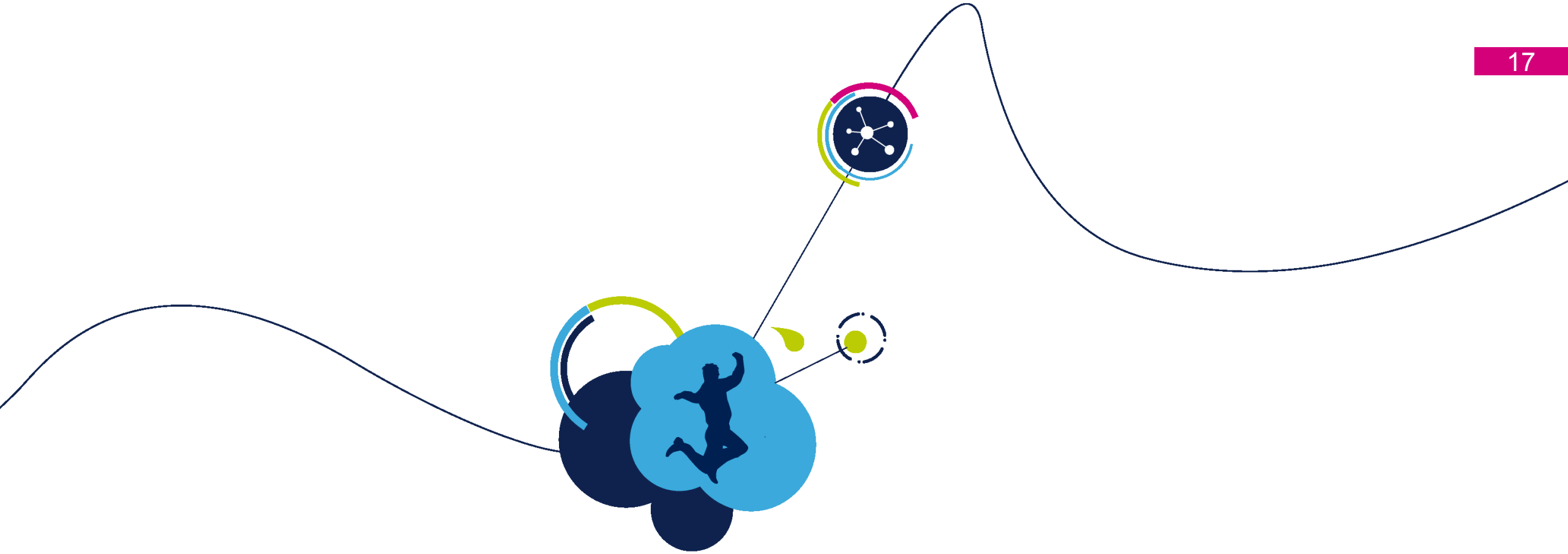
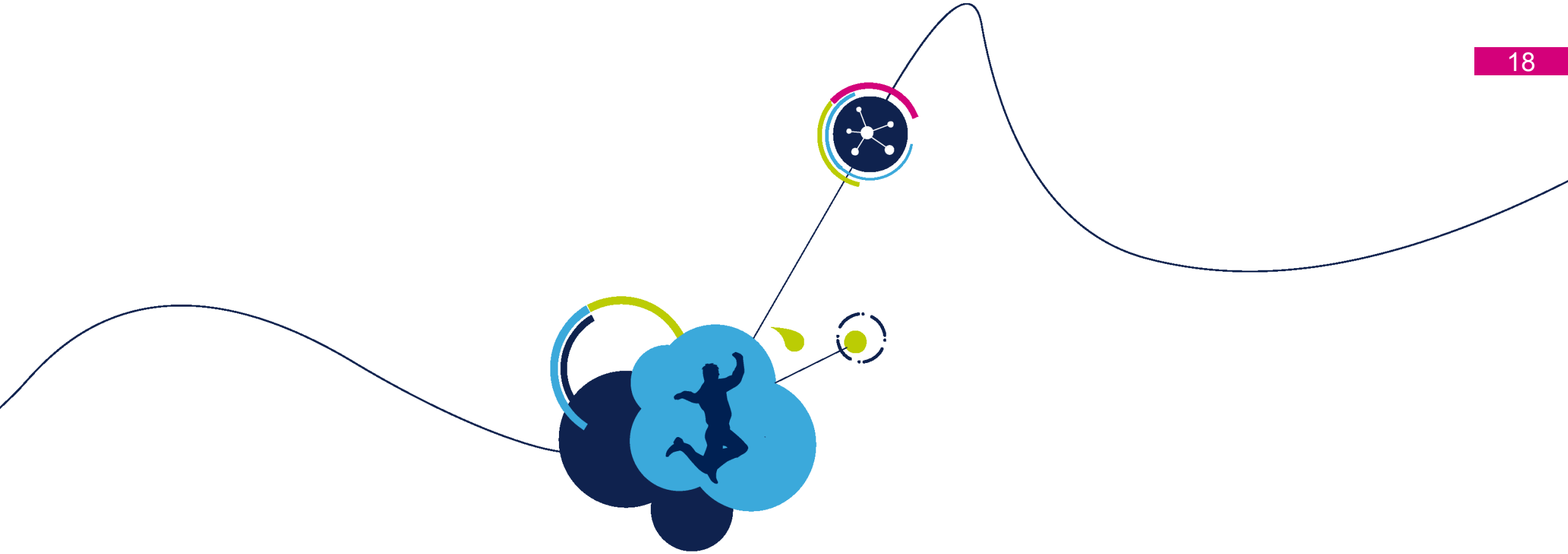


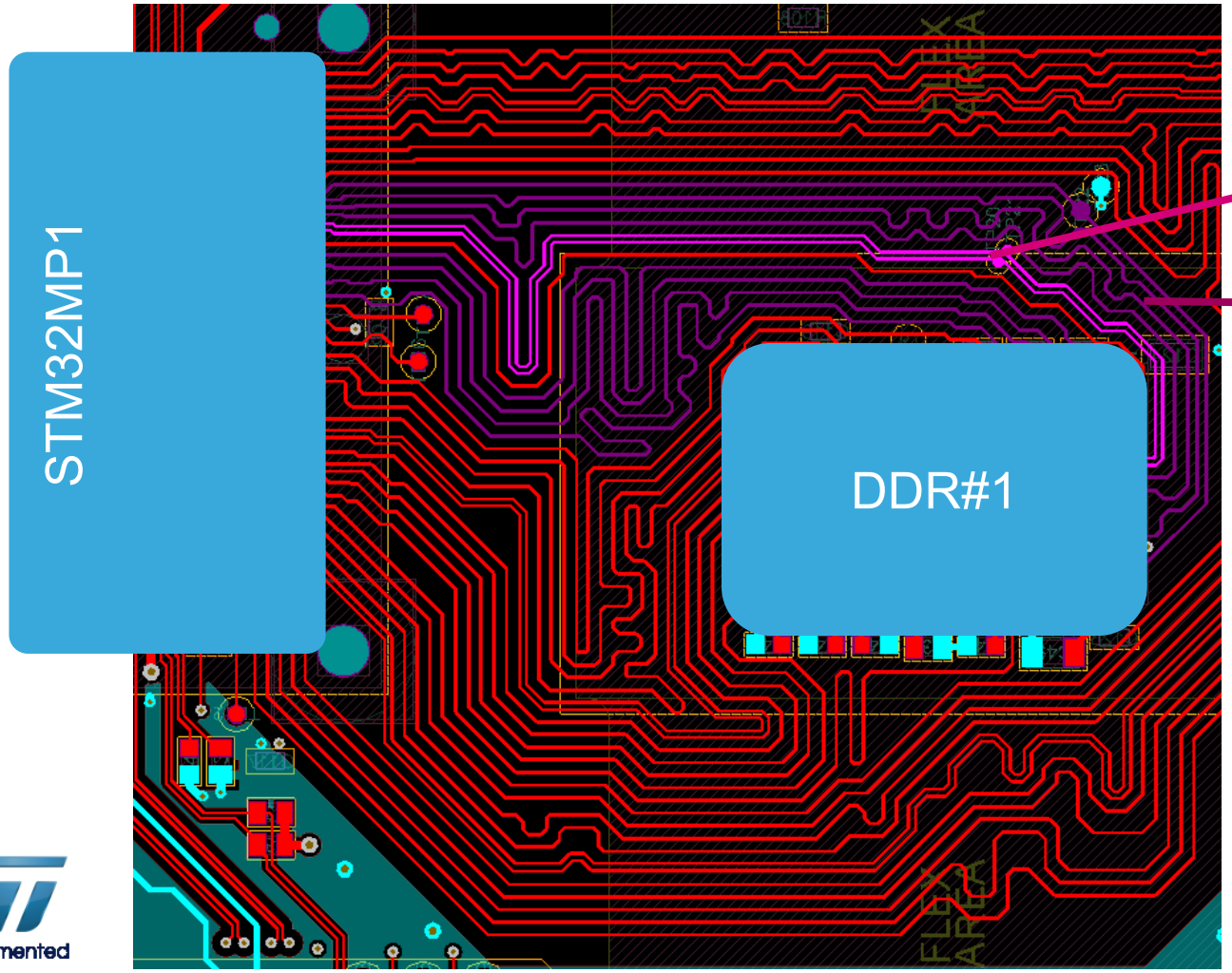
DDR tool suite



DDR tuning - Technical information

Lane delay

- Example of DDR Byte0 tunable signals



DQS0N / DQS0P signals

DQ0[0:7] byte lane

Constrained signals length
(e.g. +/-1mm within all signals
in a byte including DQS)

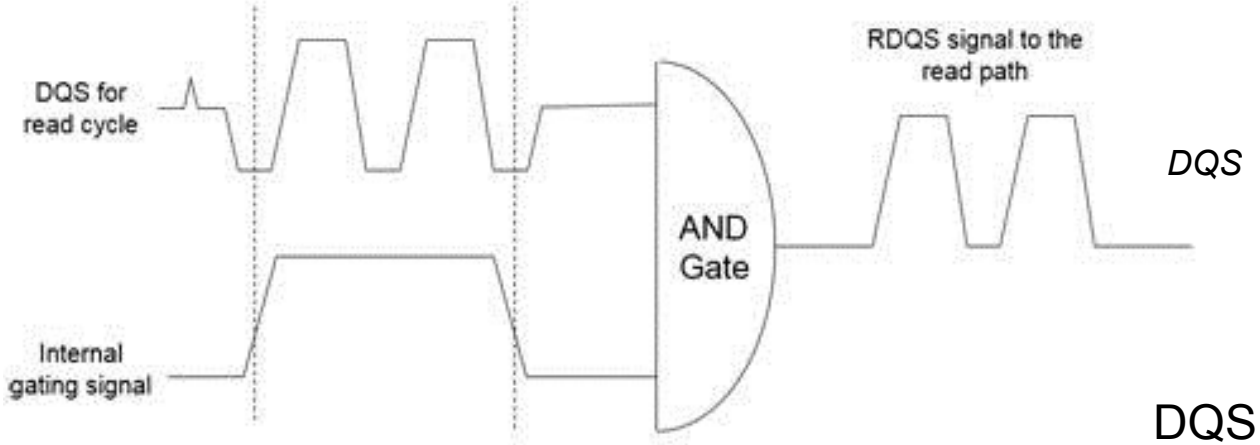
Length influences
the round trip delay

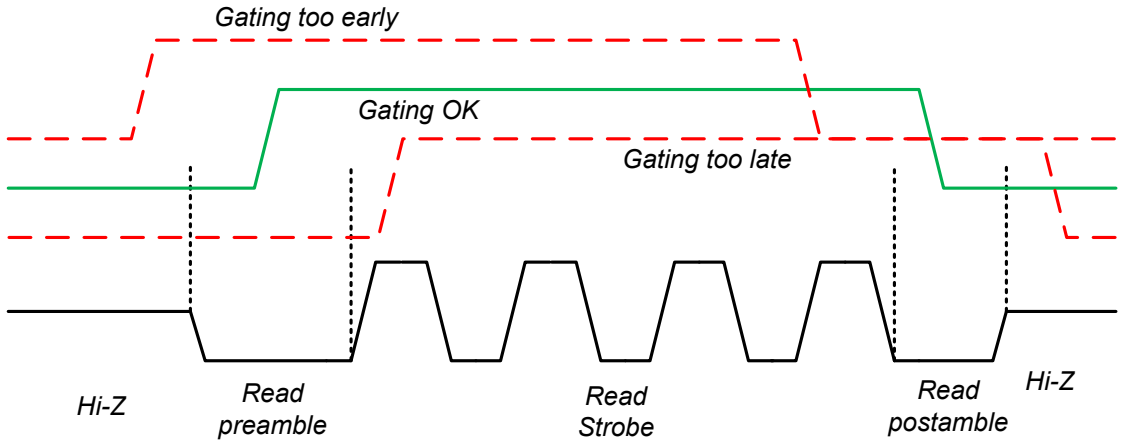
DDR tuning

- DDR tuning: **Read DQS gating training**

Read DQS gating

➢ *The purpose read DQS gating training is to adjust the timing of internal gating signal for DQS signal so that pseudo edges may occur due to glitches, post/preamble periods are eliminated.*



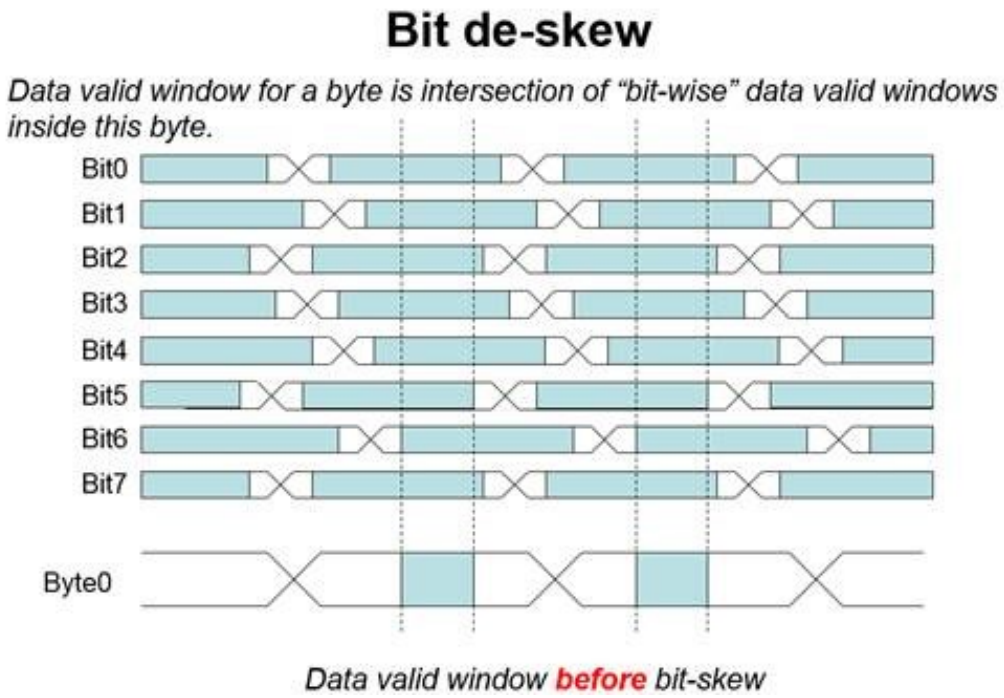


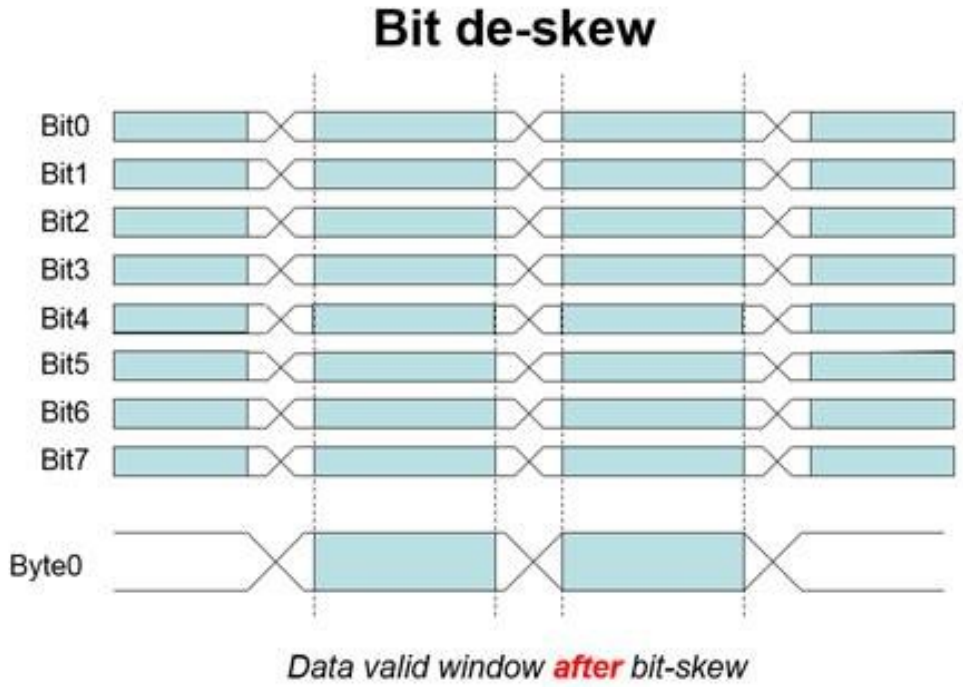
DQS gating position is depending on the round trip delay.

Read DQS signal is an input signal

DDR tuning

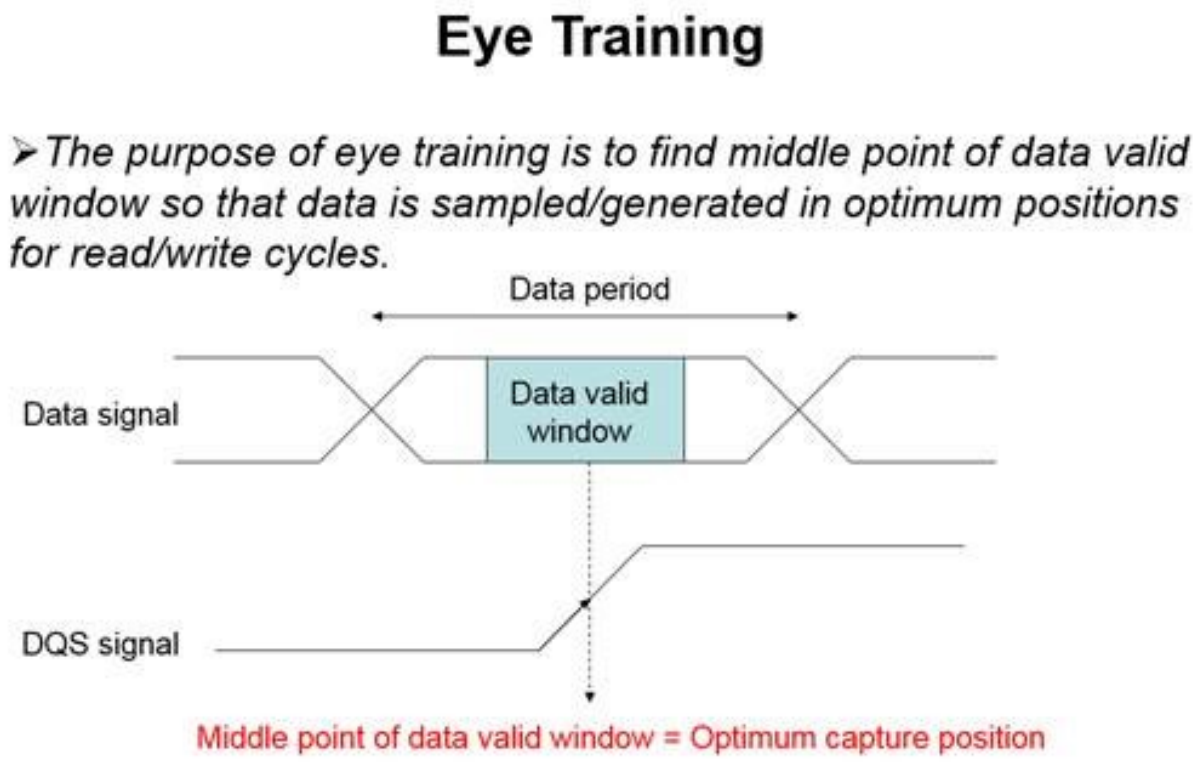
- DDR tuning: **Data Bit deskew**





  - Delay to be applied to each data line is computed based on results of several iteration DDR suite algo. This explains the step duration

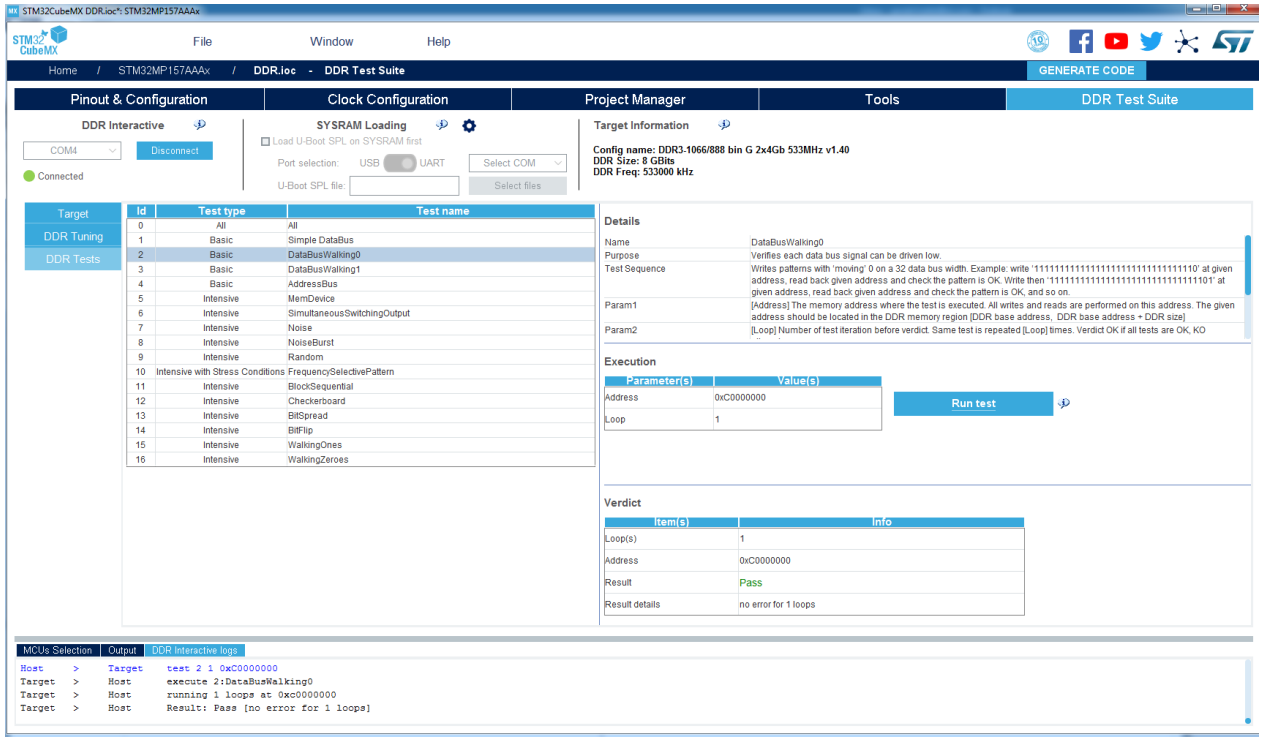
- DDR tuning: **Read Eye Training**



Read Eye training is intended for *Read access*

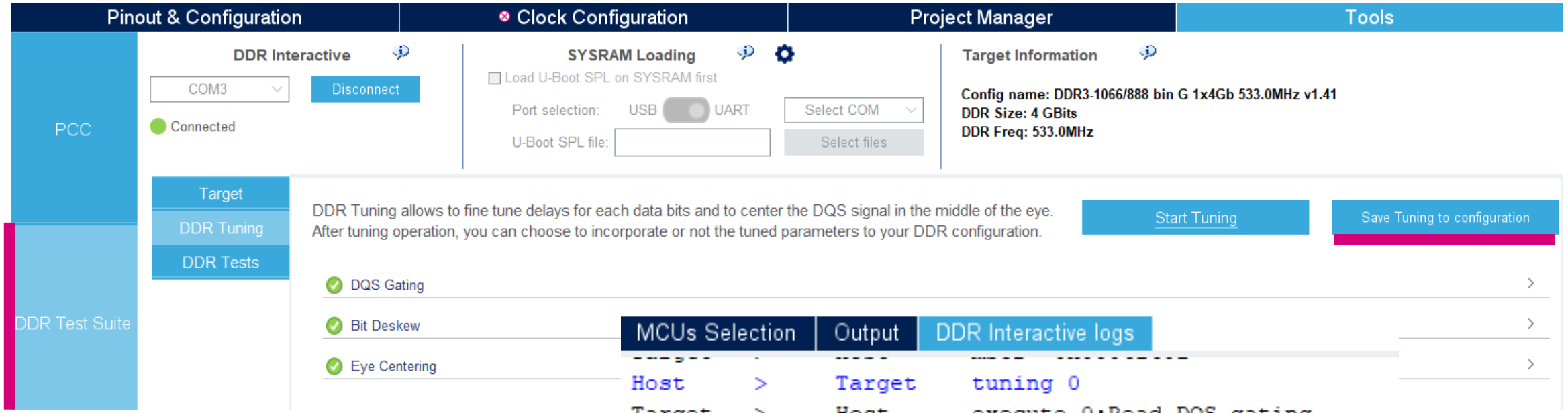
DDR tool suite

- **STM32CubeMX** comes along with an exhaustive tool suite for DDR subsystem
  - **Configuration of DDR** controller and PHY registers is managed automatically based on reduced set of editable parameters
  - **Tuning** of lanes delays is proposed to compensate design imperfection
  - **17 DDR Testing** is offered based on a rich tests list.
    - Basic, perfs and stress tests.
    - User can also develop its own tests.



DDR tuning

- CubeMX interface DDR Tuning tool



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DDR testing

- 17 tests (functional, perf, stress)
- Parameters used for test are recalled, along with Pass/Fail status and results details
- Test history is available in the output panel

Details

Name	DataBusWalking0
Purpose	Verifies each data bus signal can be driven
Test Sequence	Writes patterns with 'moving' 0 on a 32 data bus width. Example: write '11111111111111111111111111111110' at given address, read back given address and

Execution

Parameter(s)	
Address	0xC0000000
Loop	1

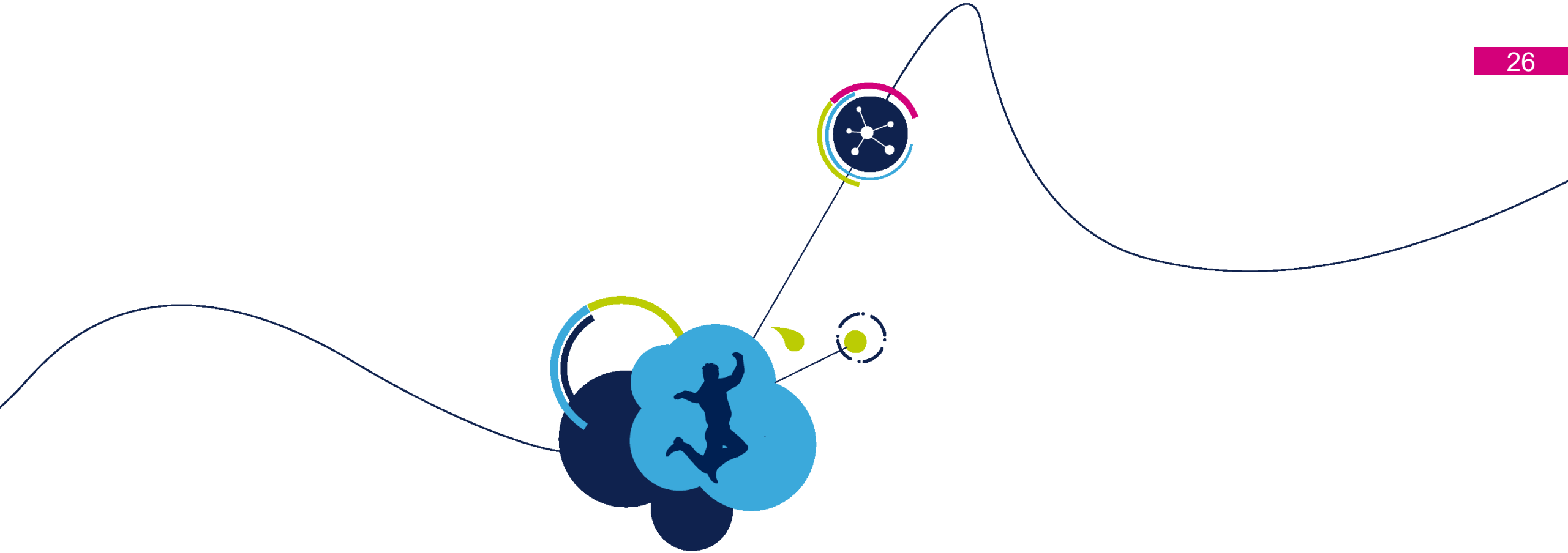
Run test

Verdict

Item(s)	Info
Address	0xC0000000
Loop(s)	1
Result	Pass
Result details	no error for 1 loops

MCUs Selection | Output | DDR Interactive logs

```
Target   >   Host     Byte 1, DQS unit = 3, phase = 3
Target   >   Host     Result: Pass []
Host     >   Target   test 2 1 0xC0000000
Target   >   Host     execute 2:DataBusWalking0
Target   >   Host     running 1 loops at 0xc0000000
Target   >   Host     Result: Pass [no error for 1 loops]
```



Documents

HW related Application Notes

(only major ones)

- AN5031 Getting started with STM32MP1 Series hardware development

  https://www.st.com/resource/en/application_note/dm00389996.pdf

  - Power supplies, external clocks and resets, boot configuration, IO speed settings, PCB, ...
  - Examples of reference schematics (Debug, STPMIC1, DDR3/DDR3L/LPDDR2/LPDDR3, SD-Card, eMMC, Raw-NAND, Serial-NOR/NAND, USB, Ethernet, DSI, etc...)
- AN5168 DDR configuration on STM32MP1 Series MPUs

  https://www.st.com/resource/en/application_note/dm00505673.pdf

  - DDR subsystem initialization and configuration
  - Configuration sequence and parameters for DDR3/DDR3L/LPDDR2/LPDDR3
  - DDR Tuning and Testing
- AN5122 STM32MP1 Series DDR memory routing guidelines

  https://www.st.com/resource/en/application_note/dm00462392.pdf

  - Memory architecture options
  - DDR3/DDR3L schematic implementation for DDR3/DDR3L/LPDDR2/LPDDR3
  - PCB design considerations, Memory layout rules
  - Provided with “STM32MP1 Series DDR memory routing guidelines examples” Zip file containing multiple Altium® schematics and PCB projects

HW related data

- STM32MP1 CAD Symbol and Footprint files
  - To quickly start projects

  https://www.st.com/resource/en/svd/stm32mp1_svd.zip 

- STM32MP1 IBIS file (Input/output Buffer Information Specification)
  - For **board signal integrity** simulations

  https://www.st.com/resource/en/bsdl_model/stm32mp1_ibis.zip 

- STM32MP1 BSDL file (Boundary Scan Description Language)
  - For **board manufacturing tests**

  https://www.st.com/resource/en/bsdl_model/stm32mp1_bsdl.zip 

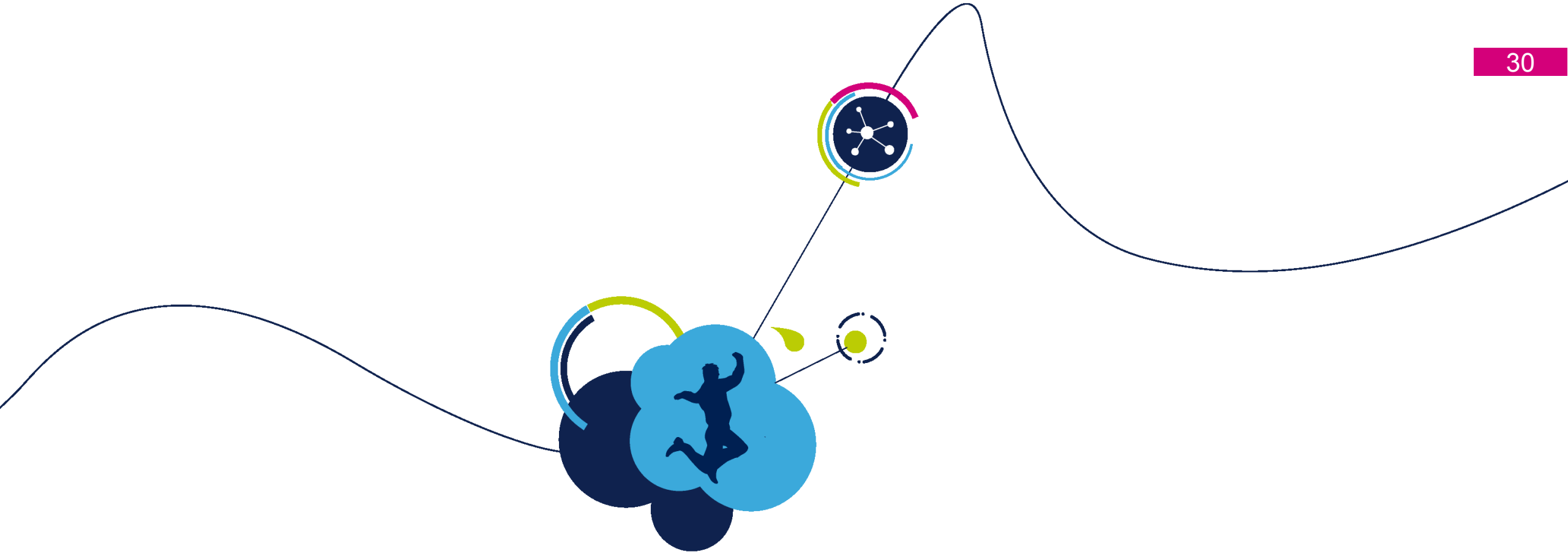
- STM32MP1 System View Description (SVD)
  - Ease debugging using abstraction of HW registers address

  https://www.st.com/resource/en/cad_symbol_library/stm32mp1_cad.zip 

- Main page
  https://wiki.st.com/stm32mpu 
- Reference documents links
  - Application Notes
  - DataSheets / Reference Manuals / ErrataSheets
  - Boards schematics and users manuals

  https://wiki.st.com/stm32mpu/wiki/STM32MP15_ecosystem_release_note#Reference_documents 
- ROM code HW related information (Boot pins, Flash connections, etc...)

  https://wiki.st.com/stm32mpu/wiki/STM32MP15_ROM_code_overview 



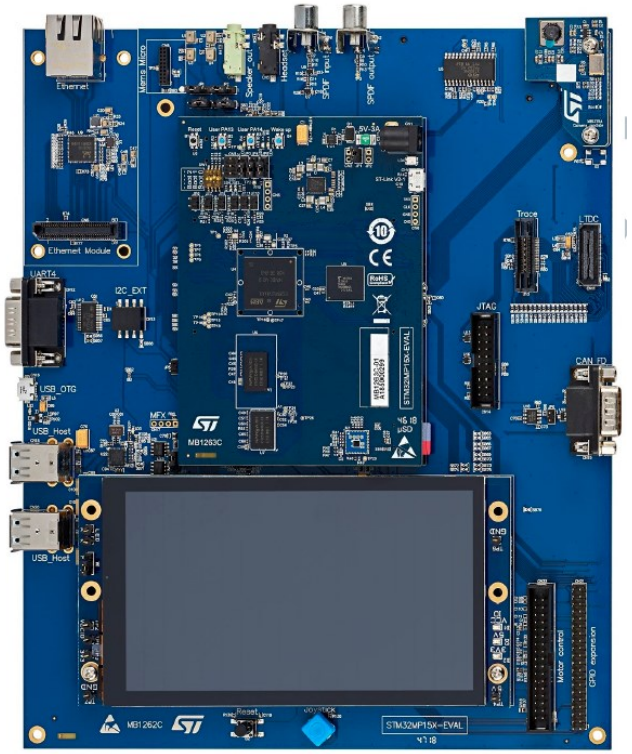
Reference Boards

Reference Boards 1/2

- Evaluation board EV1
  - with STM32MP157 LFBGA448 (18x18) + STPMIC1A + 2xDDR3L 16- + eMMC + UHS-I SD-Card + ST-LINK/V2-1 + 5.5” DSI touchscreen + 5Mpixels Camera + Ethernet Gigabit

https://www.st.com/en/evaluation-tools/stm32mp157c-ev1.html

- Board design Altium project files
- Manufacturing files
- Board Schematic
- Bill of materials



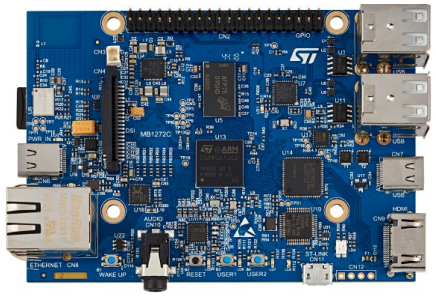
Order code	Board reference	Target STM32	Differentiating feature
STM32MP157A-EV1	• MB1262: mother board • MB1263: MPU subsystem daughterboard • MB1230: DSI display board • MB1379: camera board	STM32MP157AAA3	Basic security.
STM32MP157C-EV1		STM32MP157CAA3	Secure Boot and cryptography.

Reference Boards 2/2

- Discovery board DK1/DK2
  - with STM32MP157 TFBGA361 (12x12) + STPMIC1A + DDR3L 16-bits + SD-Card + HDMI Bridge + Gigabit Ethernet + USB Type-C + ST-LINK/V2-1 + + 4” DSI touchscreen + Ethernet Gigabit

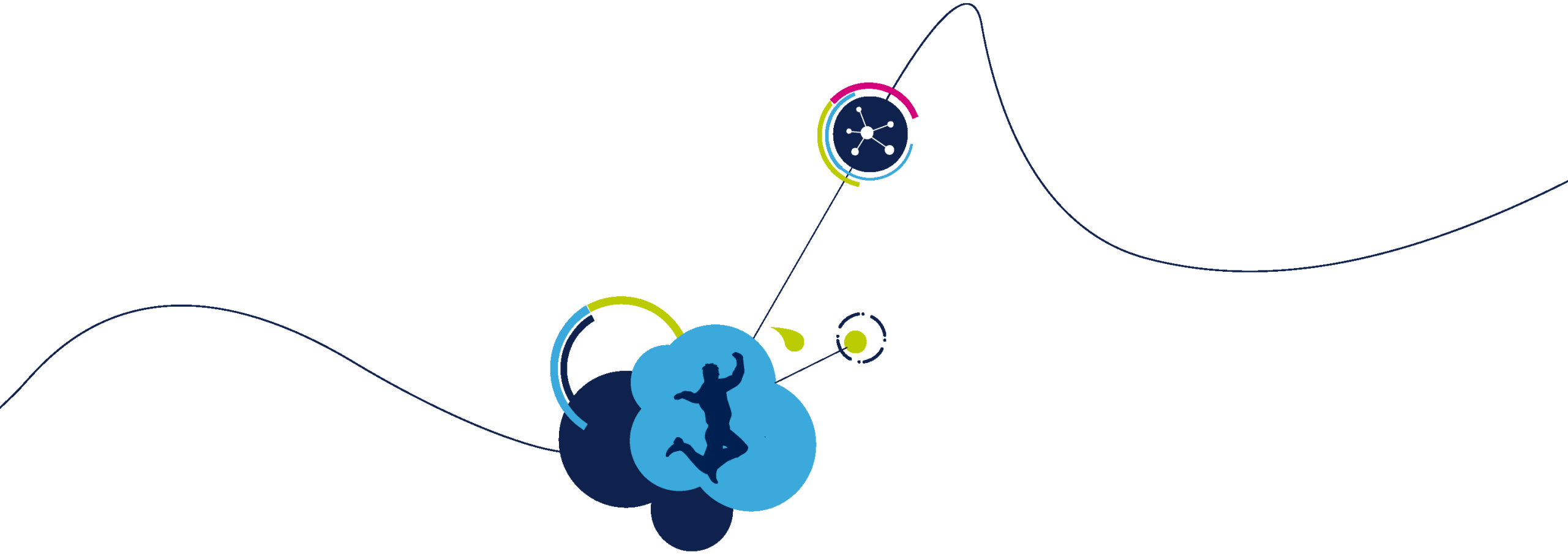
https://www.st.com/en/evaluation-tools/stm32mp157c-dk2.html

- Board design Altium project files
- Manufacturing files
- Board Schematic
- Bill of materials



Order code	Board reference	Target STM32	Differentiating feature
STM32MP157A-DK1	• MB1272	STM32MP157AAC3	• Basic security
STM32MP157C-DK2	• MB1272 • MB1407(1)	STM32MP157CAC3	• Secure Boot and cryptography • LCD • Wi-Fi® • Bluetooth® Low Energy

1. *LCD extension board.*



Are challenges still seen as complex ?

Main challenges for HW (solutions)

Platform HW definition should be simple

- STM32CubeMx, Reference board, Application Notes, Wiki

PCB routing should allow low complexity PCB stackup and technology

- Smart Package definition, DDR Tools, Reference design

Platform supplies definition should be as simple as possible

- STPMIC1, Reference design, Application Notes

Signal integrity should be easy to manage / test

- DDR Tools, IBIS models, BSDL files