STM32MP1

STM32MP1 and STPMIC Overview

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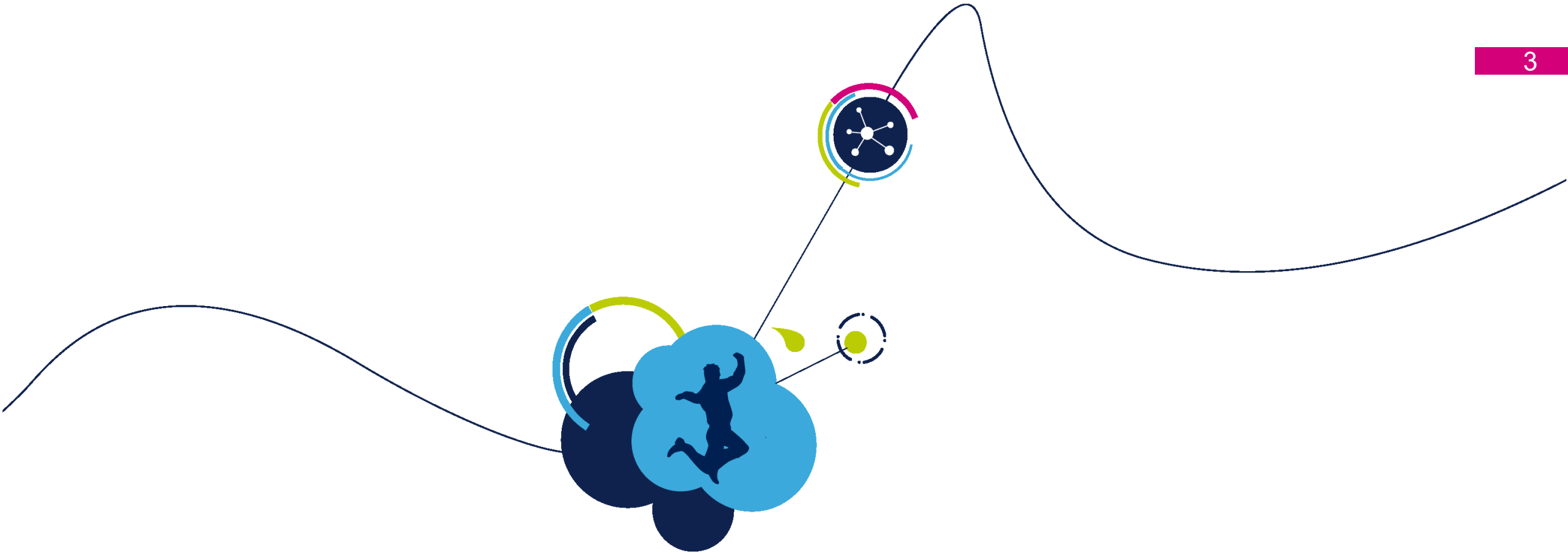
Agenda

Presentation

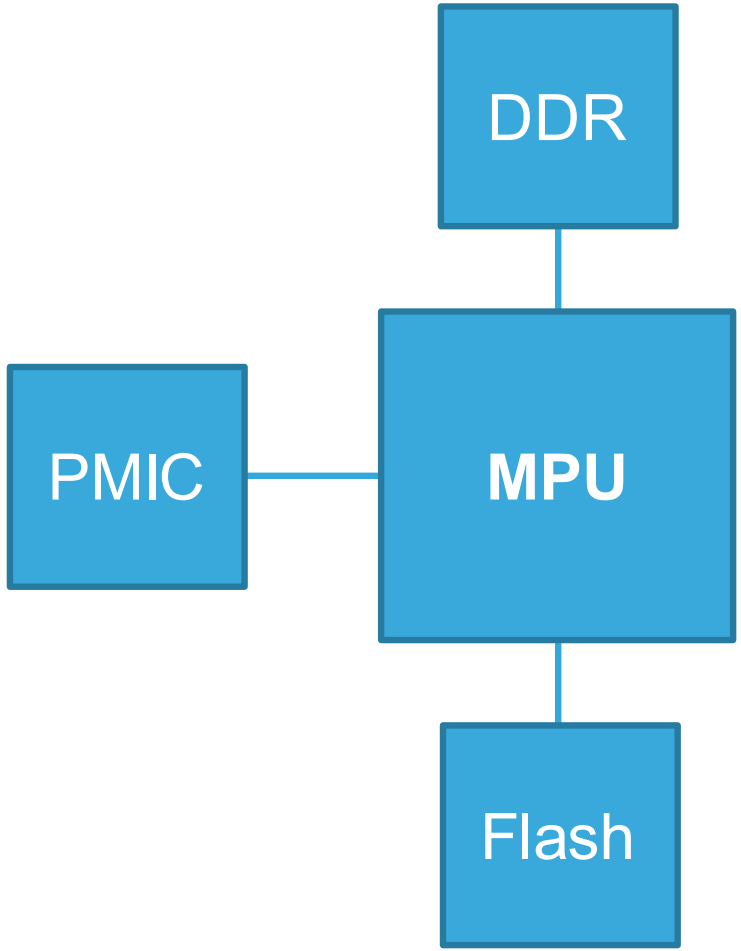
40 min

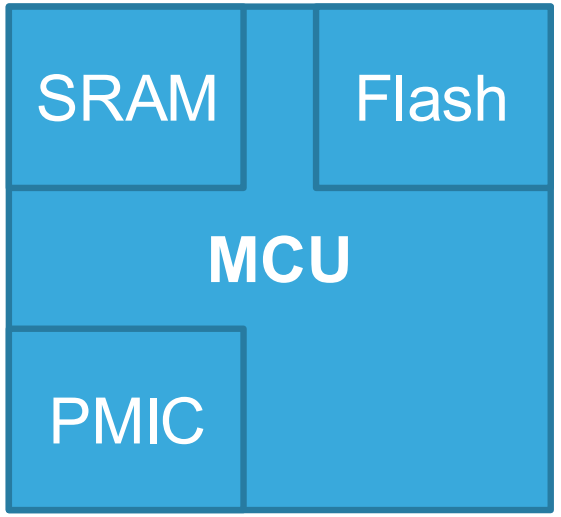
- STM32MP1 Hardware Architecture
- Power System Architecture



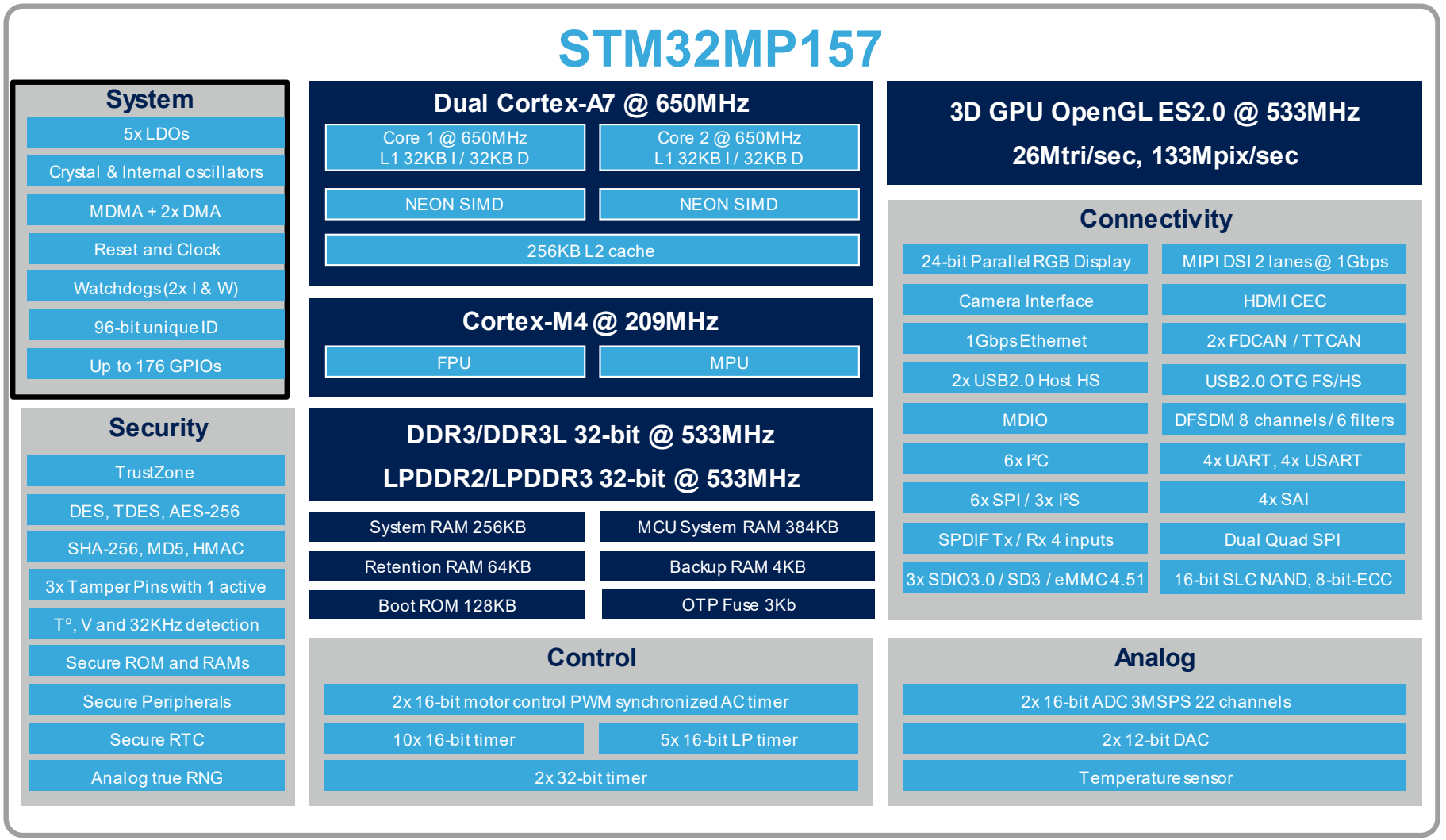
STM32MP1 hardware architecture

MPUs vs. MCUs System Diff.





STM32MP1 Block Diagram



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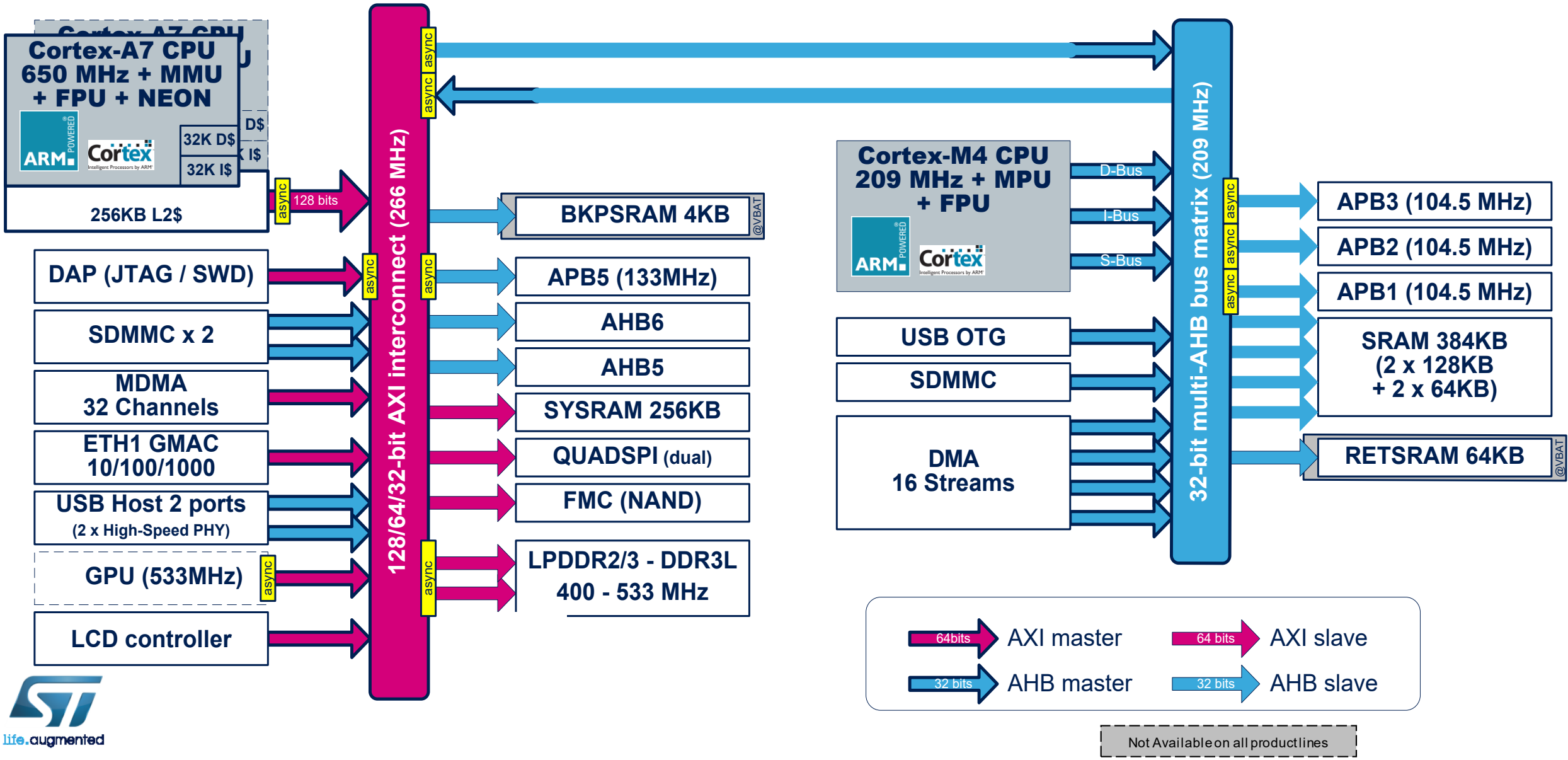
Bus architecture overview



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System & Security

- System control
  - RCC
    - Reset and Clock Controller
  - PWR
    - Power modes Controller
  - EXTI
    - External Interrupt management
  - MDMA (MasterDMA)
    - DMA1/2 sequencer
- OTP Fuse
- Security
  - ETZPC
    - Controls A7 access to some peripherals, to SYSRAM, BKPSRAM
  - TZC
    - Security firewall for DDR data accesses
  - BSEC
    - Global security settings and OTP fuses control
    - Contains Device Electronic Signature registers
  - TAMP
    - Tamper pins and backup registers management
  - BKPSRAM
    - securable memory, Tamper protected
  - CRYP, HASH, TRNG and CRC
    - Secure and non-secure instances

Memories Summary

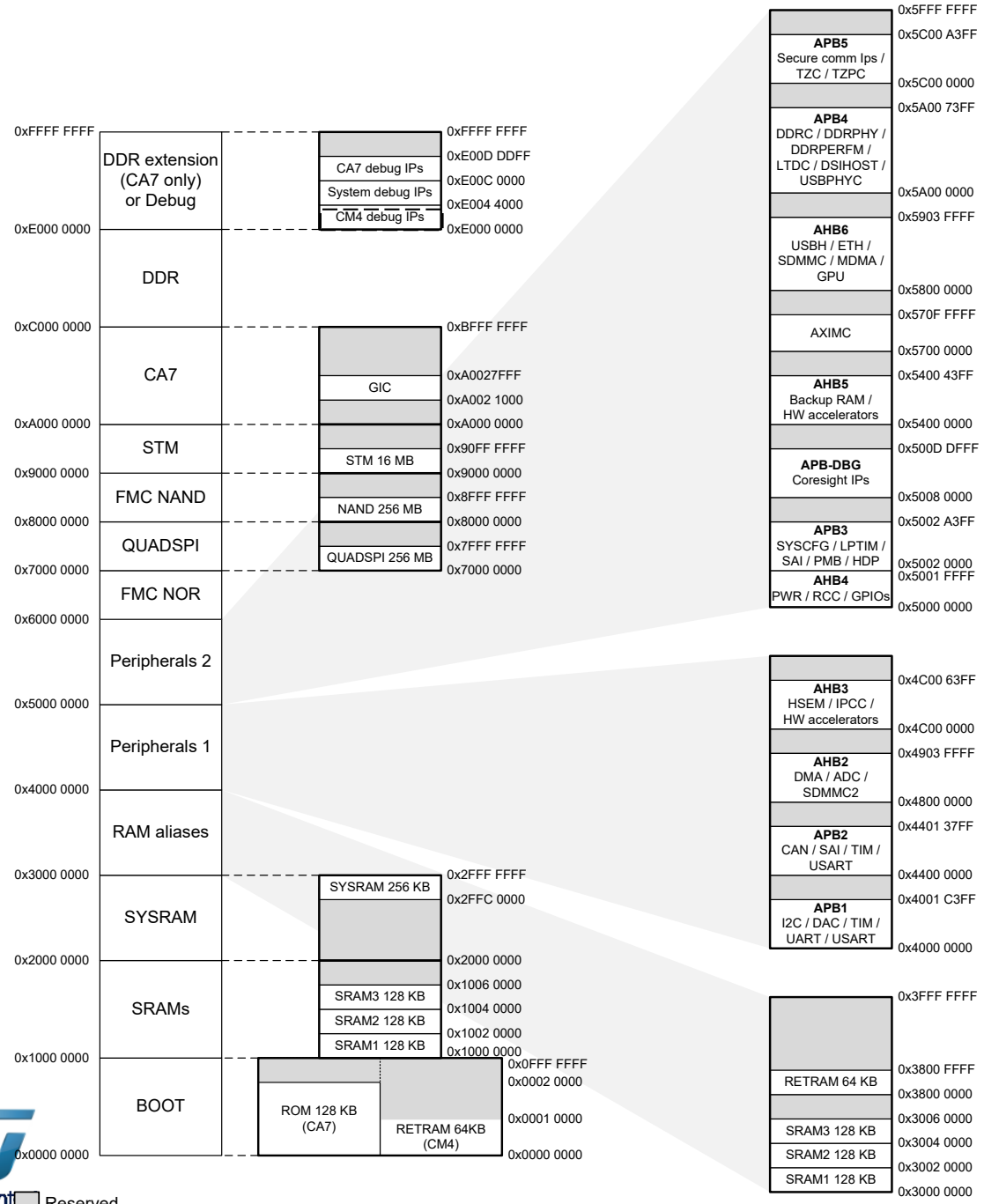
	Memory	Type	Size	TrustZone Access Control	Cortex-A7 access	Cortex-M4 access
Embedded memories	BOOTROM	ROM	128 KB	●	●	No access
	SRAM	SRAM	384 KB	●	●	●
	SYSRAM	SRAM	256 KB	●	●	●
	RETRAM	SRAM (On VBAT)	64 KB	●	●	●
	BKPSRAM	SRAM (On VBAT)	4 KB	●	●	●
External memories	DDR SDRAM	DDR3, DDR3L, LPDDR2, LPDDR3	Up to 1 GB	●	●	Not recommended
	SDMMC	SD-Card, e•MMC			●	● *(SDMMC3 only)*
	QUADSPI	SPI Flash	Up to 512 MB (1) Up to 4 GB (2)		●	Code execution **not recommended**
	FMC NOR	NOR Flash, SRAM	Up to 256 MB		●	●
	FMC NAND	NAND Flash	Up to 256 MB		●	●

Interfaces to external DRAM

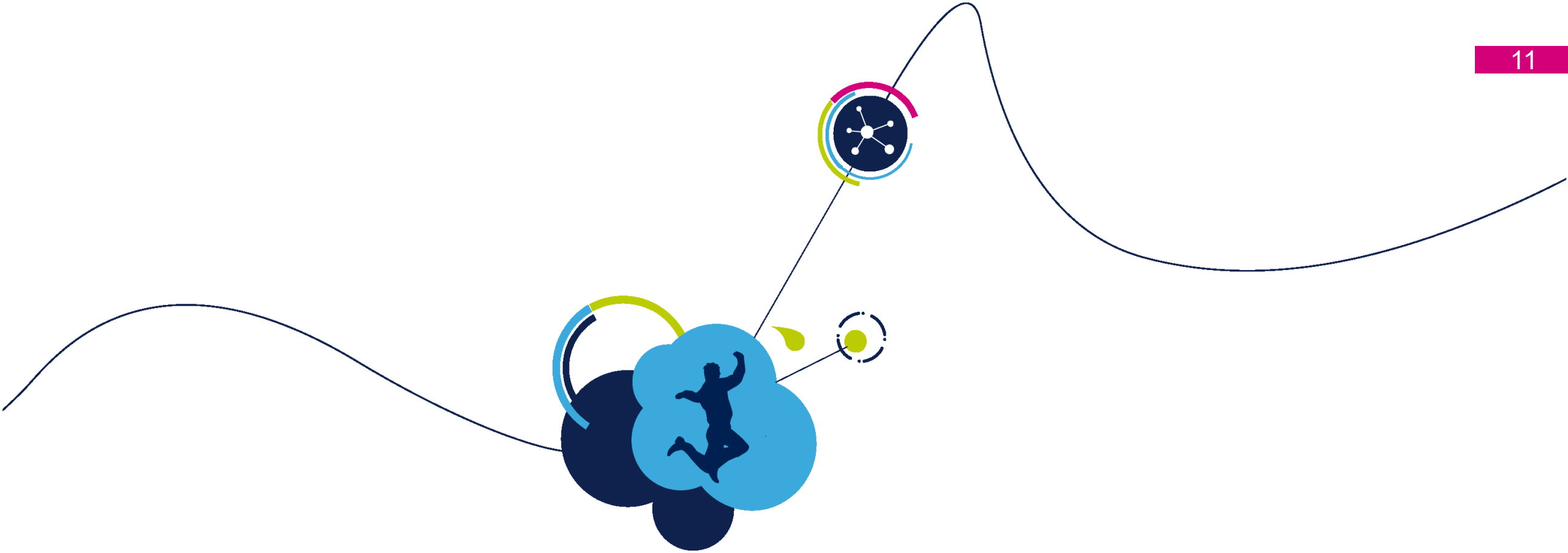
DRAM Device	Data width	Max Freq.	# of CS	# of ICs	# of wires	Comments
DDR3 / DDR3L	16-bits	533 MHz	1	1	50	DDR3L recommended for new designs
	32-bits	533 MHz	1	2	72	
LPDDR2 / LPDDR3	16-bits	533 MHz	1	1	36	16-bits less popular than 32-bits
	32-bits	533 MHz	1	1	58	

- DDR interface uses dedicated pins which cannot be reused for other purposes
- 32-bit interface only available on LFBGA448 and TFBGA361 packages

Memory Map overview

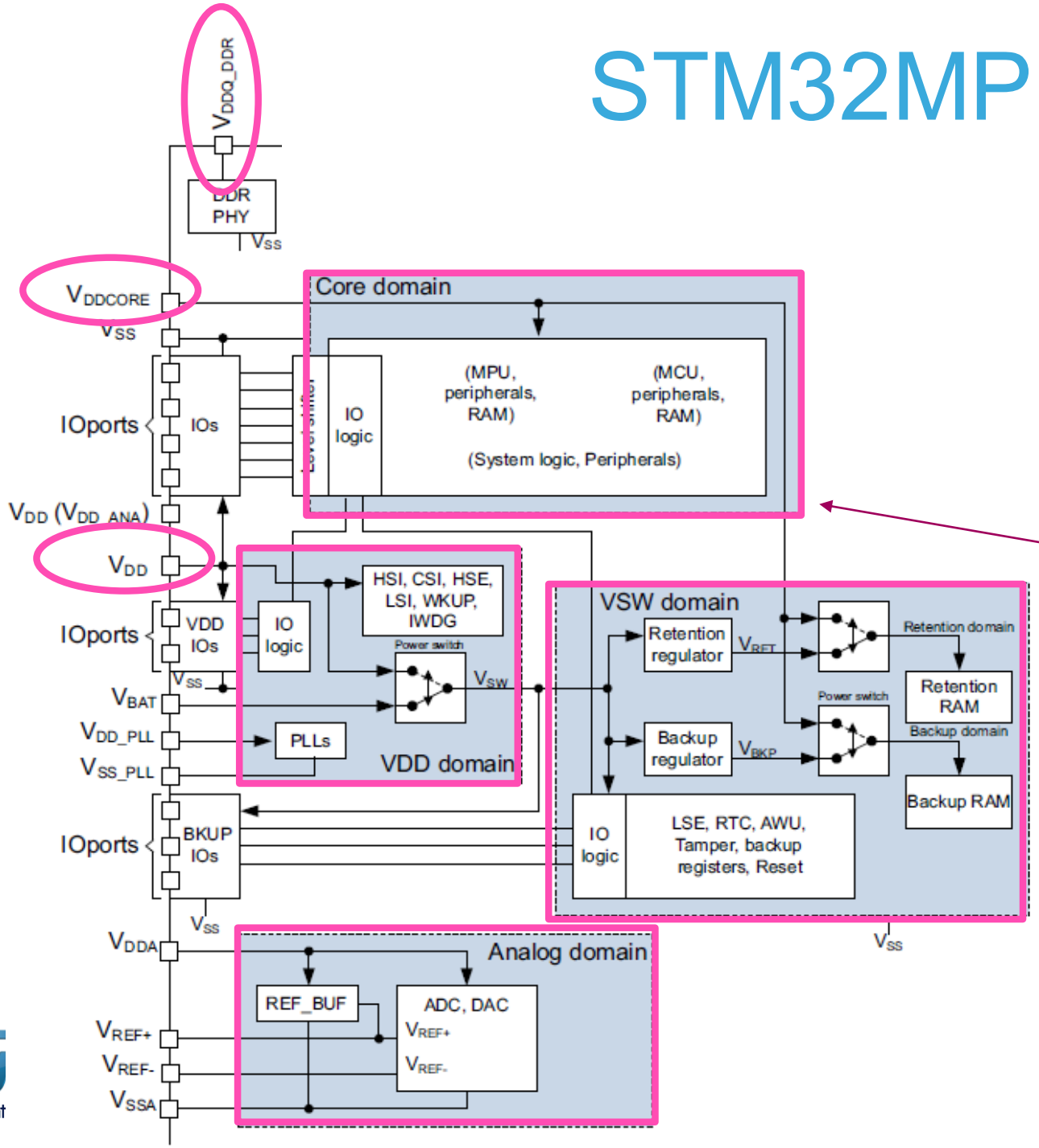


- Uniform memory map
  - All peripherals visible on same address of every masters
  - No Remap



Power architecture

STM32MP1 Power supplies



Mandatory supplies :

VDDQ_DDR 1.2V / 1.35V / 1.5V
VDDCORE 1.2 V
VDD 1.7V – 3.6V

4 power domains :

- Core domain
- VDD domain
- VSW domain (V**SW**itch) for Standby lp mode
- Analog domain

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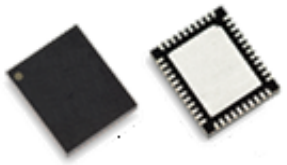
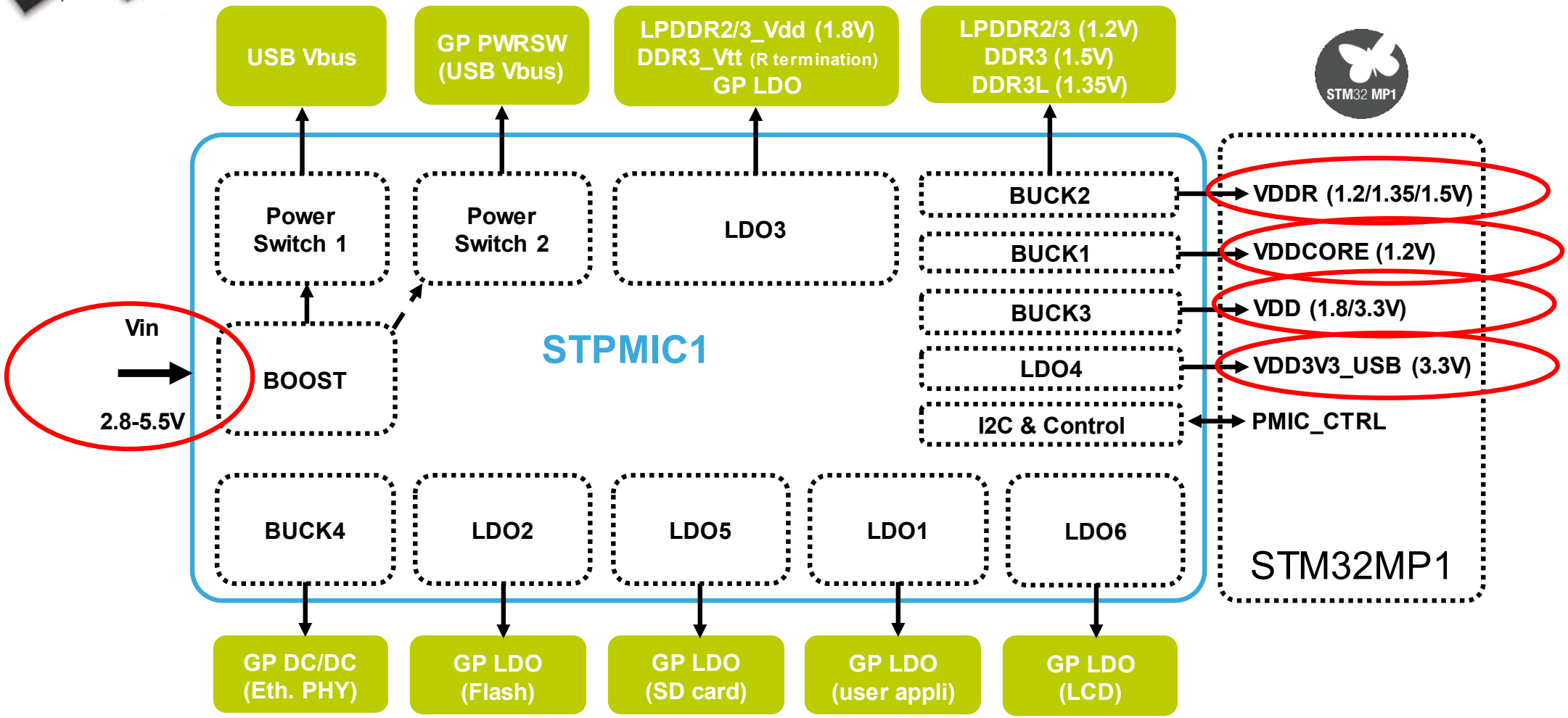
External Power Supply

- Two solutions:
  - STPMIC1 power distribution
    - Better integration on the PCB with a reduced footprint
    - Advanced features such as voltages scaling, short-circuit detection,…
    - Offers power supply for other modules (Wifi, Ethernet Phy, DSI phy)
    - Integrated power switches (USB)
  - Discrete power distribution
    - Individual set of regulators on the PCB
    - For minimalist solution (DRAM, FLASH, MPU) for SOM makers for example
    - Fixed voltage



Power supply with STPMIC1



➔ STPMIC1 save external Bucks and LDOs on PCB for typical applications

➔ 5V Vin allows power using USB

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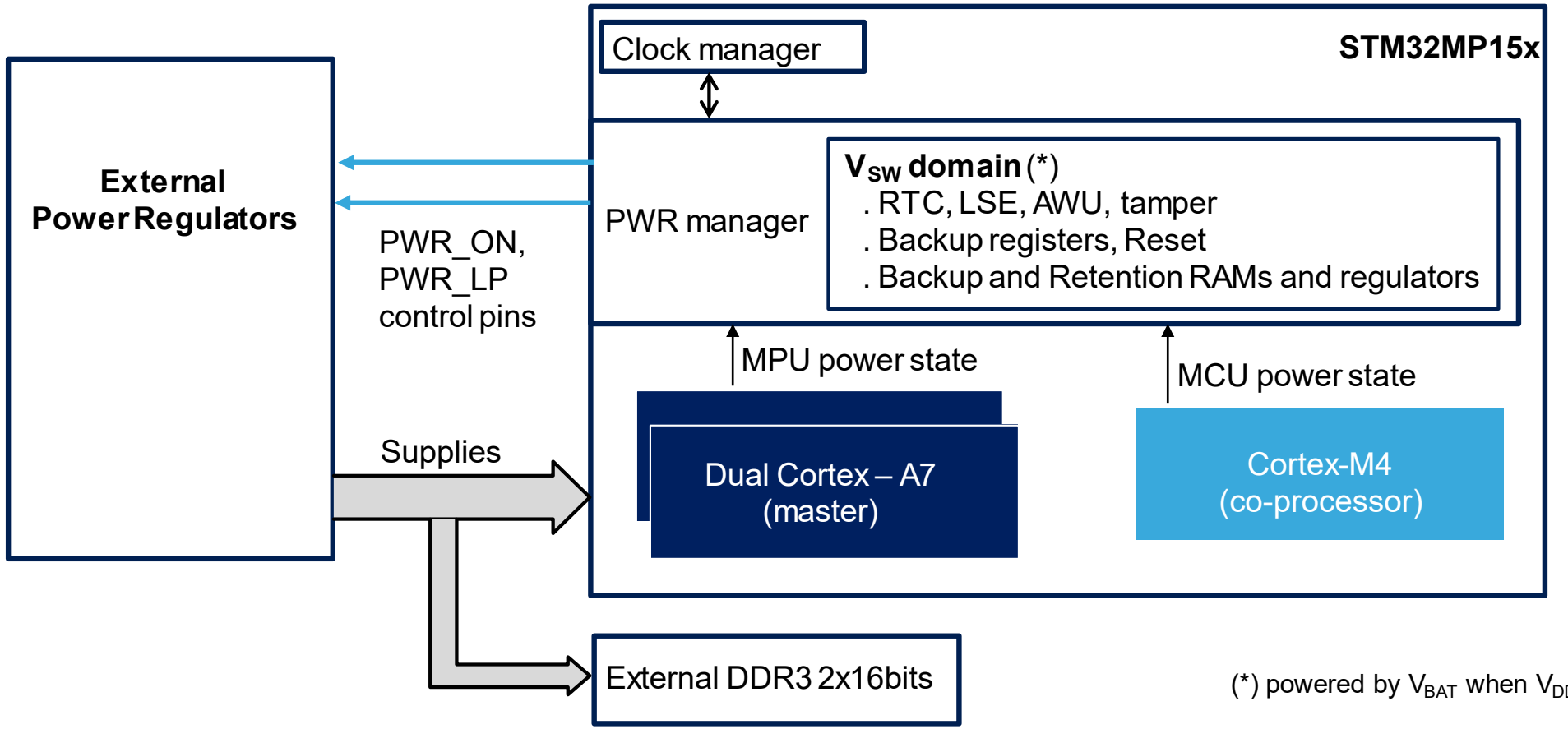
Power Management Architecture

- System power modes are set by PWR manager based on MPU and MCU power modes



(*) powered by V_{BAT} when V_{DD} is not present)

STM32MP1 system power modes

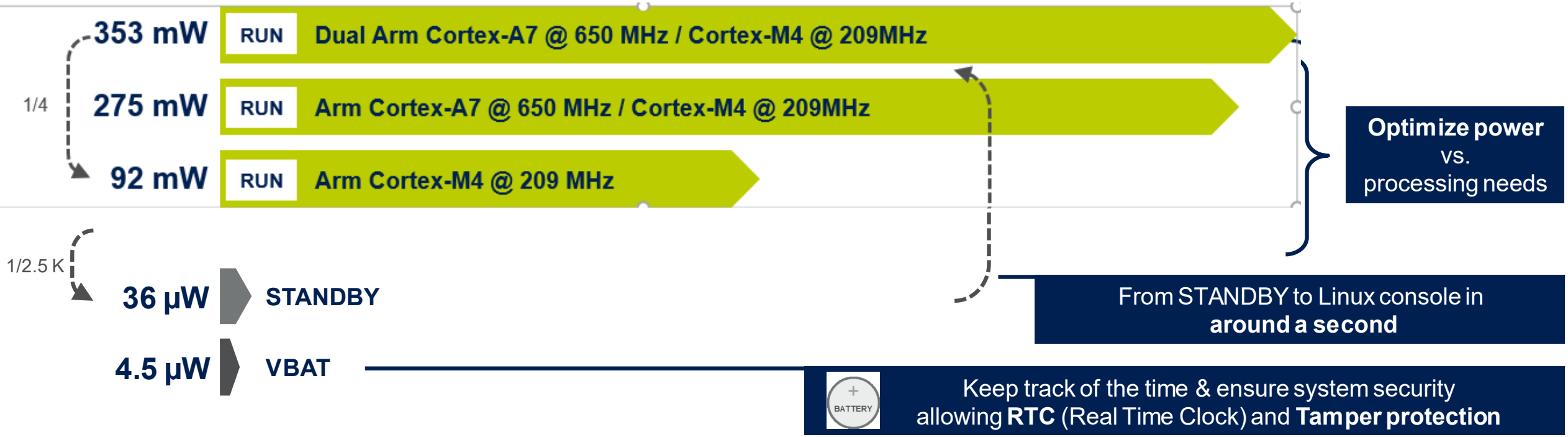
System Power Mode	V_{DDCORE}	Clocks	Wakeup sources (not all sources are available in the Linux environment)
Run	Nominal (typ. 1.2V)	ON	All
Stop	Nominal (typ. 1.2V)	MCU and MPU sub-systems clock OFF	DBG, PVD, AVD, USBH, OTG, CEC, ETH, MDIOS, USARTx, I2Cx, SPIx, TEMP, LPTIMx, GPIOs (+ VBAT mode sources)
LP-Stop	Nominal (typ. 1.2V)		
LPLV-Stop	Reduced (typ. 0.9V)		PVD, AVD, TEMP, GPIOs (+ VBAT mode sources)
Standby	0 V		6 GPIO wakeup pins (+ VBAT mode sources)
VBAT	RTC and backup domain supply provided by optional V_{BAT} supply when V_{DD} is not present		BOR, VBATH/VBATL, TEMPH/TEMPL, LSE CSS, RTC/Auto wakeup, Tamper pins, IWDGx

LPLV-Stop requires external power regulator with voltage scaling to lower down VDDCORE supply (to reduce the STM32MP1 consumption)

The STPMIC1 power regulator offers this feature

Flexible Architecture for Power Efficiency

Power figures (VDD+ VDDCORE)



Typ @ VDDCORE = 1.2V, V_{DD} = 3.3 V @ 25 °C, Peripherals OFF

See AN5284 : *STM32MP1 Series system power consumption*

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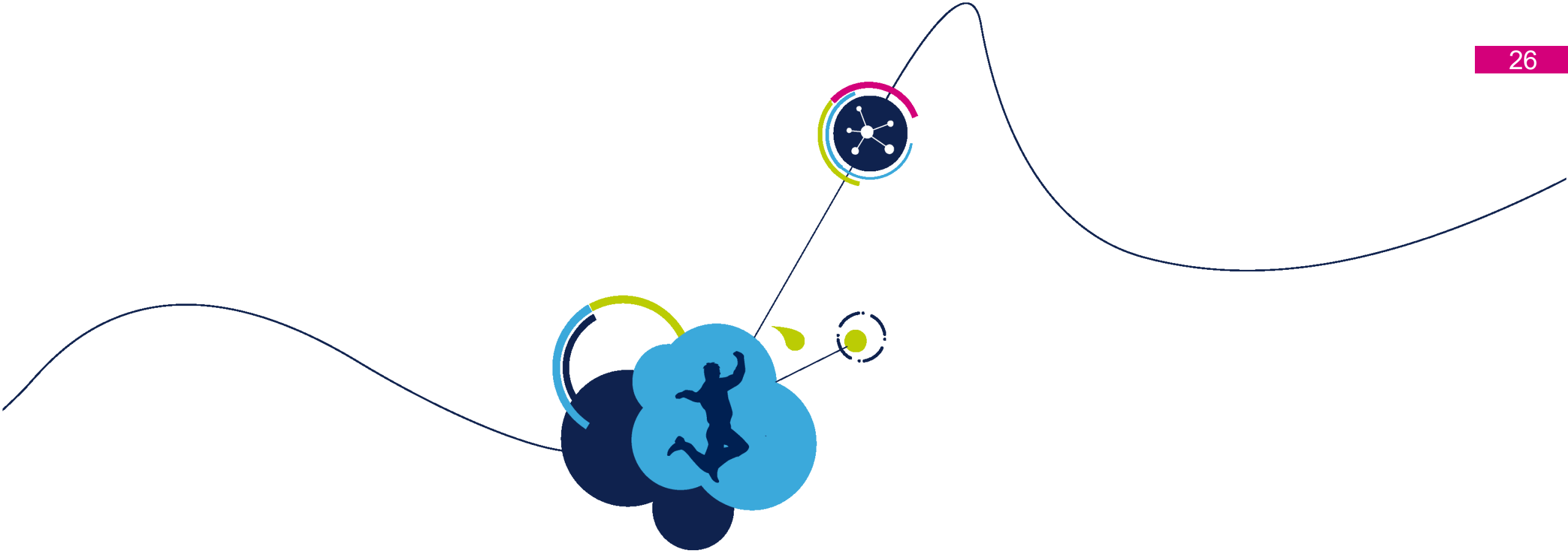
Power documentation

- AN5031 - Getting started with STM32MP15 Series hardware development
- AN5109 - STM32MP15 Series using low-power mode
- AN5256 - STM32MP15x Lines discrete power supply hardware integration
- RM0436 - reference manual - STM32MP157xxx advanced Arm®-based 32-bit MPUs

Power Consumption

Mode	Conditions V_{DDCORE}=1.20V, V_{DD}=3.3V, Tj = 25ºC, HSE=24MHz	V_{DDCORE}+V_{DD} Power(Typ.)
Run (A7+M4 Coremark)	All digital powered, All peripherals clocked, Cortex-A7@648MHz, AXI @264MHz, MCU Subsystem @209MHz. No GPU activity. DDR in Self-refresh.	409mW (1x A7 +M4) 487mW (2x A7 +M4)
Run (A7+M4 Coremark)	All digital powered, All peripherals **stopped**, Cortex-A7@648MHz, AXI @264MHz, MCU Subsystem @209MHz. No GPU activity. DDR in Self-refresh.	275mW (1x A7 +M4) 353mW (2x A7 +M4)
Run (A7 Coremark)	All digital powered, All peripherals stopped , Cortex-A7@648MHz, AXI @264MHz, MCU Subsystem @**64MHz**, **Cortex-M4 in CStop**. No GPU activity. DDR in Self-refresh.	229mW (1x A7) 307mW (2x A7)
Run (M4 Coremark)	All digital powered, All peripherals stopped, **Cortex-A7 in CStop**, **MCU Subsystem @209MHz**, **Cortex-M4 @209MHz**. No GPU activity. DDR in Self-refresh.	92mW (M4)
Stop	All digital powered. **All Cores stopped**. **HSE and PLLs are OFF**. All peripherals stopped (except those of VBAT domain). DDR in Self-refresh.	26mW
LpLv-Stop	All digital powered. All Cores stopped. HSE and PLLs are OFF. All peripherals stopped (except those of VBAT domain). DDR in Self-refresh. **V_{DDCORE} = 0.9V**.	9.5mW
Standby w/ Retention RAM	**V_{DDCORE} OFF**, 32KHz and RTC ON. Tamper detection active, 4KB Backup RAM, 64KB Retention RAM. Wake-up on RTC, Tamper event, external wake-up pins**. DDR in Self-refresh** (optional).	316µW
Standby	V_{DDCORE} OFF, 32KHz and RTC ON. Tamper detection active, 4KB Backup RAM, **no 64KB Retention RAM**. Wake-up on RTC, Tamper event, external wake-up pins. DDR in Self-refresh (optional).	36µW
Off/Vbat	V_{DDCORE} **and V_{DD} OFF**, 32KHz and RTC ON. Tamper detection active. VBAT=3V (with 4KB Backup RAM enabled)	4.5µW on VBAT (~26uW)

Above data are based on measurements done for datasheet Rev.1 (Silicon Rev.B)



Thanks