STM32MP1

STM32MP1 and STPMIC Overview





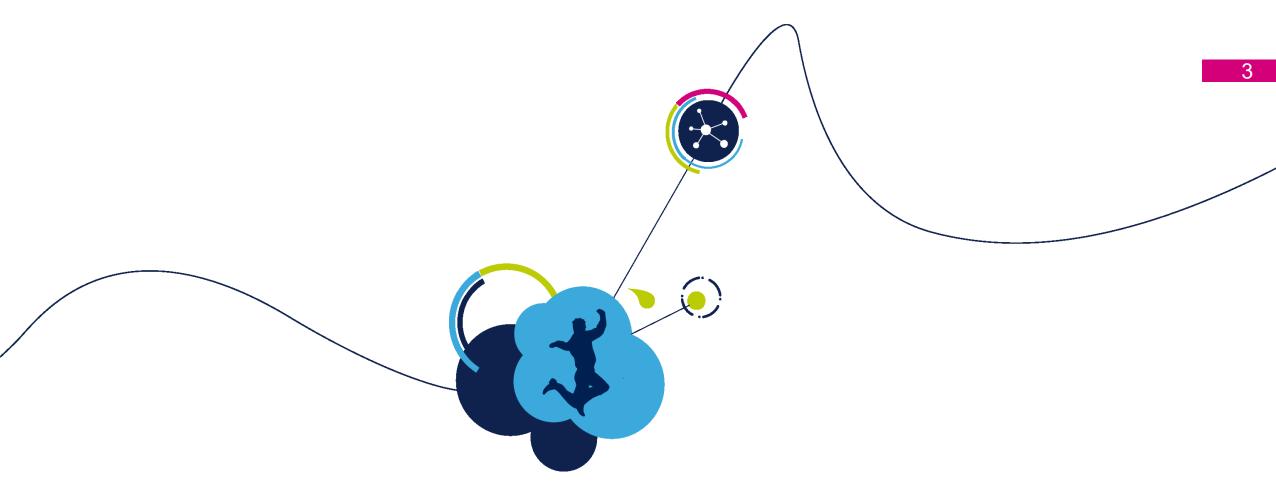
Presentation

Agenda 2

40 min

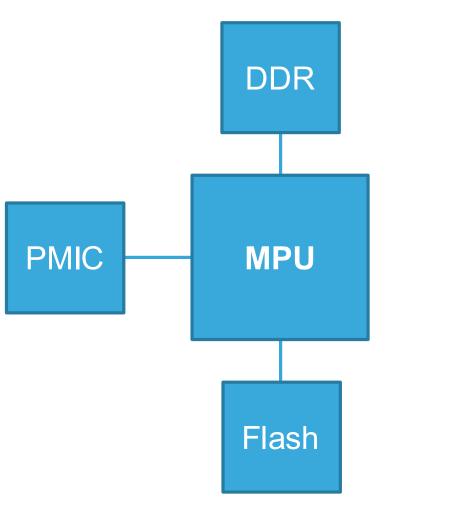
- STM32MP1 Hardware Architecture
- Power System Architecture

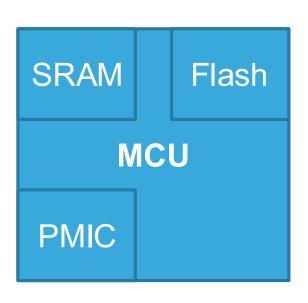




STM32MP1 hardware architecture

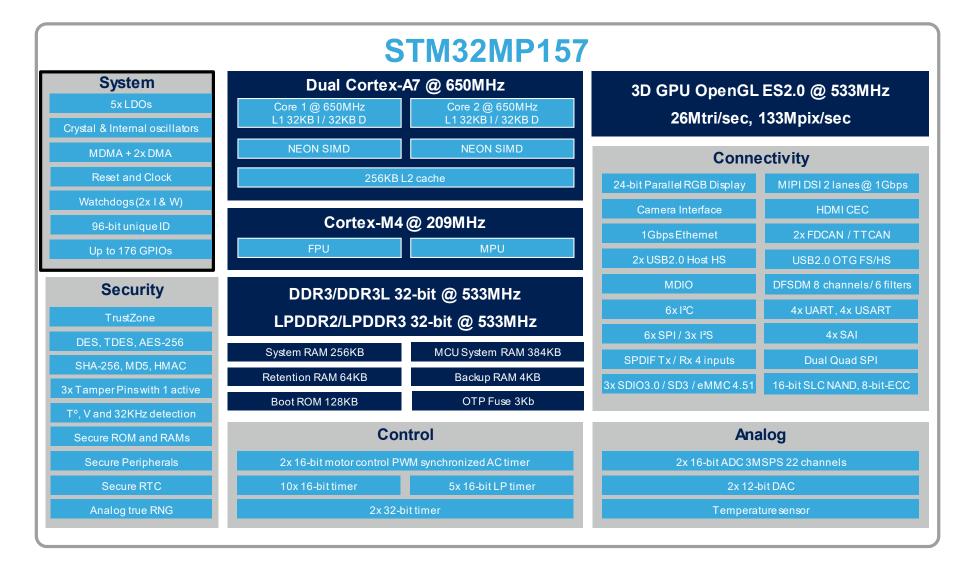
MPUs vs. MCUs System Diff.





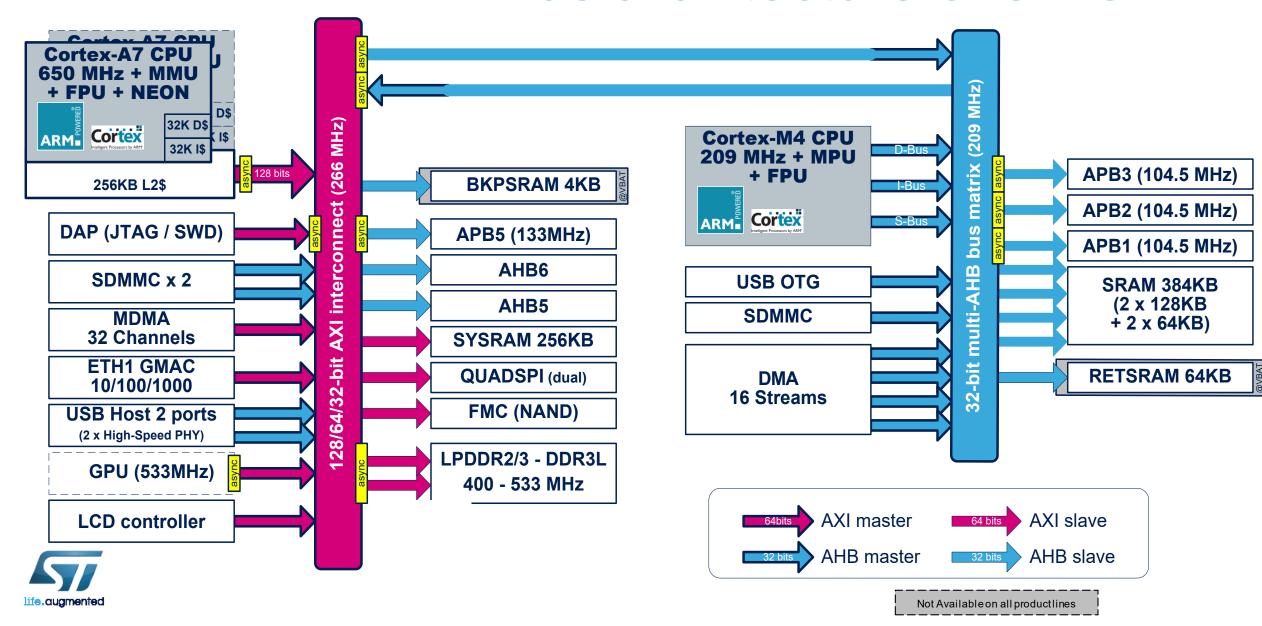


STM32MP1 Block Diagram 5





Bus architecture overview 6



System control

- RCC
 - Reset and Clock Controller
- PWR
 - Power modes Controller
- EXTI
 - External Interrupt management
- MDMA (MasterDMA)
 - DMA1/2 sequencer

OTP Fuse



System & Security _____

- Security
 - ETZPC
 - Controls A7 access to some peripherals, to SYSRAM, BKPSRAM
 - TZC
 - Security firewall for DDR data accesses
 - BSEC
 - Global security settings and OTP fuses control
 - Contains Device Electronic Signature registers
 - **TAMP**
 - Tamper pins and backup registers management
 - **BKPSRAM**
 - securable memory, Tamper protected
 - CRYP, HASH, TRNG and CRC
 - Secure and non-secure instances

Memories Summary 8

	Memory	Туре	Size	TrustZone Access Control	Cortex-A7 access	Cortex-M4 access
es	BOOTROM	ROM	128 KB	•	•	No access
Embedded memories	SRAM	SRAM	384 KB	•	•	•
	SYSRAM	SRAM	256 KB	•	•	•
	RETRAM	SRAM (On VBAT)	64 KB	•	•	•
ᇤ	BKPSRAM	SRAM (On VBAT)	4 KB	•	•	•
External memories	DDR SDRAM	DDR3, DDR3L, LPDDR2, LPDDR3	Up to 1 GB	•	• (Not recommended
	SDMMC	SD-Card, e•MMC			•	(SDMMC3 only)
	QUADSPI	SPI Flash	Up to 512 MB (1) Up to 4 GB (2)		• (Code execution not recommended
	FMC NOR	NOR Flash, SRAM	Up to 256 MB		•	•
	FMC NAND	NAND Flash	Up to 256 MB		•	•



Interfaces to external DRAM

DRAM Device	Data width	Max Freq.	# of CS		# of wires	Comments
DDR3/	16-bits	533 MHz	1	1	50	DDD21 recommended for new decigns
DDR3L	32-bits	533 MHz	1	2	72	DDR3L recommended for new designs
LPDDR2/	16-bits	533 MHz	1	1	36	16-bits less popular than 32-bits
LPDDR3	32-bits	533 MHz	1	1	58	

- DDR interface uses dedicated pins which cannot be reused for other purposes
- 32-bit interface only available on LFBGA448 and TFBGA361 packages



0xFFFF FFFF					0xFFFF F	FFF
	DDR extension				0xE00D	
	(CA7 only)			bug IPs	0xE00C 0	
	or Debug			lebug IPs	0xE004 4	
0xE000 0000			CM4 de	bug IPs	0xE000 0	
	DDR					
0xC000 0000					0xBFFF F	FFF
	CA7			IC	0xA0027F	FF
			G	ic .	0xA002 1	000
0xA000 0000					0xA000 0	000
	STM		etw.	16 MB	0x90FF F	FFF
0x9000 0000			STW	TO IVID	0x9000 0	000
	FMC NAND		NAND	256 MB	0x8FFF F	FFF
0x8000 0000			IVAIND	230 IVID	0x8000 00	000
	QUADSPI		OLIADSE	PI 256 MB	0x7FFF F	FFF
0x7000 0000			QO/IDOI	1 200 WIB	0x7000 0	000
	FMC NOR					
0x6000 0000						
	Danimbanala 0					
	Peripherals 2					
0x5000 0000						
	Peripherals 1					
0x4000 0000						
	RAM aliases					
	RAIVI aliases					
0x3000 0000					0x2FFF F	FFF
			SYSRAN	1 256 KB	0x2FFC 0	000
	SYSRAM					
0x2000 0000					0x2000 0	
			SRAM3	128 KB	0x1006 0	
	SRAMs		SRAM2	128 KB	0x1004 0	
			SRAM1	128 KB	0x1002 00 0x1000 00	
0x1000 0000					- CX 1000 0	0x0FFF FFFF
	ВООТ					0x0002 0000
	ВООТ		128 KB A7)	DETD.	MEAKE	0x0001 0000
Z.,0000 0000		(6)	· · /		M 64KB VI4)	00000 0000
0x0000 0000						0x0000 0000

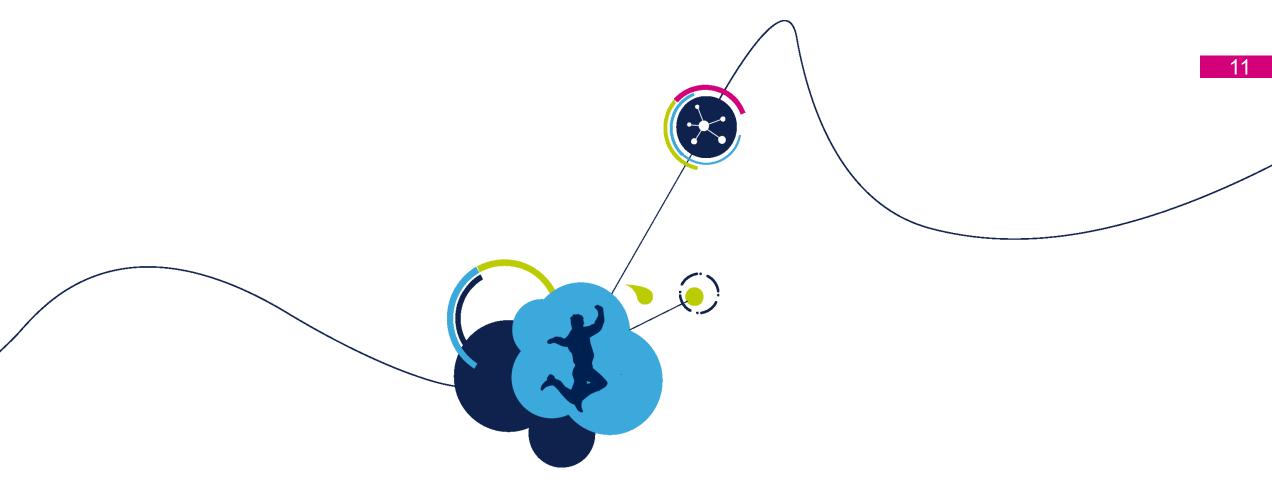
	0x5FFF FFFF
	0x5C00 A3FF
APB5 Secure comm lps / TZC / TZPC	0x5C00 0000
	0x5A00 73FF
APB4 DDRC / DDRPHY / DDRPERFM / LTDC / DSIHOST / USBPHYC	0x5A00 73FF
AHB6 USBH / ETH / SDMMC / MDMA / GPU	0x5903 FFFF
5. 5	0x5800 0000
	0x570F FFFF
AXIMC	0x5700 0000
	0x5400 43FF
AHB5 Backup RAM / HW accelerators	0x5400 0000 0x500D DEFE
APB-DBG Coresight IPs	
	0x5008 0000
APB3 SYSCFG / LPTIM /	0x5002 A3FF
SAI / PMB / HDP	0x5002 0000 0x5001 FFFF
PWR / RCC / GPIOs	0x5000 0000

	0x4C00 63FF
AHB3	0X4C00 63F1
HSEM / IPCC / HW accelerators	
7111 000010101010	0x4C00 0000
AHB2	0x4903 FFFF
DMA / ADC /	
SDMMC2	0x4800 0000
APB2	0x4401 37FF
CAN / SAI / TIM /	
USART	0x4400 0000
	0x4001 C3FF
APB1	0
I2C / DAC / TIM / UART / USART	
3, a.t., 00, att	0x4000 0000

	0x3FFF FFFF
RETRAM 64 KB	0x3800 FFFF
TETTO WI OF IED	0x3800 0000
	0x3006 0000
SRAM3 128 KB	0x3000 0000
	0x3004 0000
SRAM2 128 KB	0x3002 0000
SRAM1 128 KB	0x3002 0000
CITO WITT TEO TOD	U^3000 0000

Memory Map overview

- Uniform memory map
 - All peripherals visible on same address of every masters
 - No Remap



Power architecture

Vppa_ppR STM32MP1 Power supplies ______ υUR PHY Core domain V_{DDCORE} Vss (MPU, (MCU, peripherals, peripherals, RAM) RAM) **IOports** logic (System logic, Peripherals) V_{DD} (V_{DD ANA}) V_{DD} HSI, CSI, HSE, VSW domain LSI, WKUP, IWDG Retention do main Retention **IOports** logic regulator Retention V_{BAT} $V_{DD\ PLL}$ Backup domain PLLs Backup regulator VDD domain V_{SS_PLL} Backup RAM LSE, RTC, AWU, BKUP 10 IOports < Tamper, backup logic registers, Reset VDDAL Analog domain REF_BUF ADC, DAC V_{REF+} V_{REF+} V_{REF-} V_{REF-} VSSAF

Mandatory supplies:

VDDQ DDR 1.2V / 1.35V / 1.5V VDDCORE 1.2 V VDD 1.7V - 3.6V

Core domain

4 power domains :

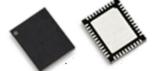
VDD domain VSW domain (V**SW**itch) for Standby Ip mode Analog domain

External Power Supply 14

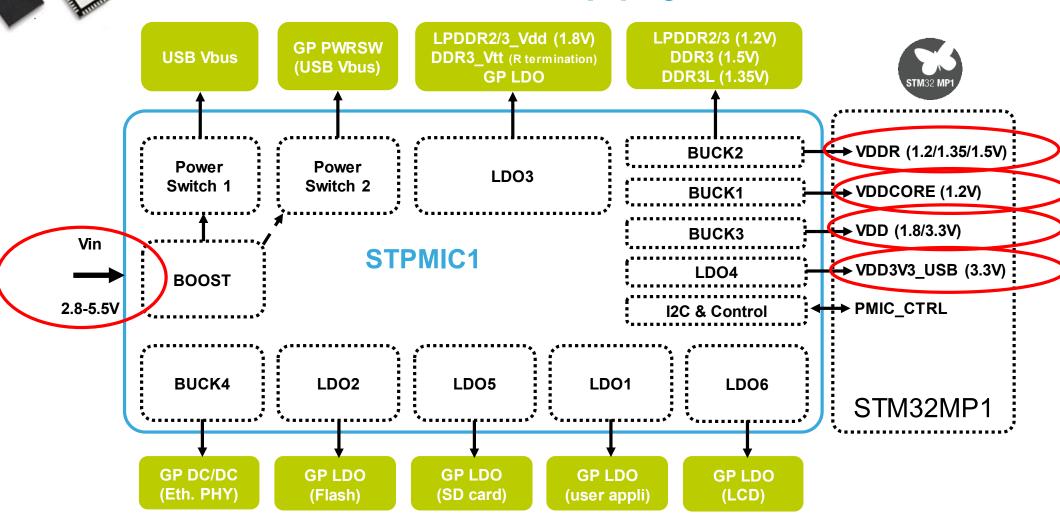
Two solutions:

- STPMIC1 power distribution
 - Better integration on the PCB with a reduced footprint
 - Advanced features such as voltages scaling, short-circuit detection,...
 - Offers power supply for other modules (Wifi, Ethernet Phy, DSI phy)
 - Integrated power switches (USB)
- Discrete power distribution
 - Individual set of regulators on the PCB
 - For minimalist solution (DRAM, FLASH, MPU) for SOM makers for example
 - Fixed voltage





Power supply with STPMIC1 15

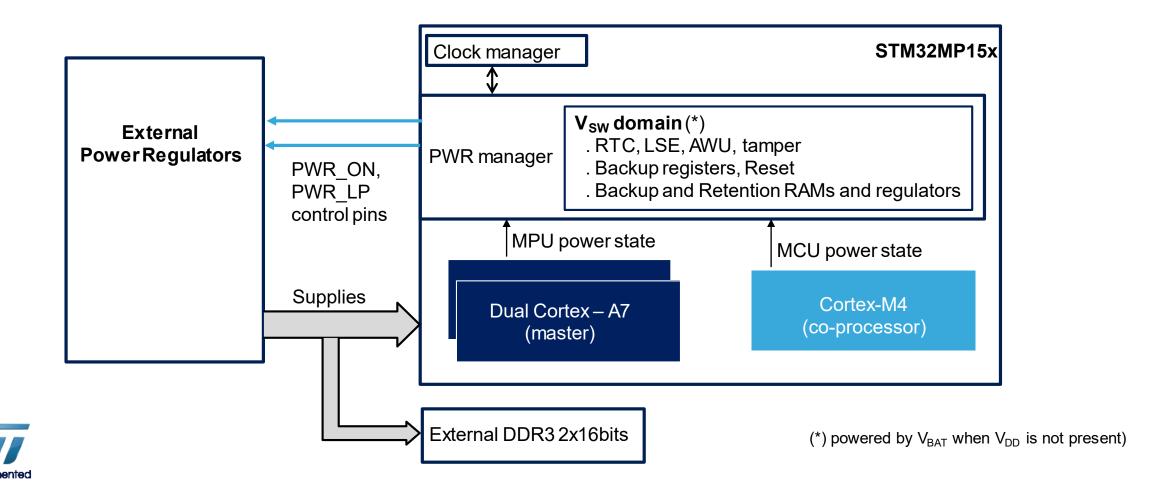




- → STPMIC1 save external Bucks and LDOs on PCB for typical applications
- → 5V Vin allows power using USB

Power Management Architecture 17

System power modes are set by PWR manager based on MPU and MCU power modes



STM32MP1 system power modes 18

System Power Mode	V _{DDCORE}	Clocks	Wakeup sources (not all sources are available in the Linux environment)	
Run	Nominal (typ. 1.2V)	ON	All	
Stop	Nominal (typ. 1.2V)		DBG, PVD, AVD, USBH, OTG, CEC, ETH, MDIOS,	
LP-Stop	Nominal (typ. 1.2V)	MCU and MPU sub-	USARTx, I2Cx, SPIx, TEMP, LPTIMx, GPIOs (+ VBAT mode sources)	
LPLV-Stop	Reduced (typ. 0.9V)	systems clock OFF	PVD, AVD, TEMP, GPIOs (+ VBAT mode sources)	
Standby	0 V		6 GPIO wakeup pins (+ VBAT mode sources)	
VBAT	RTC and backup domain supply provided by optional V _{BAT} supply when V _{DD} is not present		BOR, VBATH/VBATL, TEMPH/TEMPL, LSE CSS, RTC/Auto wakeup, Tamper pins, IWDGx	

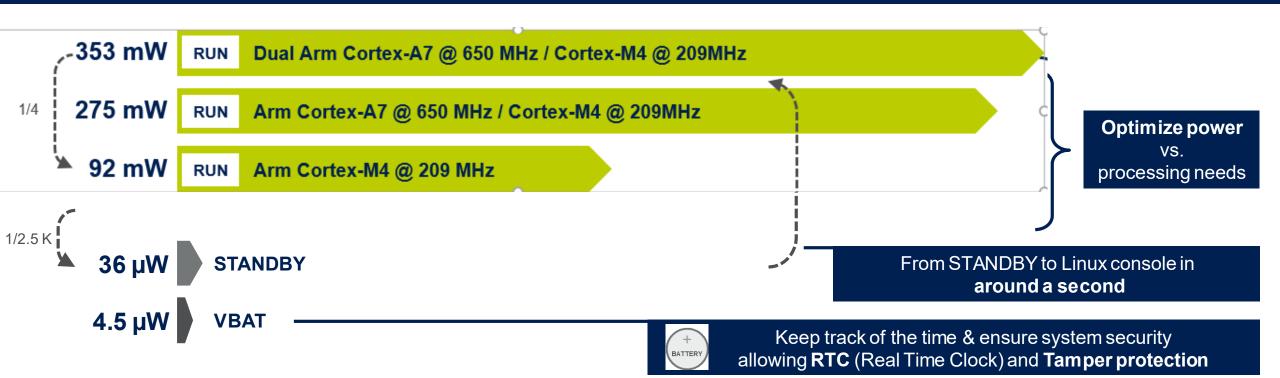
LPLV-Stop requires external power regulator with voltage scaling to lower down VDDCORE supply (to reduce the STM32MP1 consumption)

The STPMIC1 power regulator offers this feature



Flexible Architecture for Power Efficiency

Power figures (VDD+ VDDCORE)



Typ @ VDDCORE = 1.2V, V_{DD} = 3.3 V @ 25 °C, Peripherals OFF



See AN5284: STM32MP1 Series system power consumption

Power documentation 21

- AN5031 Getting started with STM32MP15 Series hardware development
- AN5109 STM32MP15 Series using low-power mode
- AN5256 STM32MP15x Lines discrete power supply hardware integration
- RM0436 reference manual STM32MP157xxx advanced Arm®-based 32-bit MPUs



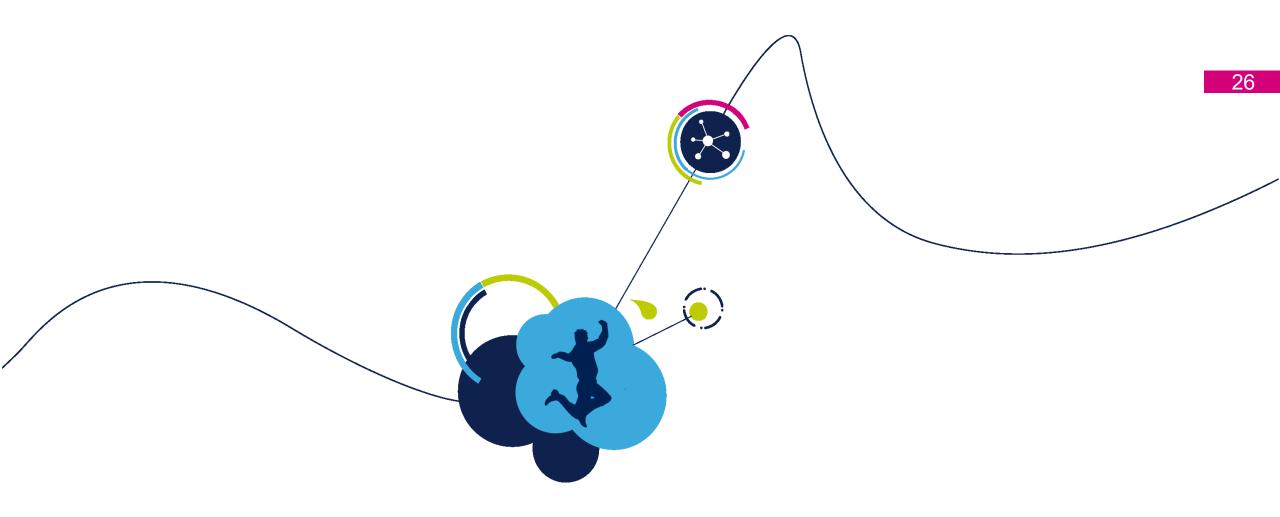


Power Consumption 22

Mode	Conditions V_{DDCORE} = 1.20V, V_{DD} = 3.3V, Tj = 25°C, HSE=24MHz	V _{DDCORE} +V _{DD} Power(Typ.)
Run (A7+M4 Coremark)	All digital powered, All peripherals clocked, Cortex-A7@648MHz, AXI @264MHz, MCU Subsystem @209MHz. No GPU activity. DDR in Self-refresh.	409mW (1x A7 +M4) 487mW (2x A7 +M4)
Run (A7+M4 Coremark)	All digital powered, All peripherals stopped , Cortex-A7@648MHz, AXI @264MHz, MCU Subsystem @209MHz. No GPU activity. DDR in Self-refresh.	275mW (1x A7 +M4) 353mW (2x A7 +M4)
Run (A7 Coremark)	All digital powered, All peripherals stopped , Cortex-A7@648MHz, AXI @264MHz, MCU Subsystem @64MHz, Cortex-M4 in CStop. No GPU activity. DDR in Self-refresh.	229mW (1x A7) 307mW (2x A7)
Run (M4 Coremark)	All digital powered, All peripherals stopped, Cortex-A7 in CStop, MCU Subsystem @209MHz, Cortex-M4 @209MHz. No GPU activity. DDR in Self-refresh.	92mW (M4)
Stop	All digital powered. All Cores stopped . HSE and PLLs are OFF . All peripherals stopped (except those of VBAT domain). DDR in Self-refresh.	26mW
LpLv-Stop	All digital powered. All Cores stopped. HSE and PLLs are OFF. All peripherals stopped (except those of VBAT domain). DDR in Self-refresh. $V_{DDCORE} = 0.9V$.	9.5mW
Standby w/ Retention RAM	V _{DDCORE} OFF , 32KHz and RTC ON. Tamper detection active, 4KB Backup RAM, 64KB Retention RAM. Wake-up on RTC, Tamper event, external wake-up pins. DDR in Self-refresh (optional).	316µW
Standby	V _{DDCORE} OFF, 32KHz and RTC ON. Tamper detection active, 4KB Backup RAM, no 64KB Retention RAM . Wake-up on RTC, Tamper event, external wake-up pins. DDR in Self-refresh (optional).	3ομνν
Off/Vbat	V_{DDCORE} and V_{DD} OFF, 32KHz and RTC ON. Tamper detection active. VBAT=3V (with 4KB Backup RAM enabled)	4.5µW on VBAT



Above data are based on measurements done for datasheet Rev.1 (Silicon Rev.B)



Thanks