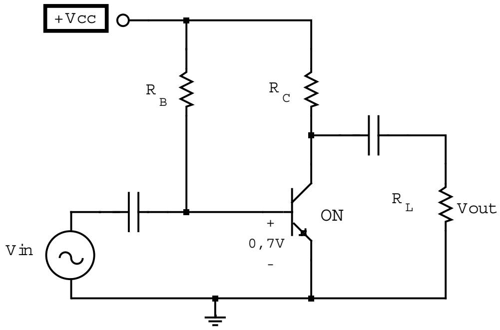
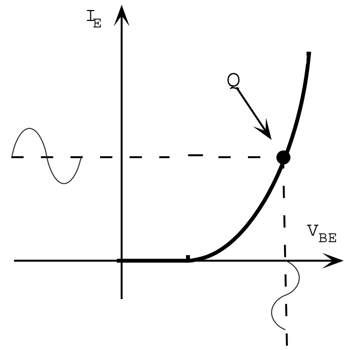
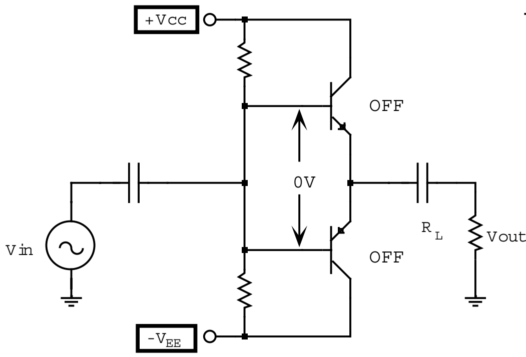
POWER AMPLIFIERS

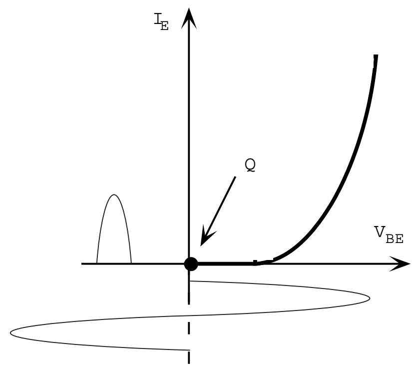
CLASS A



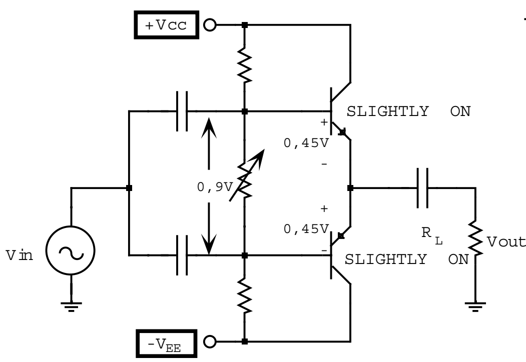


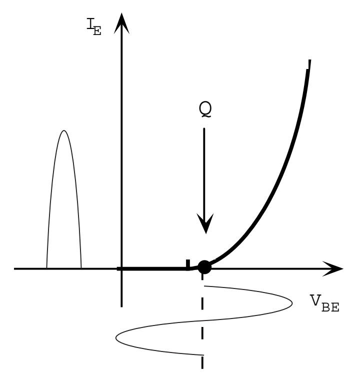
CLASS B



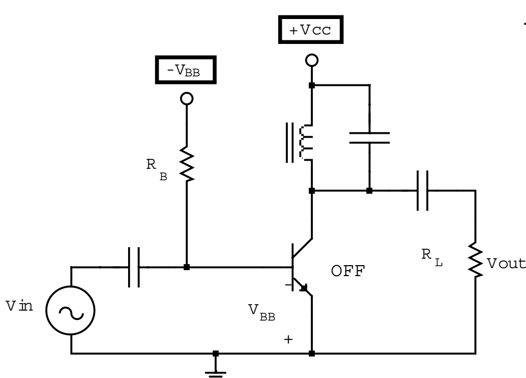


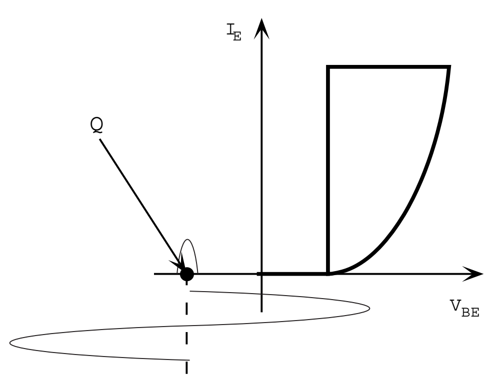
CLASS AB





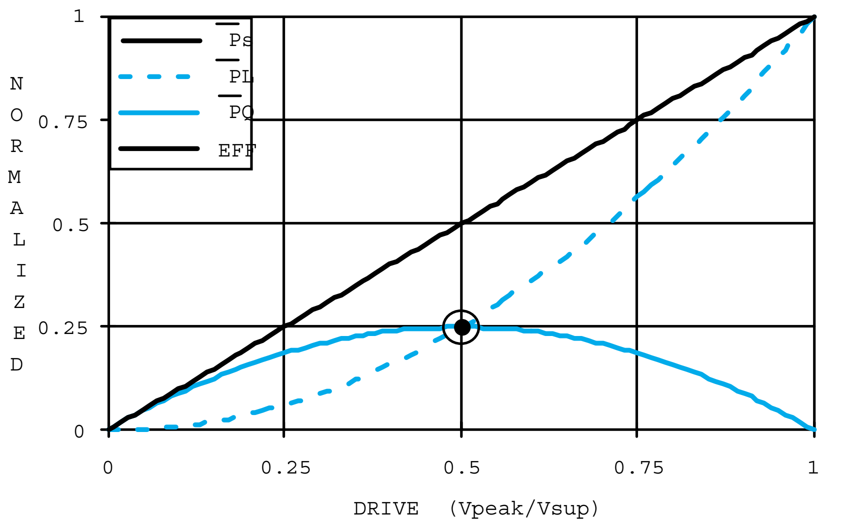
CLASS C





CLASS B AND AB AMPLIFIER POWER CHARATERISTICS

Squarewave input



$$P_{MAX} = P_{S\,MAX} = \frac{V_S^2}{R_L}$$

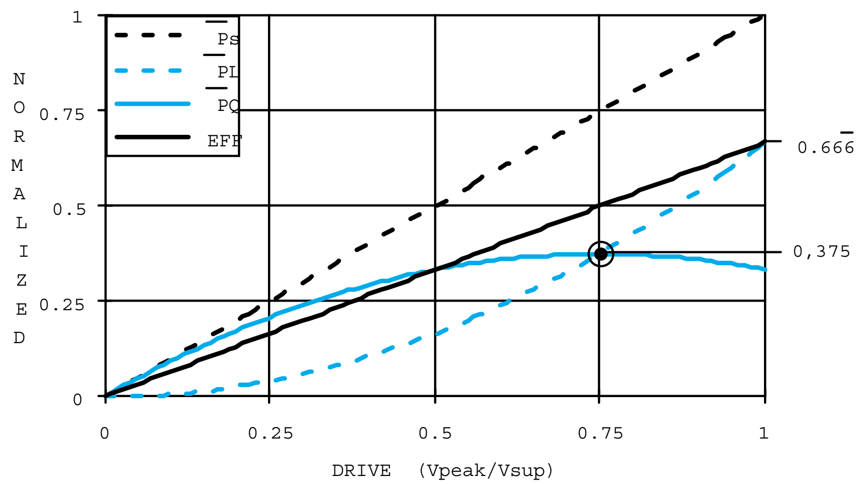
$$\overline{P_S} = \frac{P_S}{P_{MAX}} = dri$$

$$\overline{P_L} = \frac{P_L}{P_{MAX}} = dri^2$$

$$\overline{P_Q} = \frac{P_Q}{P_{MAX}} = dri - dri^2$$

$$eff. = \eta = \frac{P_L}{P_S} = dri$$

Triangular wave input



$$P_{MAX} = P_{S\ MAX} = \frac{V_S^2}{2R_L}$$

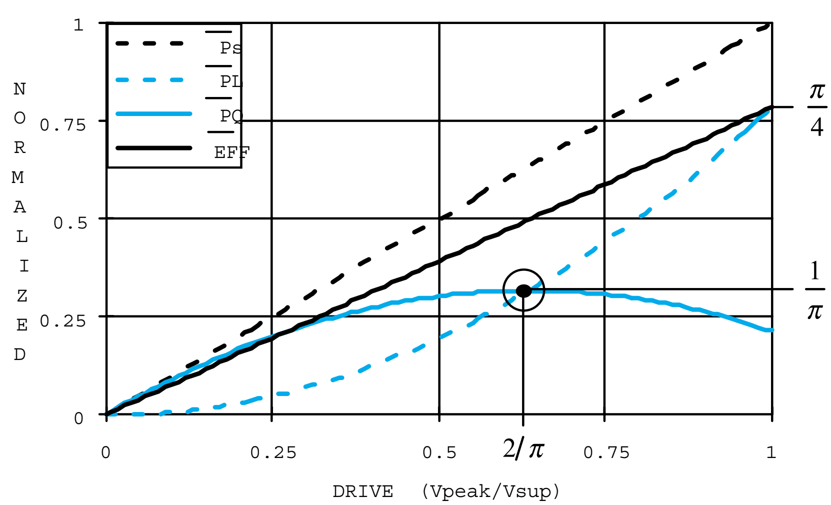
$$\overline{P_S} = \frac{P_S}{P_{MAX}} = dri$$

$$\overline{P_L} = \frac{P_L}{P_{MAX}} = \frac{2}{3}dri^2$$

$$\overline{P_Q} = \frac{P_Q}{P_{MAX}} = dri - \frac{2}{3}dri^2$$

$$eff. = \eta = \frac{P_L}{P_S} = \frac{2}{3}dri$$

Sinewave input



$$P_{MAX} = P_{S\ MAX} = \frac{2}{\pi} \times \frac{V_S^2}{R_L}$$

$$\overline{P_S} = \frac{P_S}{P_{MAX}} = dri$$

$$\overline{P_L} = \frac{P_L}{P_{MAX}} = \frac{\pi}{4}dri^2$$

$$\overline{P_Q} = \frac{P_Q}{P_{MAX}} = dri - \frac{\pi}{4}dri^2$$

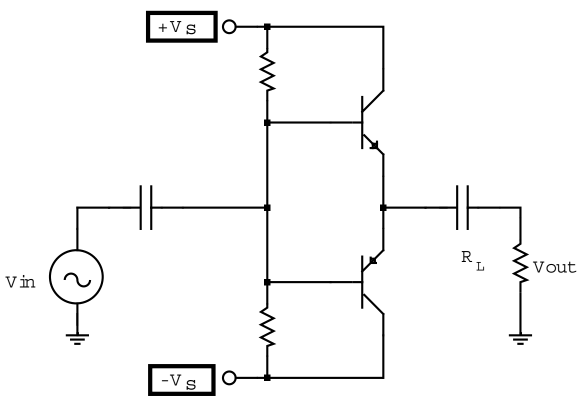
$$eff. = \eta = \frac{P_L}{P_S} = \frac{\pi}{4}dri$$

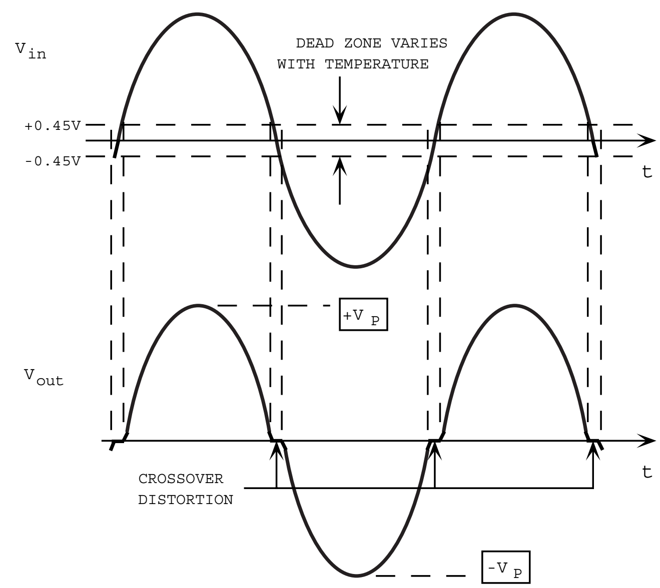
Summary of Class B and AB maximum theoretical ratings

Waveform	η max	P_L max	P_Q max	P_S max
Sinewave	0.785	0.5* V_S^2/R_L	0.202* V_S^2/R_L	0.637* V_S^2/R_L
Squarewave	1.0	V_S^2/R_L	0.25* V_S^2/R_L	V_S^2/R_L
Triangular	0.666	0.333* V_S^2/R_L	0.188* V_S^2/R_L	0.5* V_S^2/R_L

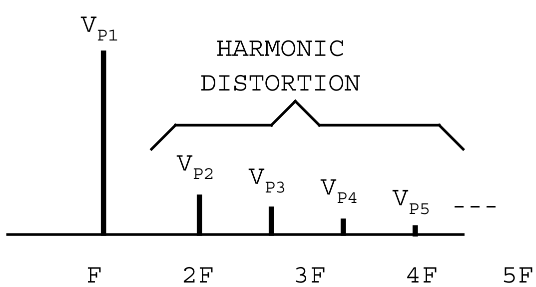
As can be seen from the above results, all of the maximum ratings depend on the actual waveform. For an audio signal, the results will most likely lie somewhere between the sinewave and the squarewave results. In order to implement a safe design, one should consider the worst case, which is the squarewave, to calculate the maximum power ratings of the electronic components.

Crossover distortion in class B power amplifiers





Harmonic distortion



Frequency spectrum

$$\%\,THD = \frac{\sqrt{V_{P2}^2 + V_{P3}^2 + V_{P3}^2 + \cdots}}{V_{P1}} \times 100$$

If one uses a matched transistor pair, the output waveform will be symmetrical and the even harmonics will be eliminated from the spectrum thus reducing the THD.

Reduction of crossover distortion

The three basic ways of reducing crossover distortion are:

A) Use of complementary matched power transistors to eliminate even harmonics caused by asymmetrical distortion.

B) Use of class AB biasing to reduce the dead zone at zero crossover point by slightly turning ON the power transistors.

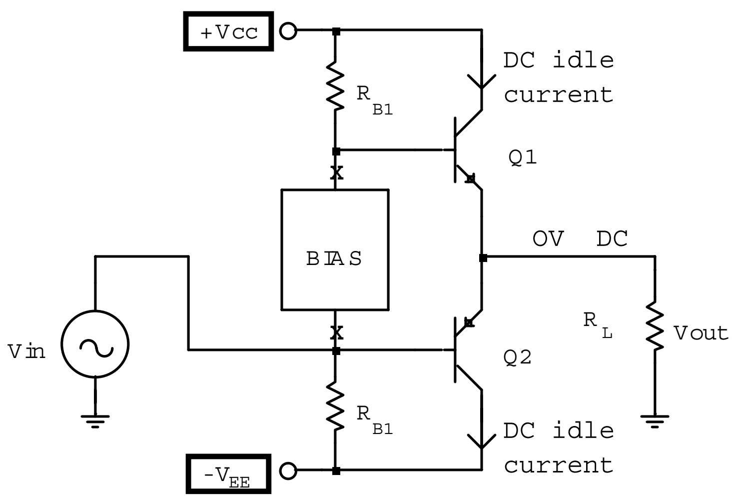
C) Use of negative feedback to greatly reduce the output distortion by a factor of $(1 + \beta_V A_V)$.

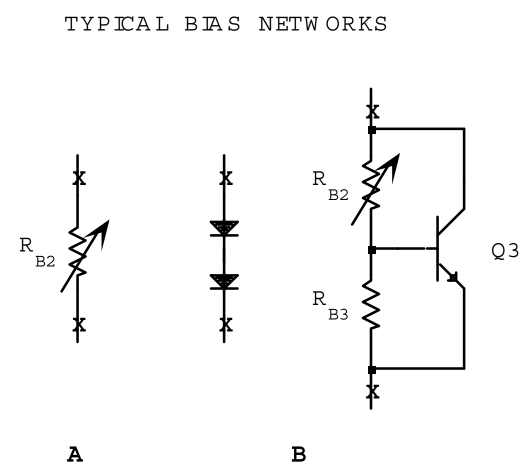
All of the above should be used to reduce distortion to the maximum extent possible.

Complementary matched pair

One can show that by Fourier analysis that if the output waveform is symmetrical with respect to the time axis, then even harmonics vanish in the frequency spectrum. Therefore a complementary matched pair (NPN-PNP pair or N channel- P channel pair) should be used in order to maintain symmetry of the output waveform.

Class AB biasing



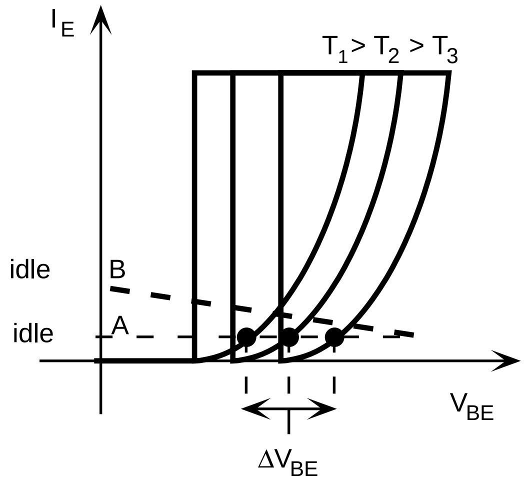


A) Constant voltage biasing with R_{B2} adjusted for desired idle current at one temperature. One could also use a thermistor for R_{B2} (resistor with negative temperature coefficient) thus resulting in a decreasing R_{B2} value as temperature of Q1 and Q2 goes up. This in turn will reduce V_{BE1} and V_{BE2} as temperature goes up.

B) Variable voltage biasing with diode temperature change - rate of about -2,2 mV/°C for a constant diode current.

C) V_{BE} multiplier provides variable voltage biasing with Q3 temperature change - rate of about -2,2 mV/°C for a constant emitter current. $V_{CE3} = (1 + R_{B2}/R_{B3}) * V_{BE3} = V_{BE1} + V_{BE2}$

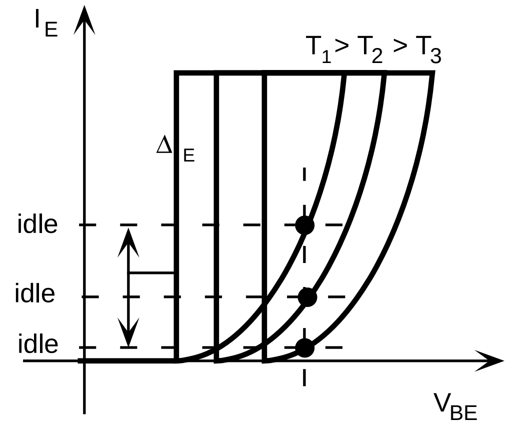
NOTE: The thermistor, or the diodes, or Q3 should be mounted on the same heat sink used for Q1 and Q2 to track the power transistors' temperature.



Constant current biasing

A) Thermistor, or diodes or Q3 temperature tracks Q1-Q2 temperature exactly.

B) Thermistor, diodes or Q3 temperature does not track Q1-Q2 temperature.



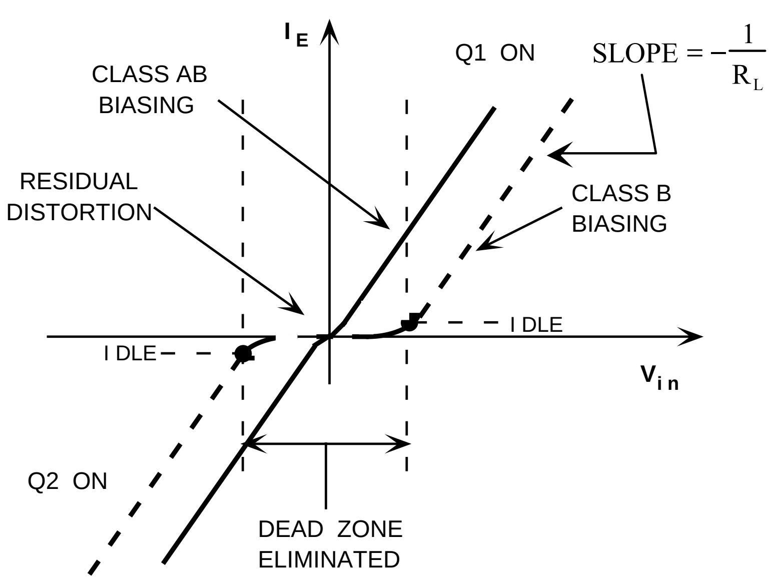
Constant V_{BE} biasing

With single resistor R_{B2}

Using a simple resistor (R_{B2}) to turn Q1 and Q2 slightly ON, provides a constant V_{BE} to Q1 and Q2 and thus will result in varying idle current as the temperature of Q1 and Q2 changes with variations in ambient temperature and power dissipation. This could lead to unreasonnably high idle currents as the temperature of the power transistors goes up.

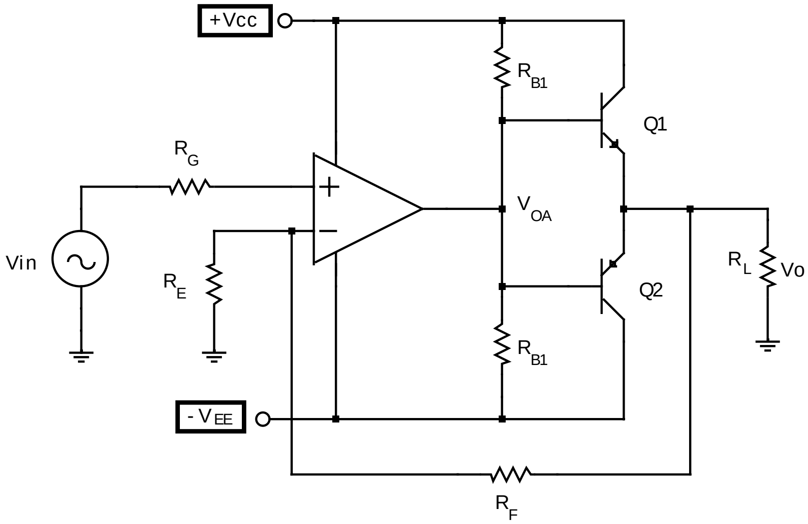
Ideally, the best way of biasing the power transistors is to allow V_{BE} of Q1 and Q2 to vary with temperature changes such that the idle current remains perfectly constant. This can be accomplished only if thermistor, the bias diodes or Q3 are mounted on a common heat sink with Q1 and Q2 and the silicon temterature of Q1, Q2 and Q3 (or of diodes) tracks perfectly over the temperature range (line A). In practice, temperature tracking is never perfect and this will result in variations of the idle current (line B).

<u>Residual distortion</u>



Class AB does not eliminate crossover distortion completely. In general as the idle current is increased, the residual distortion is reduced. One cannot make the DC idle current too large because the DC power dissipated in the circuit becomes too great and the efficiency goes down. It is better to use a small idle current and to attenuate the residual distortion with negative feedback thus maintaining a good power efficiency.

Negative feedback



$$\beta_V = \frac{V_F}{V_O} = \frac{R_E}{R_E + R_F} \qquad V_O = V_{OA} - V_{BE} = A_V(V_{in} - \beta_V V_O) - V_{BE}$$

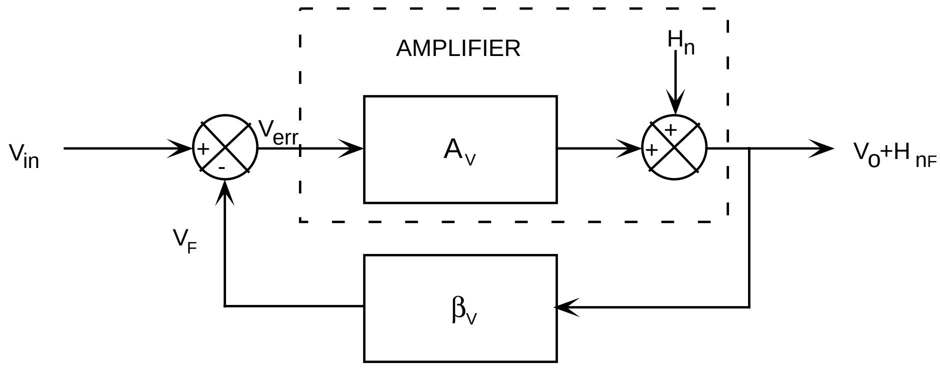
$$V_O = \underbrace{\left[\frac{A_V}{1+\beta_V A_V}\right] V_{in}}_{\text{I/P signal amplified}} - \underbrace{\frac{V_{BE}}{1+\beta_V A_V}}_{\text{O/P dead zone}} = A_{VF} V_{in} - \frac{V_{BE}}{1+\beta_V A_V}$$

$$\text{O / P dead zone distortion } \Delta V_o = \pm \frac{V_{BE}}{1+\beta_V A_V}$$

$$\text{I / P dead zone } \Delta V_{in} = \frac{\Delta V_o}{A_{VF}} = \pm \frac{V_{BE}}{A_V} \quad \text{where} \quad A_{VF} = \frac{A_V}{1+\beta_V A_V}$$

The I/P dead zone is reduced by the gain of the op amp. As most op amps are internally stabilised for -ve feedback by rolling their gain down at -20 dB/dec starting at very low frequencies, the crossover distortion (dead zone) will increase as frequency goes up. Therefore one show use a larger GBW op amp for better high frequency performance.

Harmonic distortion



H_n : n^{th} harmonic introduced by distortion in amplifier alone
H_{nF} : n^{th} harmonic introduced by distortion in amplifier with feedback

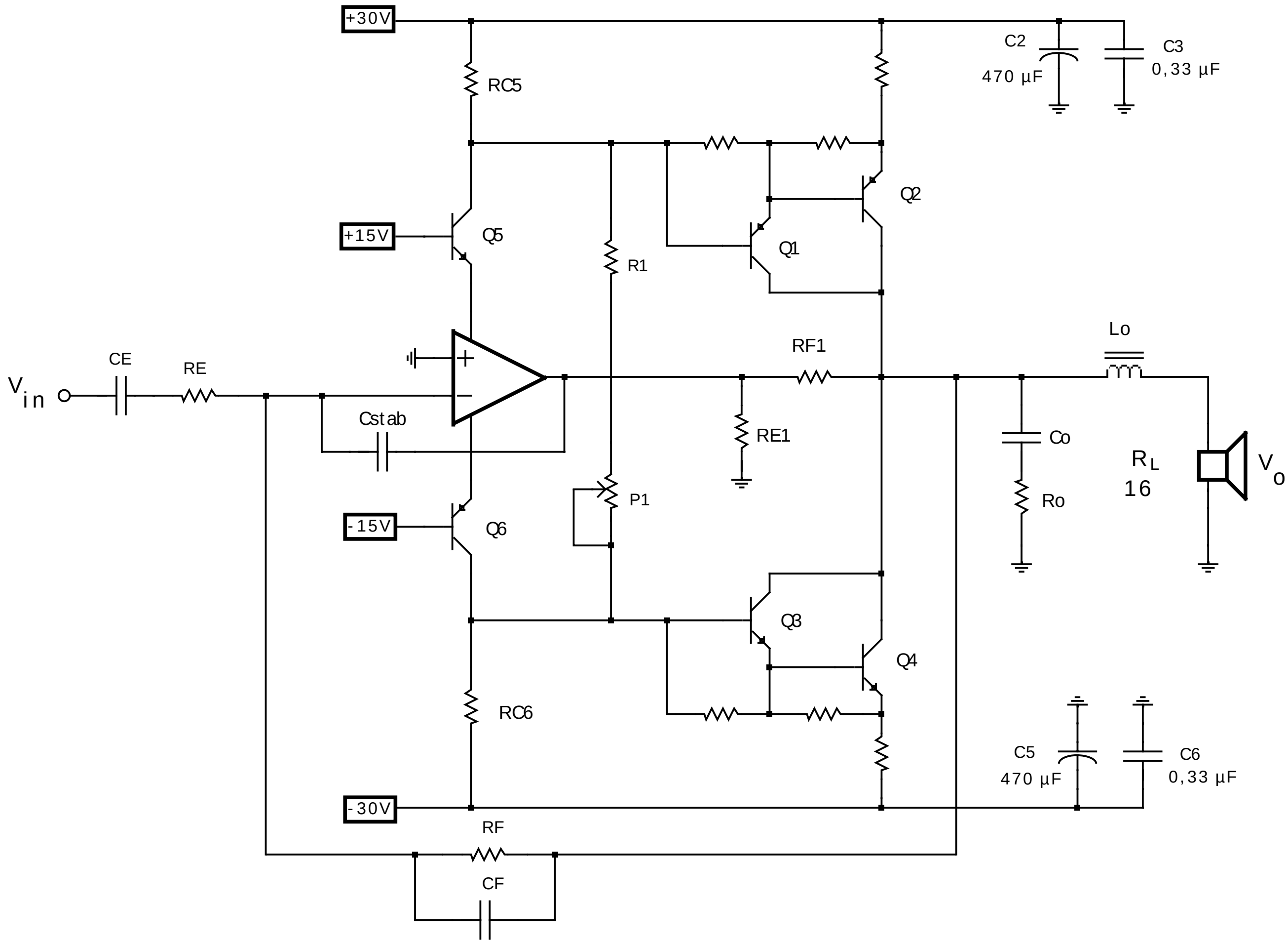
Using superposition theorem and Mason's rule we can solve for the output.

$$V_O + H_{nF} = \underbrace{\left[\frac{A_V}{1+\beta_V A_V}\right] V_{in}}_{\text{I/P signal amplified}} + \underbrace{\frac{H_n}{1+\beta_V A_V}}_{\text{O/P distortion}}$$ and if $\beta_V A_v >> 1$ $$V_O + H_{nF} = \underbrace{\left[\frac{V_{in}}{\beta_V}\right]}_{\text{I/P signal amplified}} + \underbrace{\frac{H_n}{\beta_V A_V}}_{\text{O/P distortion}}$$

This result is very similar to the one obtained for the output dead zone distortion. H_n is reduced by a factor of $(1 + \beta_v A_v)$ which shows again that if an op amp is used, its gain will decrease at a rate of -20 dB/dec and will attenuate less the high frequency harmonics.

$$\%\,\mathrm{THD} = \frac{\sqrt{H_{2F}^2 + H_{3F}^2 + H_{4F}^2 + \cdots}}{H_{1F}} \times 100$$

EXAMPLE#1 CLASS AB POWER AMP WITH COMMON EMITTER POWER STAGE



R_{E1}-R_{F1}: introduces inside feedback to reduce the gain from op amp output to final O/P, that is:

$$\frac{V_O\,final}{V_O\ op\ amp} \approx 1 + \frac{R_{F1}}{R_{E1}}$$ otherwise the op amp feedback loop would be hard to stabilize.

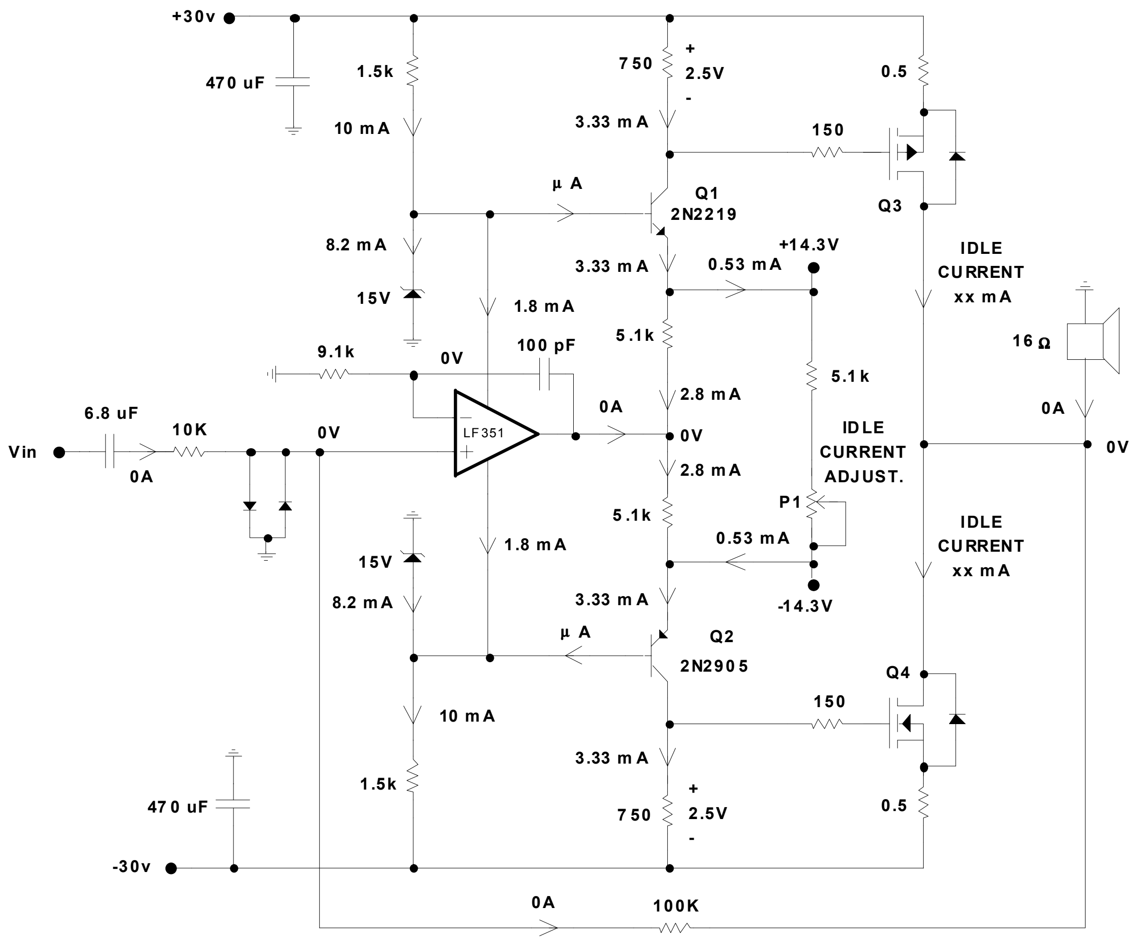
The small emitter resistors of Q2 and Q4 are needed for bipolar transistors to avoid thermal runaway – usually 0.5V to 1.5V is sufficient to prevent thermal runaway.

P1 adjusts the DC idle current of Q2 and Q4 bysetting the voltage across R_{C5} and R_{C6}:

$$V_{RC5} \approx V_{BE1} + V_{BE2} \quad and \quad V_{RC6} \approx V_{BE3} + V_{BE4}$$

Lo, Ro and Co form a “snubber” that is a circuit used to attenuate any high voltage kickback from the highly inductive speaker. This protects the O/P transistors from high voltage breakdown.

EXAMPLE # 2 CLASS AB POWER AMP – DC CONDITIONS



DC conditions in amplifier

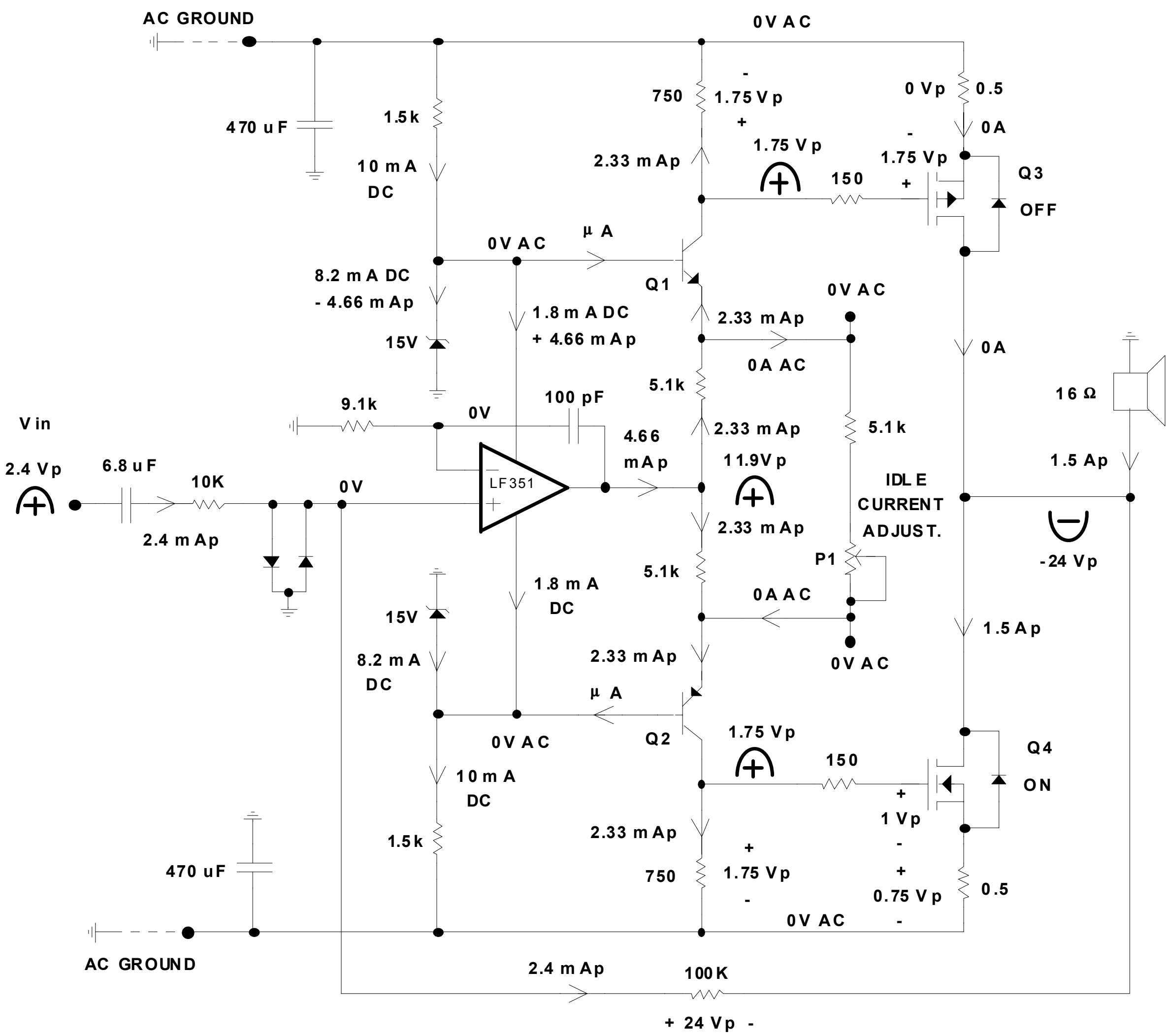
Assumptions: Q3 is an RFP12P10 P channel MOSFET with Q4 being a matched N channel MOSFET
Q3 and Q4 are DC biased near threshold with a typical V_{GS} of 2.5V to provide an idle current of 10 to 50 mA which helps reduce crossover distortion.

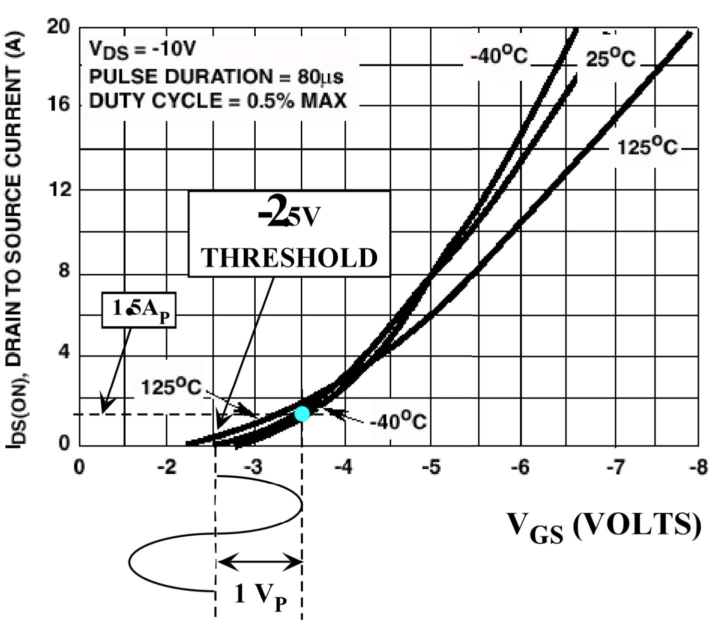
The LF351 operates with 1.8 mA typical supply current.

The diodes across the MOSFET's are the substrate diodes of the MOSFET's and protect them against high voltage kickback (back emf in more proper terms) which can occur with inductive loads – audio speakers are mostly coil type with high inductance value that can generate a lot of back emf (several thousand volts) when current is suddenly interrupted $V_L = L\frac{dI_L}{d\,t}$. The 0.5 ohm resistors in series with the source of the MOSFET's limit the surge current the back emf can produce.

Potentiometer P1 adjusts the voltage across the two 750 resistors which is rougly equal to V_{GS} of the MOSFET's if we ignore the drop across the 0.5 ohm resistors. This works fine as long as the MOSFET's are matched and need the same V_{GS} to operate. In case of mismatch, the two V_{GS} must be different and one needs a second pot to balance the O/P of the op amp to 0V while providing two different V_{GS} values.

EXAMPLE # 2 CLASS AB POWER AMP – AC CONDITIONS

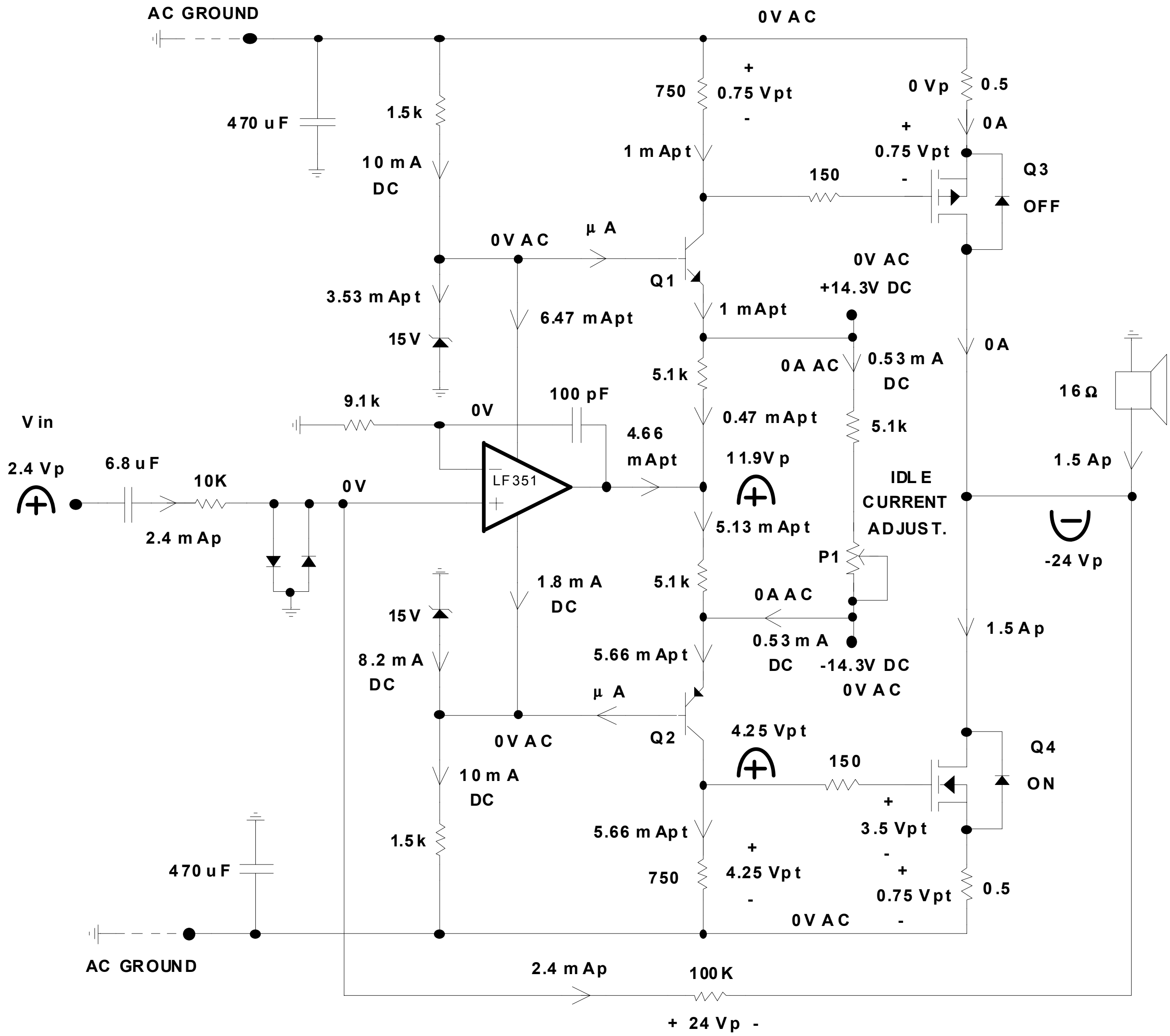




NOTE: The AC voltage at the base of Q1 has been assumed 0V but in practice it would be -4.66 mAp* r_z where r_z is the AC or dynamic resistance of the Zener diode that can be obtained from the data sheets. The result would be a few tens of mV AC which is negligible compared to 11.9 V_P at the op amp O/P.

The second assumption is that the AC emitter voltages are also 0V which is an approximation. In fact we have: v_{e1} = -4.66 mA_P* r_z + 2.33 mA_P* r_{e1} and v_{e2} = 2.33 mA_P* r_{e2} where r_{e1} and r_{e2} are the AC or dynamic resistances of the EB junctions of Q1 an Q2 which would be around 10Ω when operating at 3.33 mA DC. This shows that those AC voltages are of the order of 20 mV_P to 30 mV_P and can be ignored compared to the large op amp O/P voltage of 11.9 V_P.

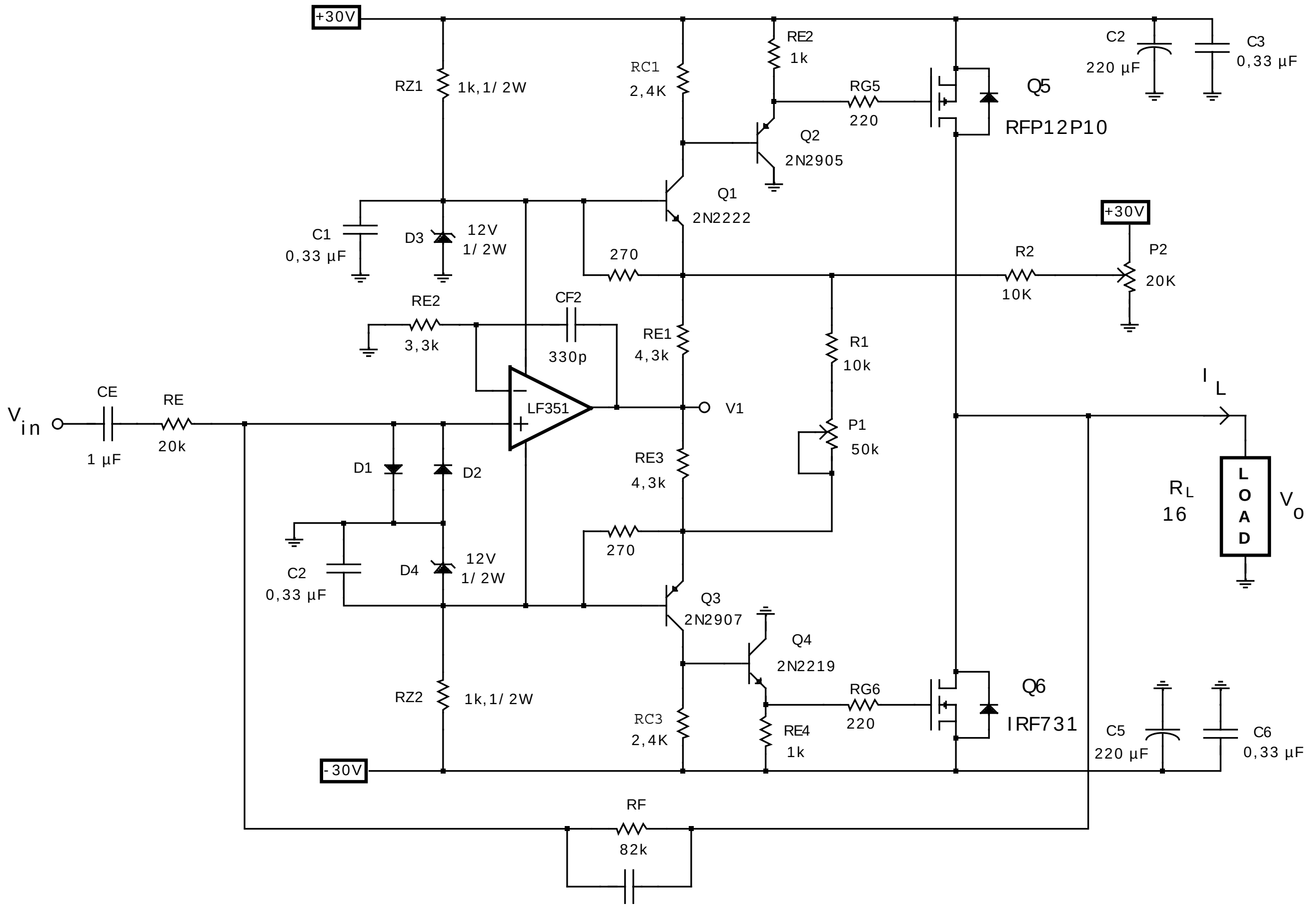
EXAMPLE # 2 **CLASS AB POWER AMP – DC + AC CONDITIONS**



The above values are the instantaneous values of the currents and the voltages that occur at the peak of the AC waveforms and include the AC plus the DC components together when labeled xx A_{pt} or xx V_{pt} . Some straight DC and AC values still appear on the circuit diagram.

Of particular importance is the fact that the top MOSFET is completely OFF as its minimum instantaneous V_{SG} reaches 0.75 V_{Pt} which is well below the threshold that was assumed to be 2.5 V.

EXAMPLE#3 **CLASS AB POWER AMP**



A) Assuming that the MOSFET's have a $|V_{GS(TH)}|$ that ranges from 2V to 4V, determine the values of R1, P1, R2 and P2 are appropriate.

B) If V_{in} = 3 V_P, determine the peak AC values of V_o, V_1, V_{gs5} and I_{OA} .

C) If $R_{DS\,(ON)}$ = 0,5Ω for the MOSFET's, determine V_o max, P_L max and the maximum efficiency of this amplifier and P_{max} of each MOSFET assuming a sinewave input.

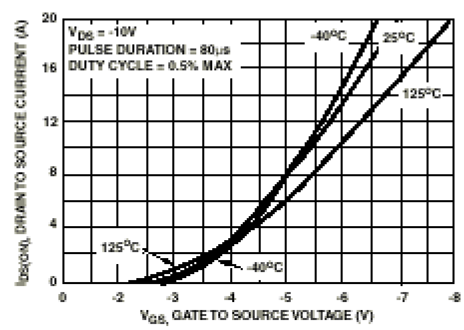
D) Repeat question C for a square wave input.

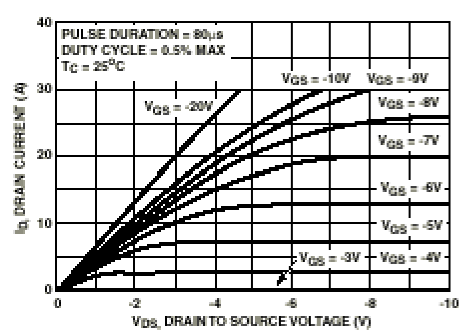
E) Explain what crossover distortion is and what are the two features of the above circuit that contribute to reduction of crossover distortion.

F) As frequency increases, how will THD vary ? Explain.

G) Determine the gain response of the amplifier.

$$A_{V(tot)} = -\frac{Z_F}{Z_E} = \frac{V_o}{V_{in}} \qquad A_{V2} = \frac{R_{C1}}{R_{E1}} = \frac{R_{C3}}{R_{E3}}$$



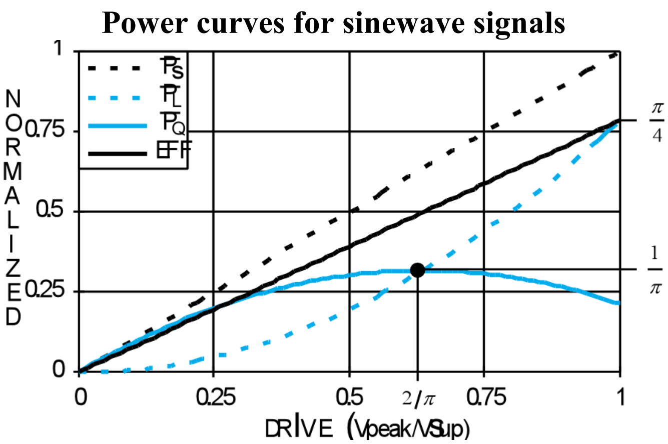


LM3886 Overture™ Audio Power Amplifier .

The LM3886 is made by National Semiconductors Inc. and is a single chip power amp capable of outputting up to 68W of continuous average power into a load. Depending on the supply voltages and the load resistance used, the maximum output power will vary. See data sheets for details.

Maximum O/P Power and Maximum IC power

Using the specs for $R_L = 4\Omega$ and $V_S = \pm 28V$ we are told P_L max = 68W typical. Let's determine the heat sink required to handle the maximum IC power dissipation. Assuming a sinewave input, we have:

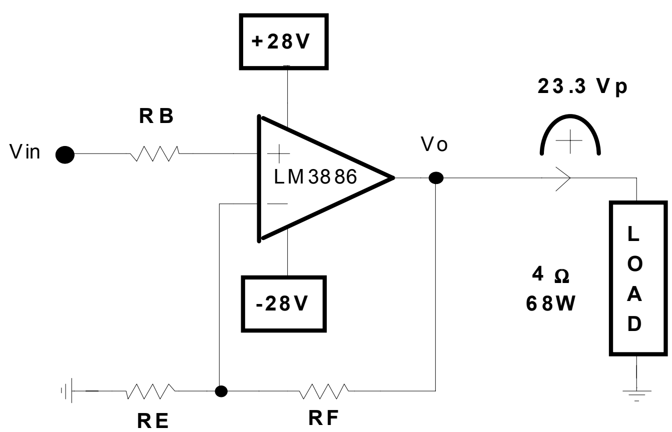


$$P_{MAX} = P_{S\,MAX} = \frac{2}{\pi} \times \frac{V_S^2}{R_L} \qquad \overline{P_L} = \frac{P_L}{P_{MAX}} = \frac{\pi}{4} dri^2$$

$$\overline{P_Q} = \frac{P_Q}{P_{MAX}} = dri - \frac{\pi}{4} dri^2$$

Remember that P_Q max = P_{IC} max is reached when $V_P = 2V_S/\pi$ which does not occur at the same drive level than maximum O/P power (P_L max) that occurs at maximum drive level or maximum V_P.

$$P_{Q\,MAX} = \frac{P_{S\,MAX}}{\pi} = \frac{2}{\pi^2} \times \frac{V_S^2}{R_L} = \frac{2}{\pi^2} \times \frac{28^2}{4} = 39.7W \approx 40W$$



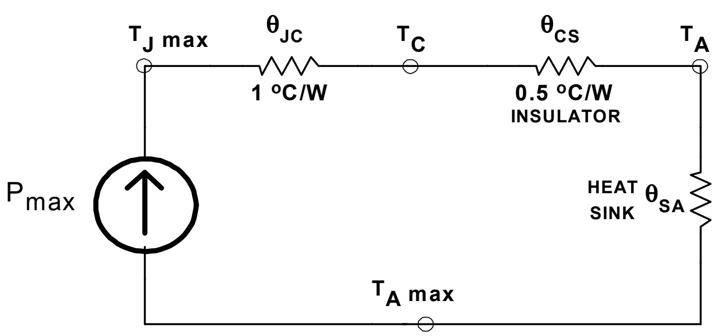
Assuming a maximum junction temperature of 150°C (thermal shutdown actually kicks in at 165 °C) we have:

$$P_L \max = \frac{V_P^2}{2R_L} \text{ for a sinewave O/P (average power)}$$

therefore for 68W of O/P power we have:

$$V_P = \sqrt{2P_L \max R_L} = \sqrt{2 \times 68 \times 4} = 23.3V$$

and $I_P = 23.3 / 4 = 5.83\ A_P$



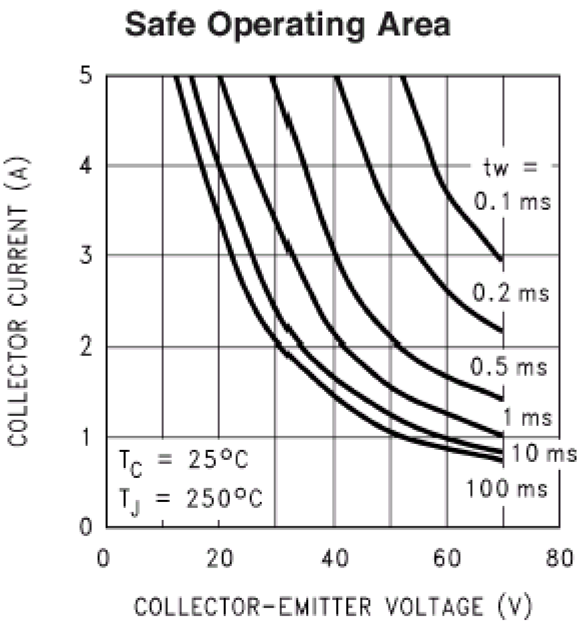
$$P_{MAX} = \frac{T_J \max - T_A \max}{\theta_{JA}} = \frac{150-40}{\theta_{JA}} = 40W$$

$$\Rightarrow \quad \theta_{JA} = 2.75$$

and θ_{SA}, = 2.75- 1.5 = 1.25 °C/W

This is a reasonable heat sink.

The amount of O/P power that can be obtained depends on the size of the heat sink and T_J max provided I_o or V_o is within the safe operating area (SOA) of the LM3886.

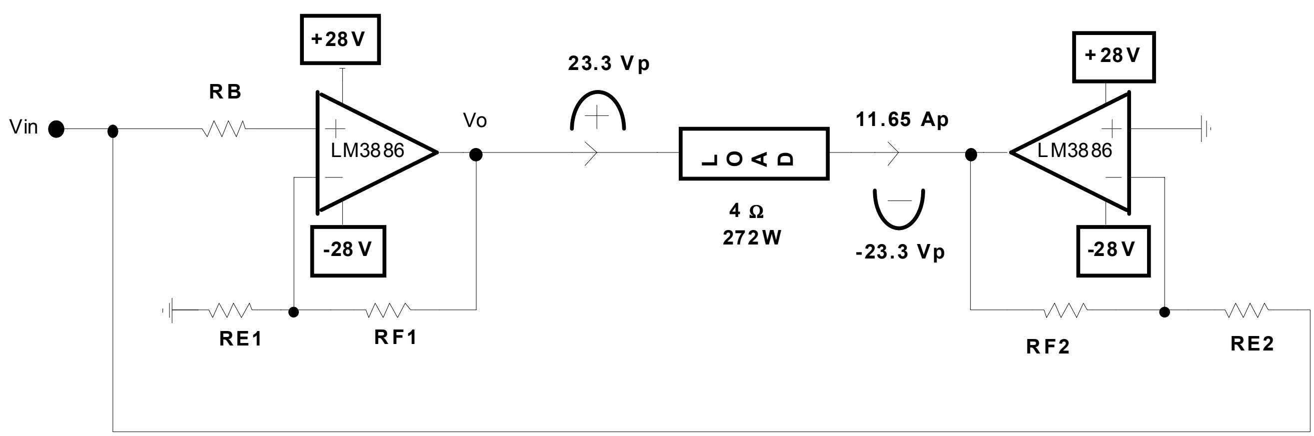


For short amounts of time, the LM3886 can provide upwards of 200W of instantaneous power to the load as it allows the junction temperarure to reach 250 ^{o}C above which SPIKe* protection kicks in to protect the O/P power transistors of the LM3886.

* See AN-898 for extensive SPIKe protection description.

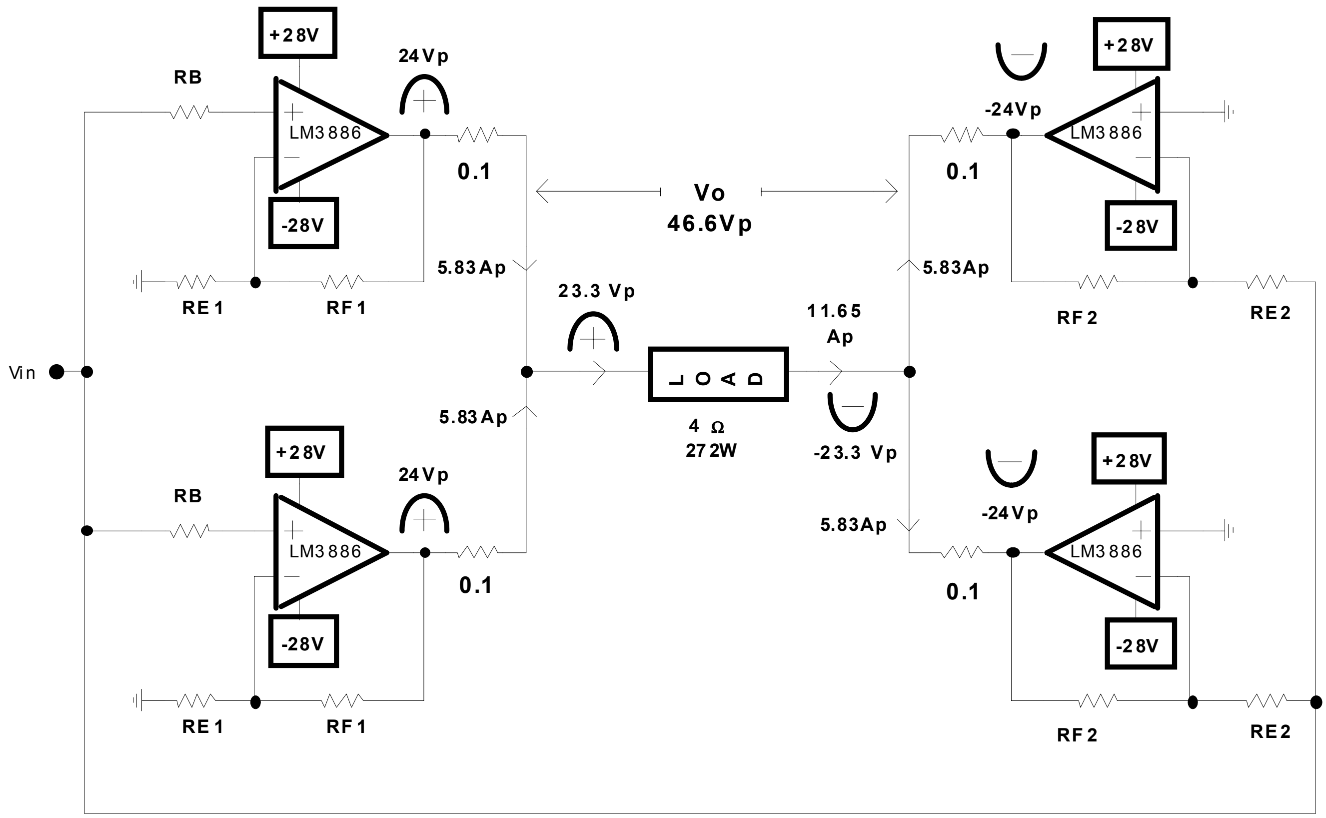
BRIDGE CONFIGURATION

Now if we want to increase the amount of power to the same 4Ω load, we can use a bridge configuration and double the voltage across the load using the same power supply voltages.



Now with a peak voltage of 46.6 V_P we can deliver 272W to the load. Now the problem is that **<u>if we keep the same heat sink</u>** on the LM3886's then the maximum power they can each dissipate stays the same therefore they will not be able to deliver the 11.65 A_P required because the maximum power dissipation is now: P_{IC} max $= 2\ V_S^2/\ (\pi^2 R_L) = 2*28^2/(\pi^2\ *2) = 79.4W \sim 80W$ as the load resistor appears to be a 2Ω resistor seen by each O/P alone, that is $R_{EQ} = 23.3\ V_P/\ 11.65A_P = 2\Omega$. Because each LM3886 now ouputs twice the current it normally does, it dissipates twice the power it did before. To be able to deliver 272W to the load, we now have to use four LM3886's in a bridge parallel configuration as shown below.

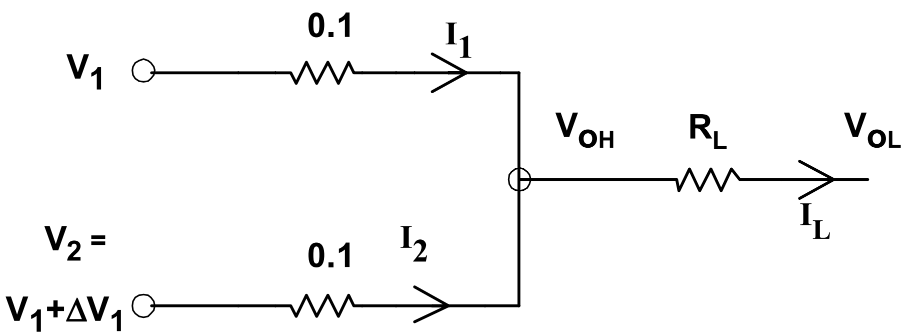
BRIDGE-PARALLEL CONFIGURATION



Now the load current is shared 50/50 between two amplifiers connected in parallel and the equivalent load resistance seen by each amplifier is now $R_{EQ} = 24\ V_P / 5.83\ A_P = 4.1\Omega$. The O/P currents of each amplifier will be equal only if their O/P voltages are exactly equal and the 0.1Ω resistors are equal.

This means that the gains are exactly the same: $A_{NI} = |A_{INV}| = 1 + \frac{R_{F1}}{R_{E1}} = \frac{R_{F2}}{R_{E2}}$

The O/P voltages of each amplifier will not be exactly the same therefore the 0.1Ω resistors are used to isolate them as they cannot be connected directly together.



$$I_1 = \frac{V_1 - V_{OH}}{0.1} \qquad I_2 = \frac{V_1 + \Delta V_1 - V_{OH}}{0.1} \qquad \Delta I = I_2 - I_1 = \frac{\Delta V_1}{0.1} = \frac{A_{V2}V_{in} - A_{V1}V_{in}}{0.1} = \frac{\frac{R'_{F2}}{R'_{E2}}V_{in} - \frac{R''_{F2}}{R''_{E2}}A_{V1}V_{in}}{0.1}$$

Using 1% gain setting resistors, we have:

$$\Delta I = I_2 - I_1 = \frac{\Delta V_1}{0.1} = \frac{\frac{1.01\times R_{F2}}{0.99\times R_{E2}}V_{in} - \frac{0.99\times R_{F2}}{1.01\times R_{E2}}V_{in}}{0.1} = \frac{1.02\times\frac{R_{F2}}{R_{E2}}V_{in} - 0.98\times\frac{R_{F2}}{R_{E2}}A_{V1}V_{in}}{0.1} = \frac{0.04\times\frac{R_{F2}}{R_{E2}}V_{in}}{0.1}$$

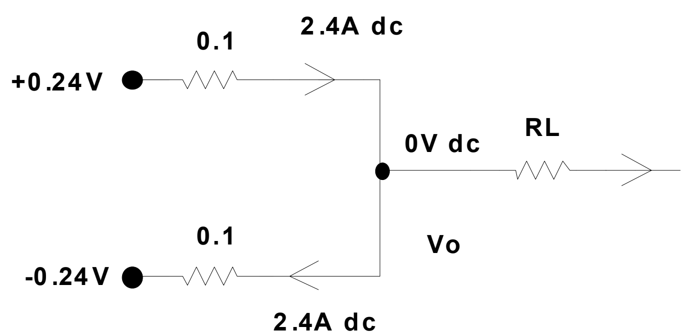
$$\Delta I \max = I_2 - I_1 = \frac{4\times\frac{TOL}{100}\times V_1 nom}{0.1} = \frac{0.04\times 24}{0.1} = \frac{0.96}{0.1} = 9.6A$$

This demonstrates that 1% resistors would not be appropriate as the worst case current imbalance is out of sight. Using 0.1% resistors the worst case imbalance would be 0.96A relative to 5.83A_P which is more acceptable. To further reduce the current imbalance with 0.1% gain setting resistors, one has to increase the 0.1Ω resistors. Say we use 0.2Ω instead, then ΔI = 0.48A max relative to 5.83 A_P which is more acceptable. One must realize that a severe current imbalance will result in different power dissipation for the current sharing parallel amplifiers and may result in premature thermal shutdown of the amplifier as the junction temperatures would be imbalanced.

O/P DC Current

O/P offset voltage can cause a large DC current to flow from one parallel amp to the other and introduce unnecessary power dissipation. Let's assume the input AC voltage is 1V_P max, therefore we need a gain of 24V/V to produce 24 V_P. As shown on the previous page, the bridge-parallel amplifier has a serious flaw with respect to DC offsets.

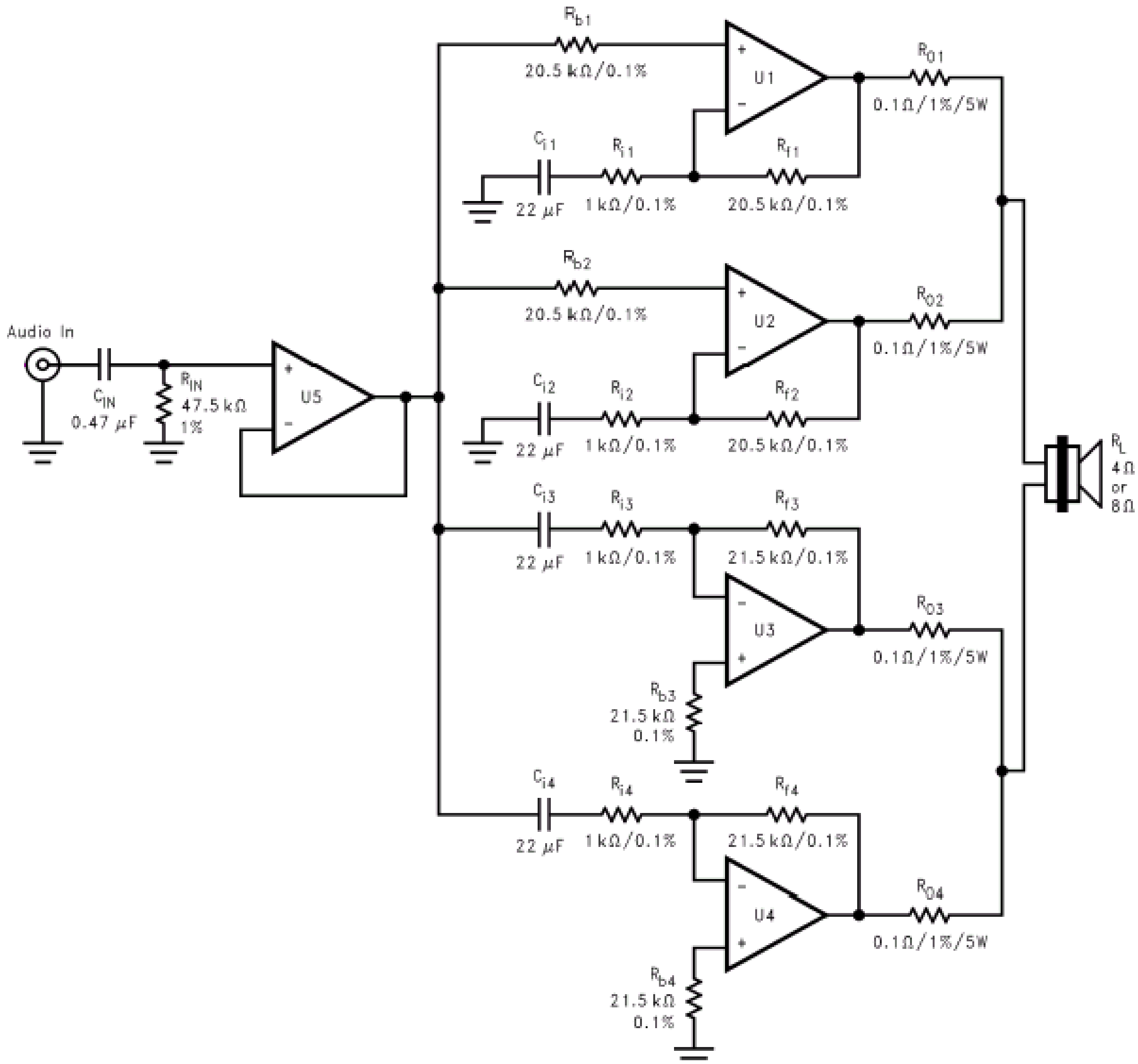
The maximum input offset voltage specified for the LM3886 is 10 mV, therefore V_{oo} max = 24*10mV = 0.24V which can be either +ve or –ve. This results in 2.4A dc maximum flowing from one amplifier to the other. This is totally unacceptable.



To solve the this problem all R_E's are AC coupled to ground and the input signal is AC coupled to remove any DC component. The input offset voltages are now amplified by a gain of one, that is V_{oo} = V_{io} = ±10 mV max which will produce a maximum DC current of I_{DC} max = 20mV / 0.2Ω = 0.1A .

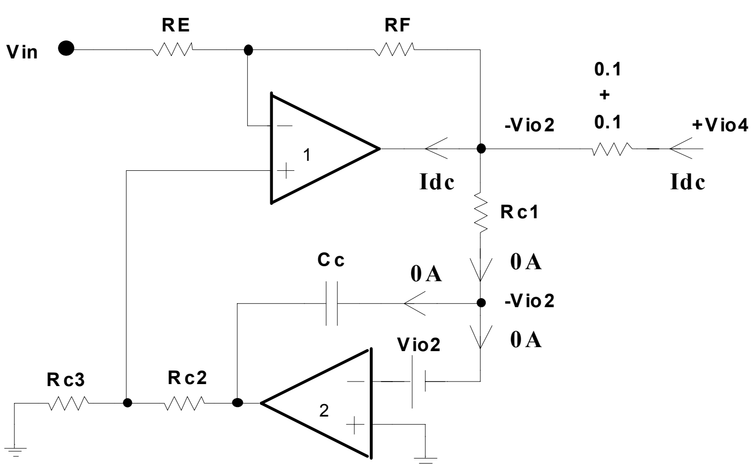
Those capacitors will introduce a low cutoff frequency in the gain response. The 22 µF capacitors have to be non-electrolytic and can be bulky and expensive.

See circuit on the next page.



Bridge-Parallel Amplifier with AC coupling used to lower V_{oo} of the LM3886's

BRIDGE-PARALLEL AMPLIFIER WITH DC AUTOZERO FEEDBACK LOOP

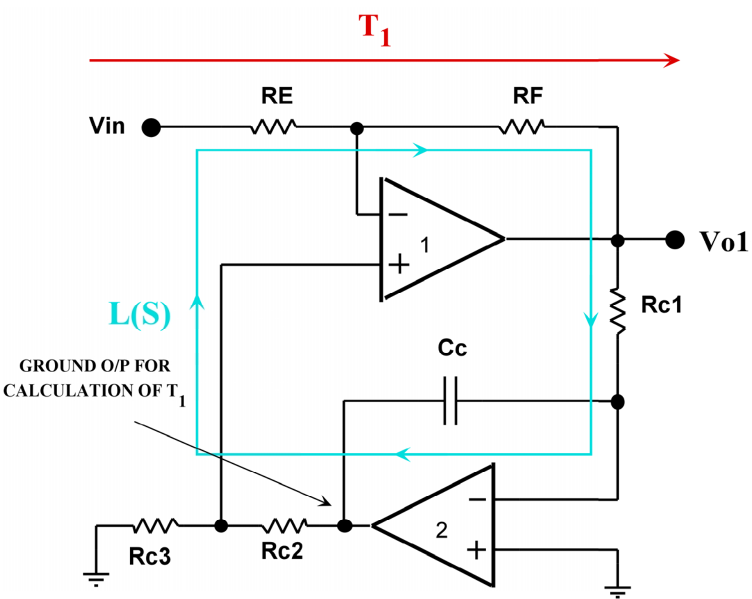


Op amp 2 will force V_{o1} to equal $-V_{io2}$ As no DC current flow through R_{C1} . Although there is no DC feedback through C_c, there is a DC feedback loop through op amp 2, R_{C2}-R_{C3}, op amp 1 and back through R_{C1} which will force V^- of op amp 2 to equal V^+ ideally if V_{io} is zero.

I_{DC} max = 2 V_{io} max/0.2 = 2*1 mV/0.2
I_{DC} max = 10 mA for LF412A's whose V_{io} max is specified as 1 mV.

The non-inverting amplifiers have a different DC autozero circuit but the result is the same.

TRANSFER FUNCTION OF INVERTING AMPLIFIER WITH AUTOZERO LOOP



Using Mason's rule we have:

$$\frac{V_{o1}}{V_{in}} = \frac{\sum T_k N_k}{1-\sum B_1 + \sum B_2 - \sum B_3 + \ldots} = \frac{T_1 N_1}{1-B_1}$$

$$T_1 = -\frac{R_F}{R_E} \quad N_1 = 1 \quad B_1 = L(S)$$

$$L(S) = -\frac{1}{SC_C R_{C1}} \times \frac{R_{C3}}{R_{C2}+R_{C3}} \times \left(1+\frac{R_F}{R_E}\right)$$

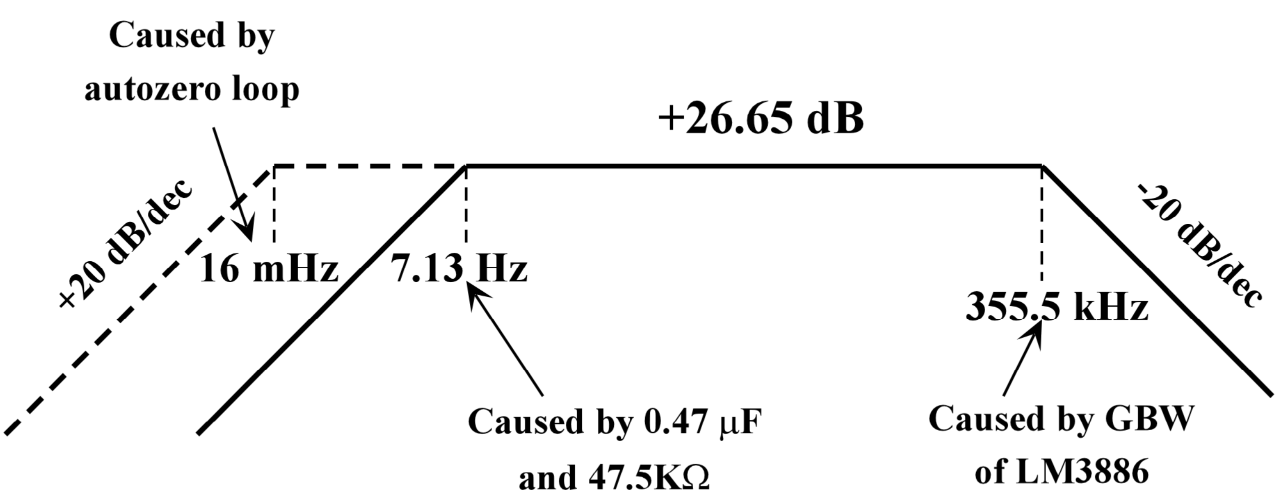
$$A_{VF} = \frac{V_{O1}}{V_{in}} = \frac{-\frac{R_F}{R_E}\times 1}{1+\frac{1}{SC_C R_{C1}} \times \frac{R_{C3}}{R_{C2}+R_{C3}} \times \left(1+\frac{R_F}{R_E}\right)}$$

$$A_{VF} = \frac{V_{O1}}{V_{in}} = -\frac{R_F}{R_E} \times \frac{SC_C R_{C1}}{SC_C R_{C1} + \left(1+\frac{R_F}{R_E}\right)\times\left(\frac{R_{C3}}{R_{C2}+R_{C3}}\right)}$$

The resulting TF shows a first-order response whose break frequency is (in r/s) given by the root of the denominator, that is

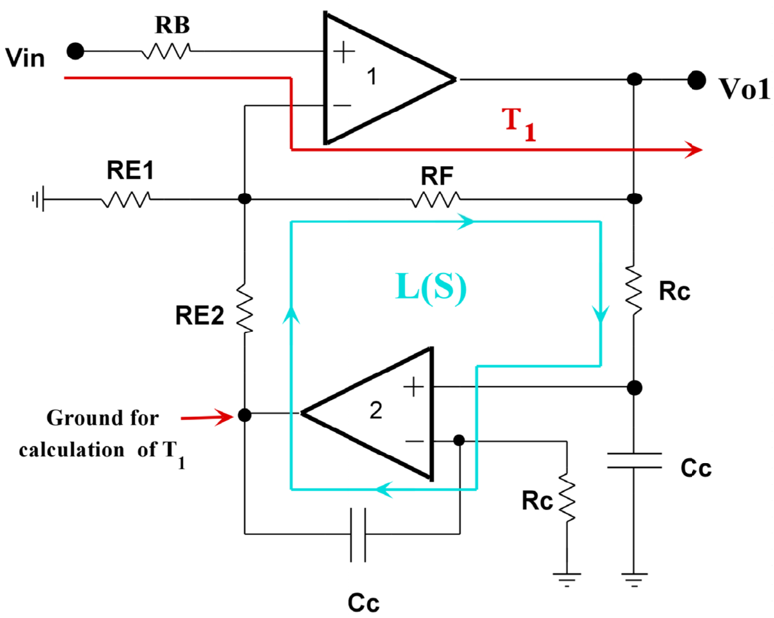
$$S_{den} = -\frac{\left(1+\frac{R_F}{R_E}\right)\times\left(\frac{R_{C3}}{R_{C2}+R_{C3}}\right)}{C_C R_{C1}} = -\frac{\left(1+\frac{21.5k}{1k}\right)\times\left(\frac{1k}{215k+1k}\right)}{0.47\mu \times 2.21M} = -0.1 \quad \omega_C = 0.1\, r/s \quad or \quad F_C = 16\, mHz$$

$$F_{HI} = \beta_V \times GBW = \frac{R_E}{R_E+R_F}\times GBW = \frac{1k}{1k+21.5k}\times 8M = 355.5\, kHz$$



Inverting Amplifier Gain Response

TRANSFER FUNCTION OF NON-INVERTING AMPLIFIER WITH AUTOZERO LOOP



$$\frac{V_{o1}}{V_{in}} = \frac{\sum T_k N_k}{1-\sum B_1 + \sum B_2 - \sum B_3 + \ldots} = \frac{T_1 N_1}{1-B_1}$$

$$T_1 = c \qquad N_1 = 1$$

$$L(S) = \frac{1}{1+SC_C R_C} \times \left(1+\frac{1}{SC_C R_C}\right) \times \left(-\frac{R_F}{R_{E2}}\right)$$

$$A_{VF} = \frac{V_{O1}}{V_{in}} = \frac{\left(1+\frac{R_F}{R_{E1}\|R_{E2}}\right) SC_C R_C}{SC_C R_C + \frac{R_F}{R_{E2}}}$$

$$S_{den} = -\frac{\left(\frac{R_F}{R_{E2}}\right)}{C_C R_C} = -\frac{\left(\frac{20.5k}{205k}\right)}{0.47\mu \times 2.21M} = -0.0963 \quad \omega_C = 0.0963\ r/s \quad or \quad F_C = 15.3\ mHz$$

The HF gain is (past F_C) $A_{VF} = \frac{V_{O1}}{V_{in}} = \left(1+\frac{R_F}{R_{E1}\|R_{E2}}\right) = 1 + \frac{20.5}{1k\|205k} = 21.6V/V$ which is off from the inverting gain that was –21.5V/V and would create a non-zero average voltage across the load. If V_o max = 24V_P for the inverting amp, the non- inverting amp will output 24V_P*21.6/21.5 = 24.111V_P, therefore the average voltage will be

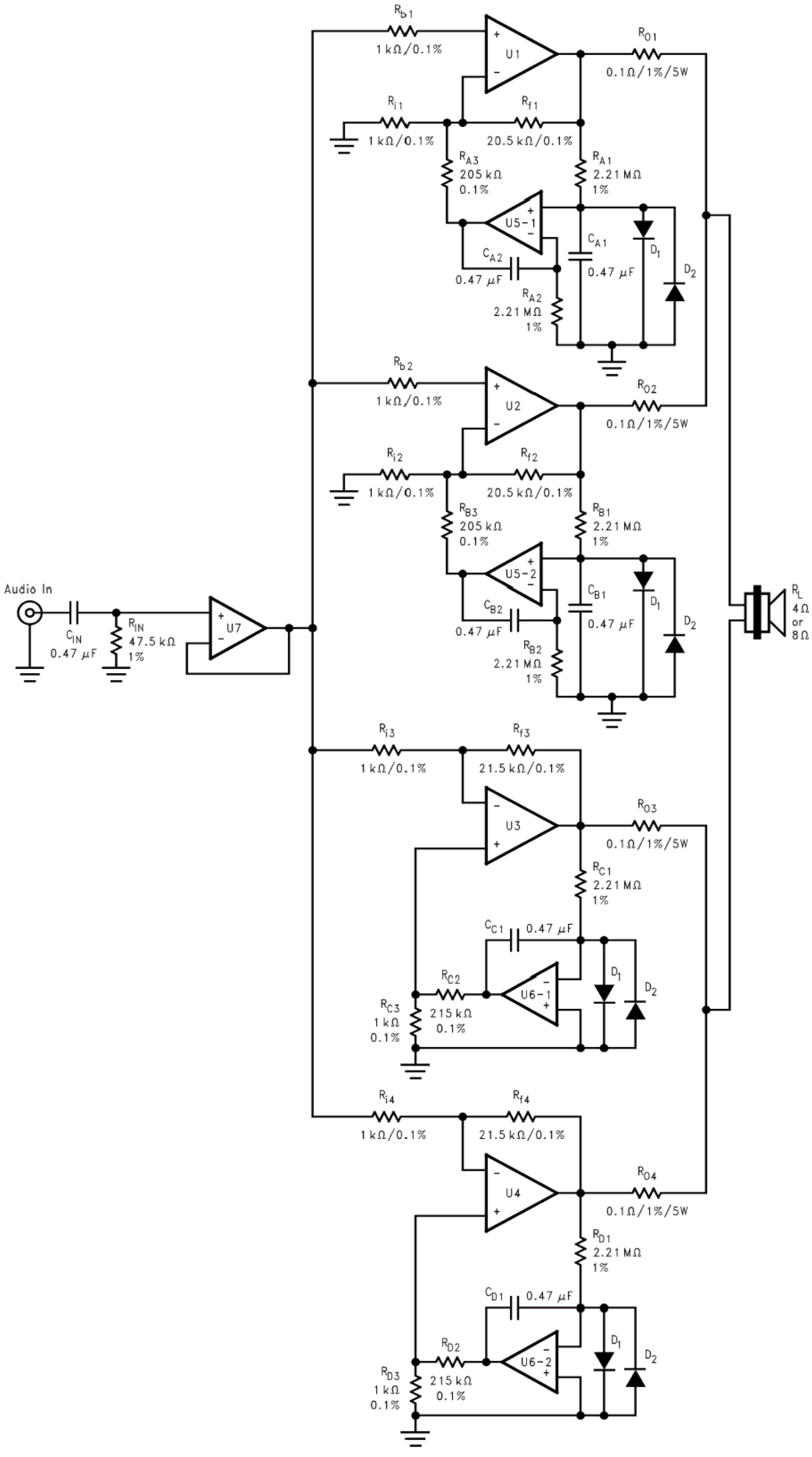
$$V_{avg} = \frac{24-24.111}{2} = 55.5mV \quad and \quad I_{avg} = \frac{55.5m}{4+0.1+1.1} = 13.2\ mA$$

Which is not significant.

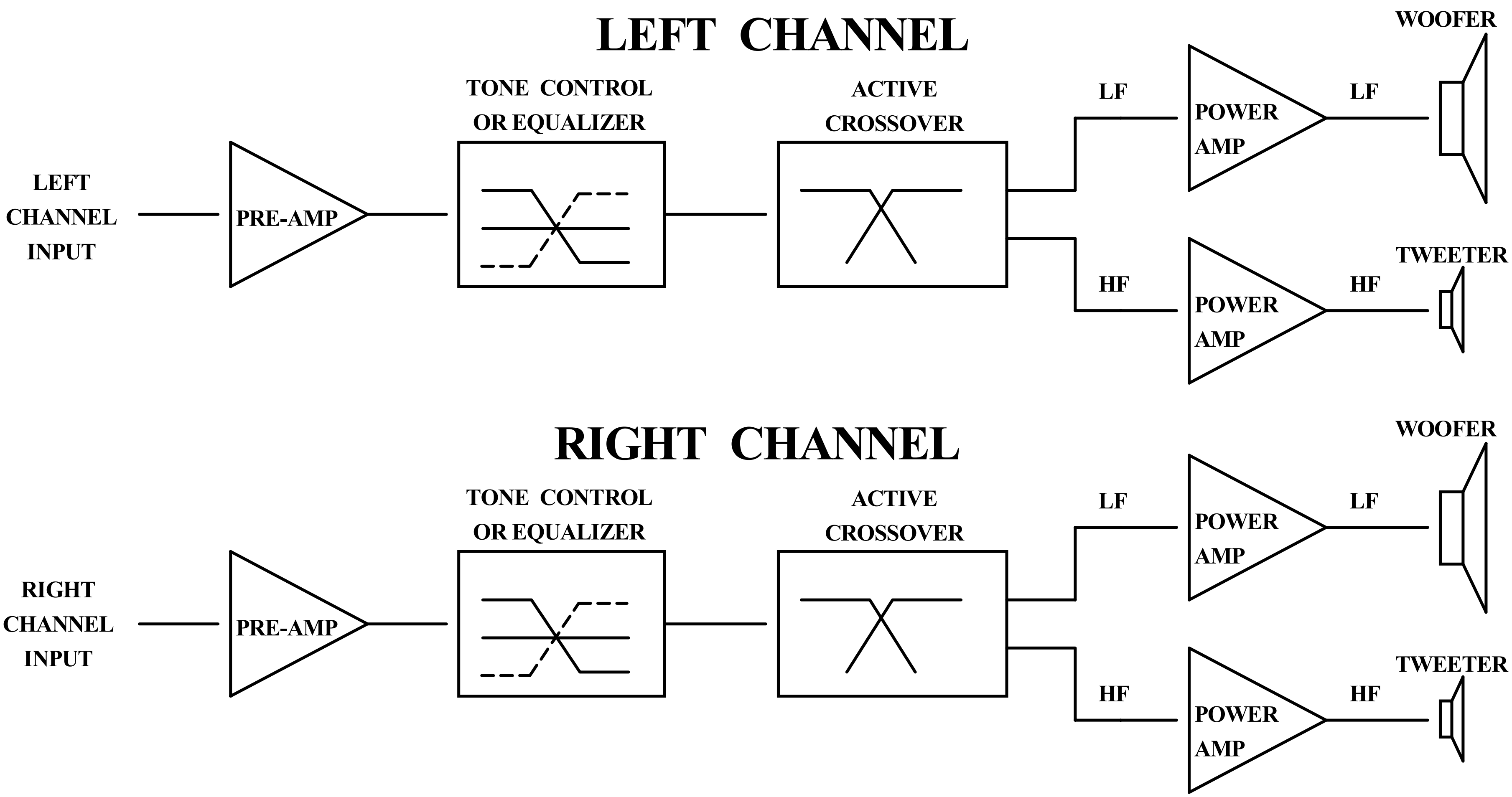
To match the gains of the inverting and non-inverting amps, the value of R_F should be changed to 20.4K in the non-inverting amp .

Another thing that should be matched is the cutoff frequencies of the DC autozero loops. As it stands now, they are very close but that could pose a problem for LF frequency signals or slow transient voltages that have to be amplified. The O/P's of the inverting and non-inverting amps will not respond at the same speed due to different time constants ($\tau_{loop} = 1/\omega_c$) of the loops and may result in large differences in the magnitudes of the O/P voltages.

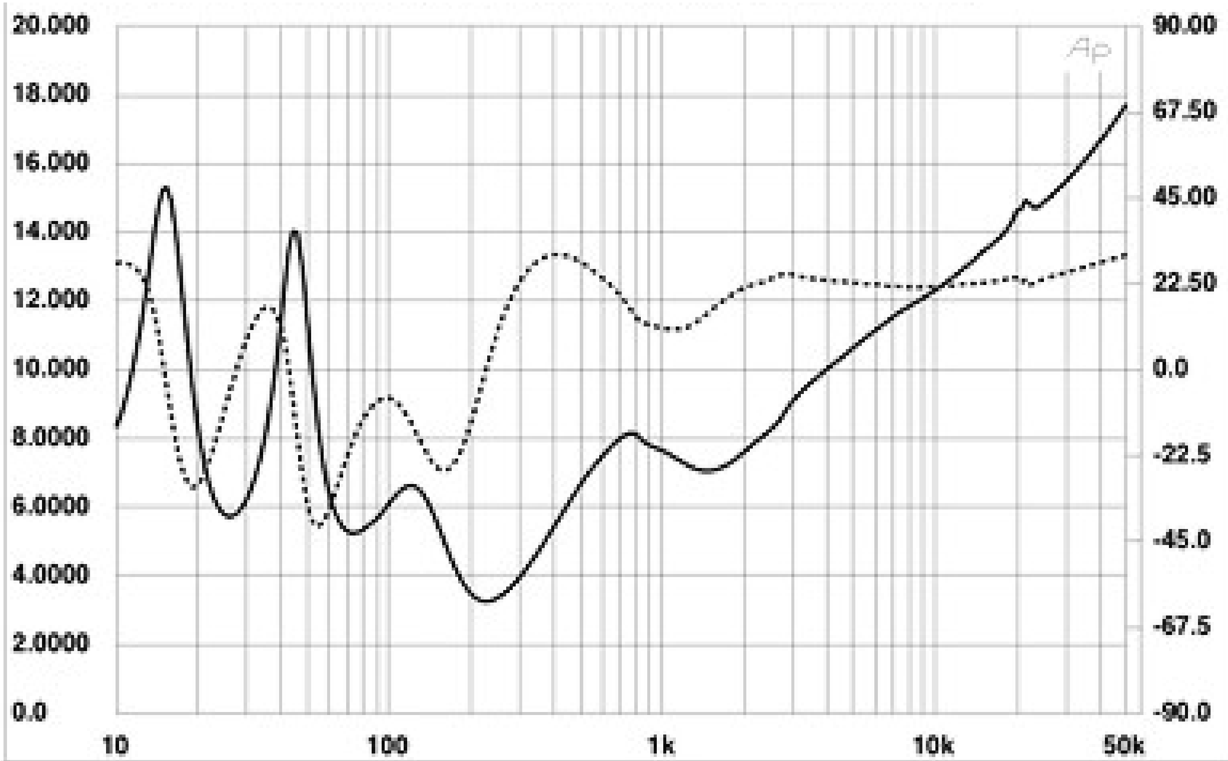
NOTE: The 7.13 Hz cutoff frequency would attenuate very slow transient inputs and as a result the DC autozero loops would not react very much to very slow transients. Therefore the imbalance in DC autozero loop time constants (or F_C) is not a big concern.



Parallel-Bridge Amplifier with DC Autozero Loop



AUDIO AMPLIFIER BLOCK DIAGRAM



Woofer Speaker Impedance (Magnitude is solid line, phase is dotted line)

The above graph shows clearly that speaker impedance – including enclosure effect – varies with frequency and shows several resonant points (dips) where the impedance is minimum, the worst of which is at about 200 Hz where it dips to about 3Ω /-55° where the power amplifier can be stressed more and will have to supply more current and may have to absorb some of the reactive power caused by the phaseshift. Let's say that the above response is not very good and reflects a poor speaker-enclosure combination design and could be improved and also corrected with active equalizer filters inserted after the pre-amps.