Flip-Flops

- A flip-flop is a type of circuit that contains two states, 0 or 1(on or off and are often used to store state information. By sending a signal to the flip-flop, the state can be changed.

- Flip-flops are used in a number of electronics, including computers and communications equipment. Flip-flop circuits are interconnected to form the logic gates for the digital integrated circuits (IC s) used in memory chips and microprocessors.

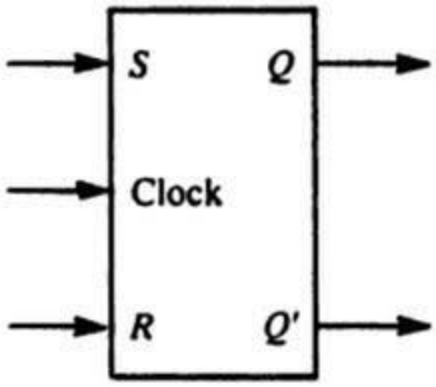
- There are several different kinds of flip-flop circuits, with designators such as T (toggle), S-R (set/reset), J-K and D (data).

- A flip-flop typically includes zero, one, or two input signals as well as a clock signal and an output signal. Some flip-flops also include a clear input signal to reset the current output.

SR Flip Flop

- SR flip-flop is one of the most common types of flip-flop. SR stands for Set Reset.

- Diagram shows the graphic symbol of SR flip-flop. The flip-flop has three inputs S (set), R, (reset) and C (clock)

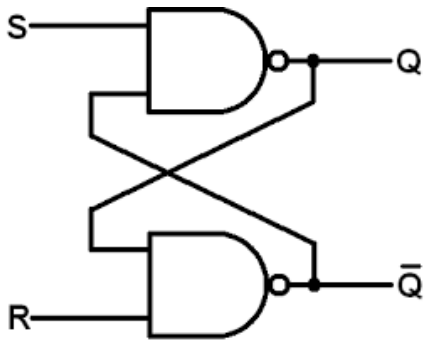


S	R	Q
0	0	No change
0	1	0
1	0	1
1	1	Indeterminate

Operation of SR flipflop

- If there is no signal at the clock input C, the output of the circuit cannot change the values of S and R.
- If S=1 and R=0 when C changes from 0 to 1, output Q is set to 1.
- If S=0 and R=1 when C changes from 0 to 1, output Q is cleared to 0.
- If both S and R are 0 during the clock transition, the output does not change.
- When both S and R are equal to 1, the output is unpredictable and may go to either 0 or 1.

Logic Diagram

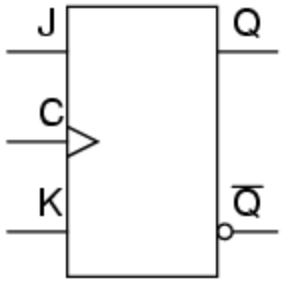


JK flip Flop

- The **JK Flip Flop** is the most widely used flip flop. It is considered to be a universal flip-flop circuit. The sequential operation of the JK Flip Flop is same as for the RS flip-flop with the same **SET** and **RESET** input.

- The JK Flip Flop name has been kept on the inventor name of the circuit known as **Jack Kilby.**

- The intermediate condition of SR flip-flop is defined in JK.



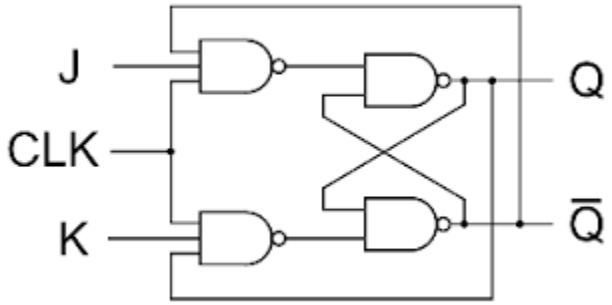
Truth Table

J	K	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	$\overline{Q}_0$ (toggles)

Operation of JK flipflop

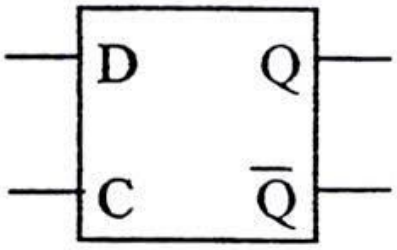
- The J input is equivalent to the S (set) input of SR flip-flop and K input is equivalent to R (clear) input.
- Instead of indeterminate condition, the JK flip-flop has a complement condition (toggle).

Logic Diagram



D Flip-flop

- The D-type flip-flop is constructed from a gated SR flip-flop with an inverter added between the S and the R inputs to allow for a single D (data) input.
- The **D Flip Flop** is by far the most important of the clocked flip-flops as it ensures that ensures that inputs S and R are never equal to one at the same time.



Input D	Circuit Action $Q_{(t-1)}$
0	0
1	1

Simply, for positive transition on clock signal,

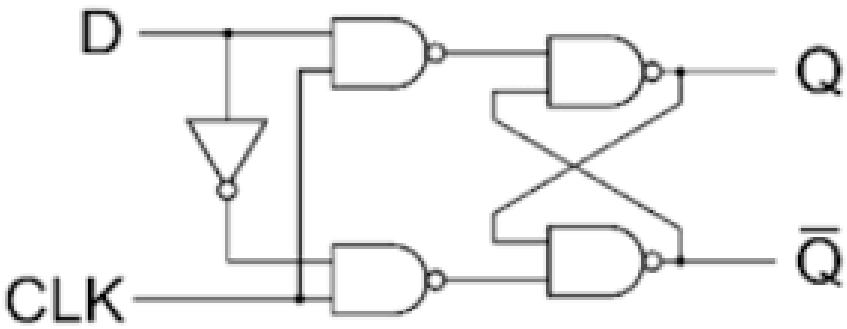
If D = 0 => Q = 0 so flip flop is reset.

If D = 1 => Q = 1 so flip flop is set.

Operation of D flip-flop

- If the clock signal is high (rising edge to be more precise) and if D input is high, then the output is also high and if D input is low, then the output will become low.

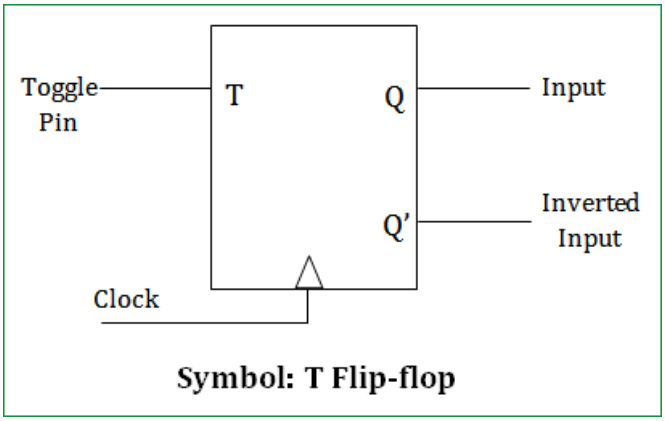
Logic Diagram



T flip – flop

- T flip – flop is also known as “Toggle Flip – flop”. Then the flip – flop acts as a Toggle switch.

- **T flip flop is modified form of** JK flip-flop making it to operate in toggling region. The T flip – flop is a single input device and hence by connecting J and K inputs together and giving them with single input called T. So a T flip – flop is sometimes called as single input JK flip – flop.



Symbol: T Flip-flop

T	Q	Action
0	Q	hold state
1	Q’	toggle state

Operation of T flip-flop

- When T=0 a clock transition does not change the state of the flip-flop.
- When T=1 a clock transition complements the state of flip-flop.

Logic Diagram