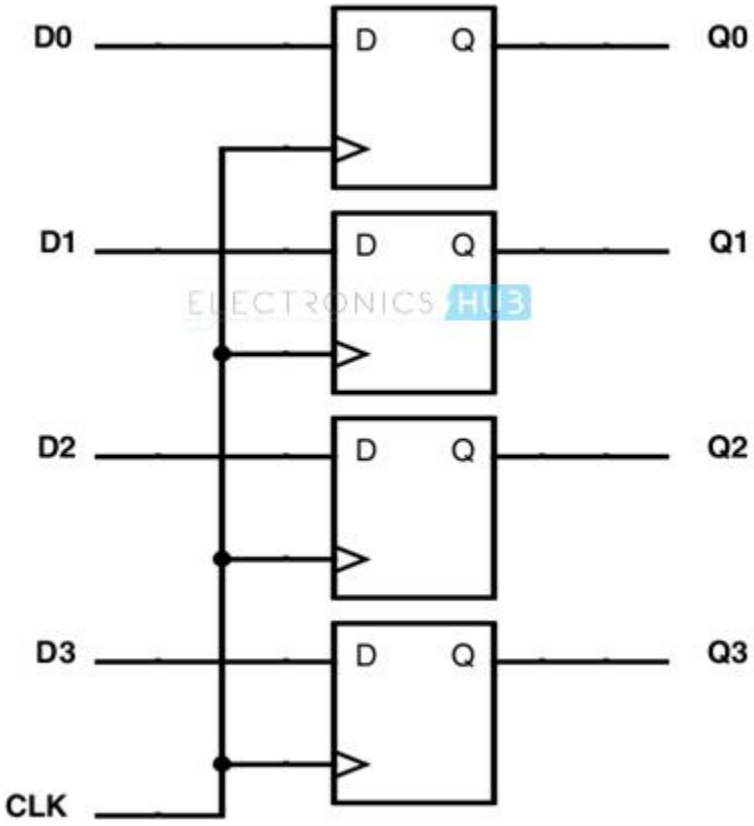
Registers

- Register is a group of flip-flop capable of storing one bit of information. The n-bit register will consist of n number of flip-flop and it is capable of storing an n-bit word.

- The binary data in a register can be moved within the register from one flip-flop to another. A register consists of a group of flip-flops and gates.

- Following diagram shows register constructed with four D flip-flop.



- The common clock input triggers all flip-flops on the rising edge of each pulse, and the binary data available at the four inputs are transferred into 4-bit register.

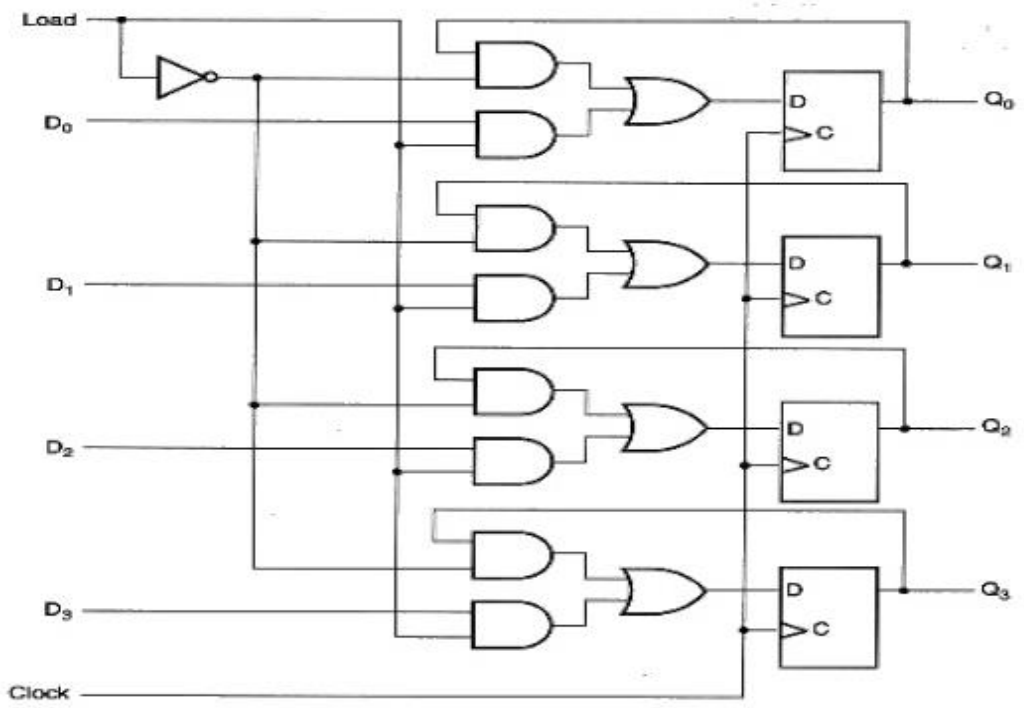
- The clear input is useful for clearing the register.

- **Register load-** The transfer of new information into a register is referred as loading.

Register with parallel load

- **If** all the bits of the register are loaded simultaneously with a common clock pulse transition, is called loading is done in parallel.

- A 4 bit register with a load control input that is directed through gates and into the D input is shown in diagram.



- **The C input** receives clock pulses at all times. **The load input** determines the action to be taken with each clock pulse.

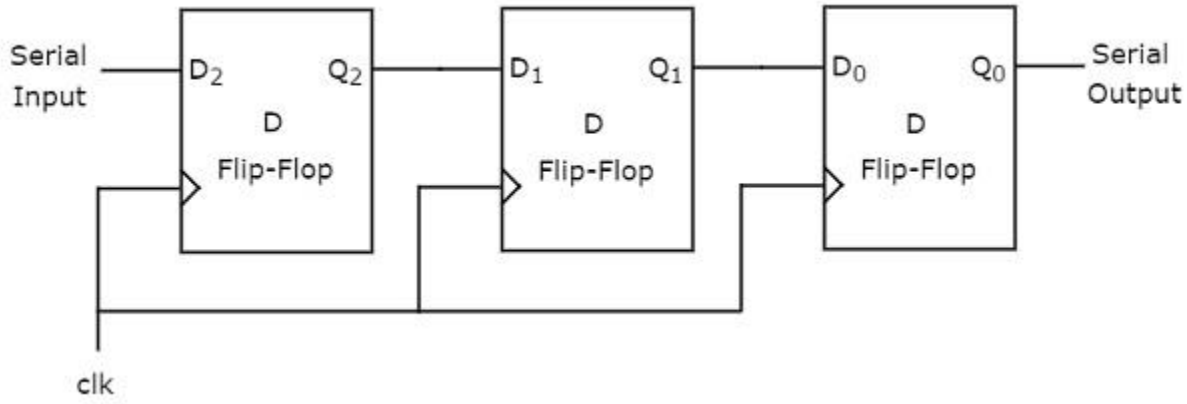
- When load input is 1, the data in the four inputs are transferred into the register. When load input is 0, the data inputs are inhibited and the D inputs of the flip-flops are connected to their outputs.

- The feedback connection from output to input is necessary because the D flip-flop does not have “no change” condition. With each clock pulse, the D input determines the next state of the output.

Shift Registers

- Shift Registers are **sequential logic circuits**, capable of storage and transfer of data. The shift register is capable of shifting bits either towards right hand side or towards left hand side.

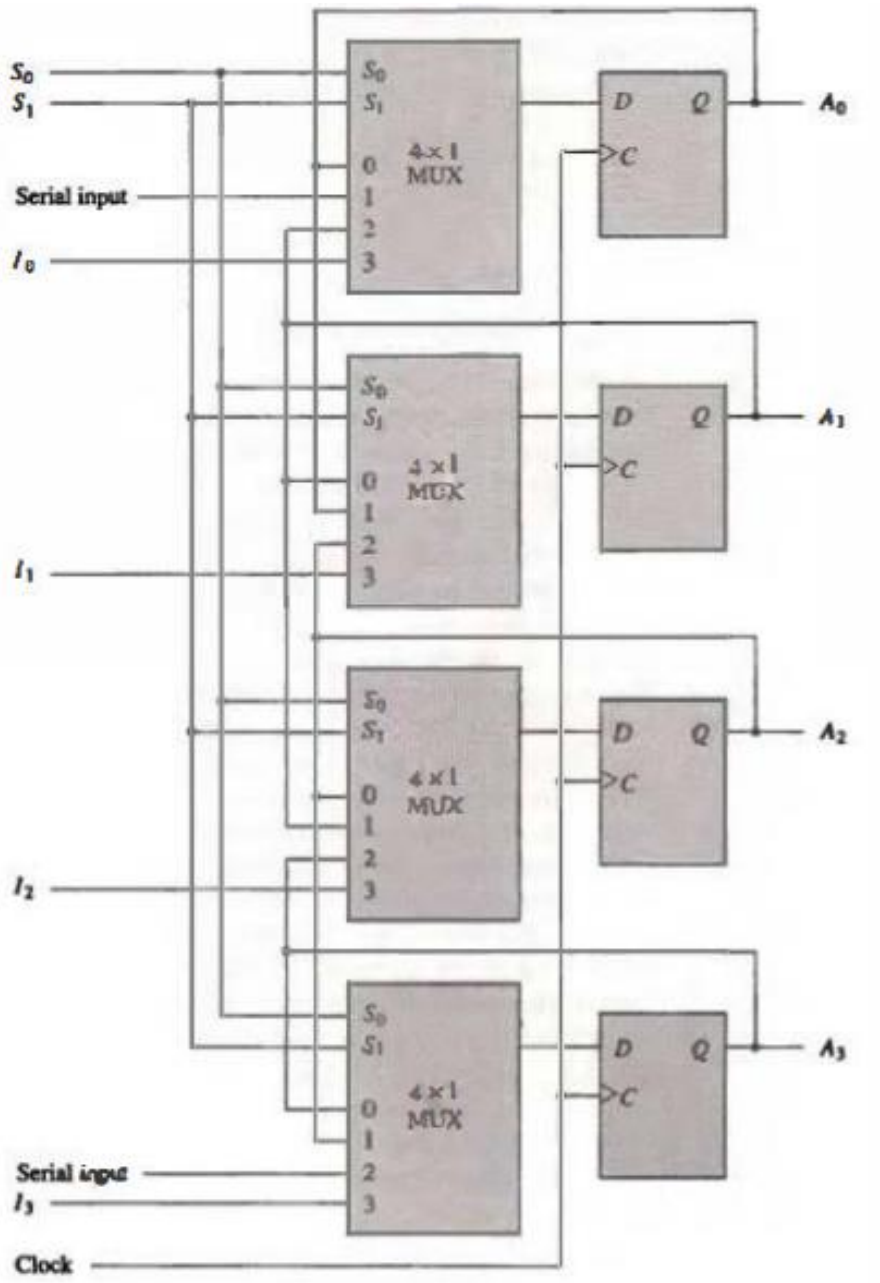
- They are made up of Flip Flops which are connected in such a way that the output of one flip flop could serve as the input of the other flip-flop, depending on the type of shift registers being created.



- The output of a given flip-flop is connected to the D input of the flip-flop at its right. The clock is common to all flip-flops.
- The serial input determines what goes into leftmost position during shift. The serial output determines what is taken from the rightmost flip-flop.

Bidirectional Shift Registers with parallel load

- Bidirectional shift register shift in both directions.
- Following are the four types of shift registers based on applying inputs and accessing of outputs.
  - Serial In - Serial Out shift register
  - Serial In - Parallel Out shift register
  - Parallel In - Serial Out shift register
  - Parallel In - Parallel Out shift register



- The two selection inputs S_1 and S_0 select one of the multiplexer data inputs for the D flip-flop.
- The selection lines control the mode of operation of the register shown in table below

Function Table for the Register

Mode Control		
s_1	s_0	Register Operation
0	0	No change
0	1	Shift right
1	0	Shift left
1	1	Parallel load

- When the mode control **s_1s_0=00**, data input 0 of each multiplexer is selected. **This condition forms a path from the output of each flip-flop into the input of the same flip-flop.**
- When **s_1s_0=01,** the terminal marked 1 in each multiplexer has a path to D input of corresponding flip-flop. This causes **shift right(down)** operation, **with the serial input data transferred into A_0 and content of each flip-flop A_{i-1} transferred to Ai for i=1,2,3.**
- When **s_1s_0=10, shift left(up)** operation results, **with the serial input data going into A_3 and content of each flip-flop A_{i+1} transferred to Ai for i= 0,1,2.**
- When **s_1s_0=11, the binary information from each input I0 to I3 is transferred into corresponding flip-flop.**

Binary Counter

What is a Counter?

- In a digital logic system or computers, **counter can count and store the number of time any particular event or process have occurred, depending on a clock signal.**
- A binary counter is a hardware circuit that is made out of a series of flip-flops. The output of one flip-flop is sent to the input of the next flip-flop in the series.
- A binary counter can be constructed from J-K flip-flops by taking the output of one cell to the clock input of the next.
- There are **two types of counters**

1. **Asynchronous counters**
2. **Synchronous counters**

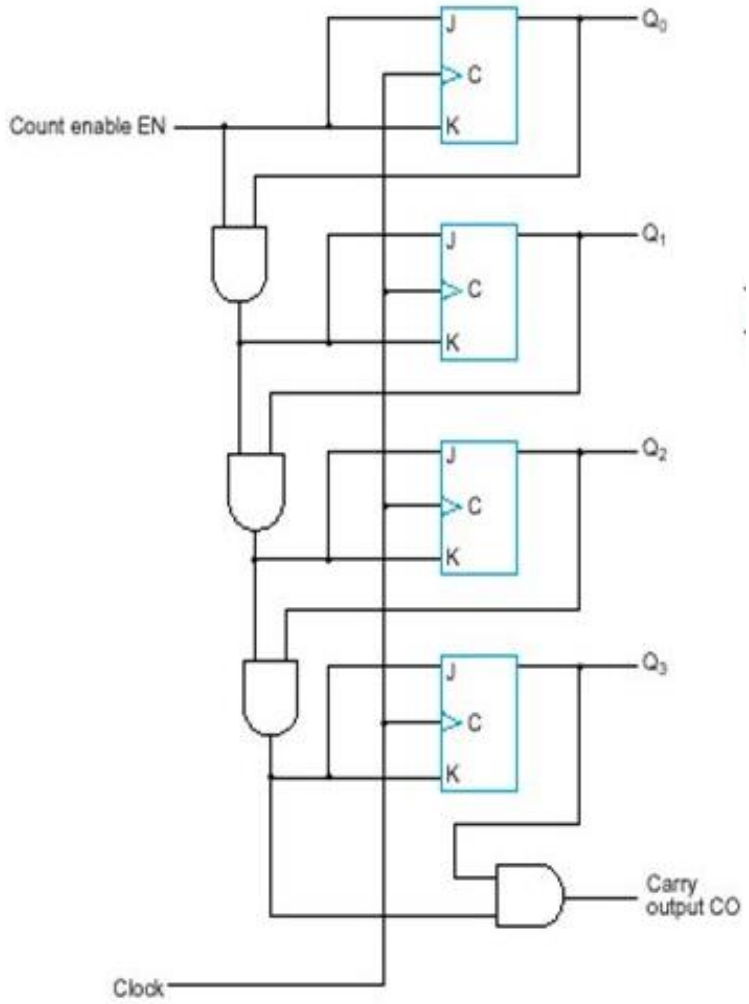
1. Asynchronous Counters

- If the flip-flops do not receive the same clock signal, then that counter is called as Asynchronous counter.
- The output of system clock is applied as clock signal only to first flip-flop. The remaining flip-flops receive the clock signal from output of its previous stage flip-flop. Hence, the outputs of all flip-flops do not change affect at the same time.
- **Disadvantage:** When counting a large number of bits, due to the chain system, **propagation delay** by successive stages became too large which is very difficult to get rid off. In such a situation, Synchronous counters are faster and reliable. There are

also **counting errors** in Asynchronous Counter when high clock frequencies are applied across it.

2. Synchronous Counter

- The counters which use clock signal to change their transition are called “Synchronous counters”. This means the synchronous counters depends on their clock input to change state values.
- The external clock signal is connected to the clock input of EVERY individual flip-flop within the counter so that all of the flip-flops are clocked together simultaneously (in parallel) at the same time giving a fixed time relationship. In other words, changes in the output occur in “synchronization” with the clock signal.
- The result of this synchronization is that all the individual output bits changing state at exactly the same time in response to the common clock signal with no ripple effect and therefore, no propagation delay.
- In synchronous counters, all flip flops are connected to the same clock signal and all flip flops will trigger at the same time.

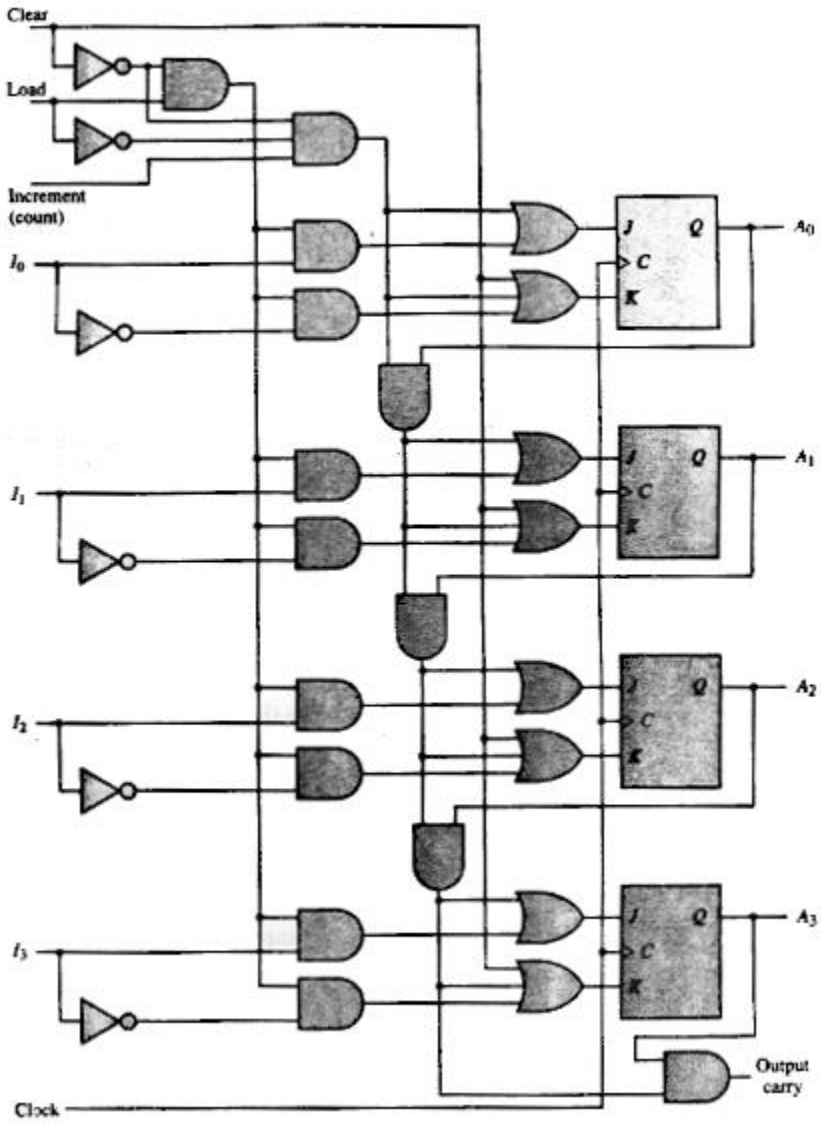


(a) Logic diagram

- J and K inputs of flip-flops are driven from separate AND gates which are also supplied with signals from the input and output of the previous stage. These additional AND gates generate the required logic for the JK inputs of the next stage.
- The C inputs of all flip-flops receive a common task.
- If count enable is 0, all J and k inputs are maintained at 0 and the output of counter does not change.
- The first stage A0 is complemented when counter is enabled.

- Each of the other flip-flops are complemented when all previous least significant flip-flops are equal to 1.

Binary Counter with parallel load



Clock	Clear	Load	Increment	Operation
↑	0	0	0	No change
↑	0	0	1	Increament count by 1
↑	0	1	×	Load inputs I_0through I_3
↑	1	×	×	Clear outputs to 0