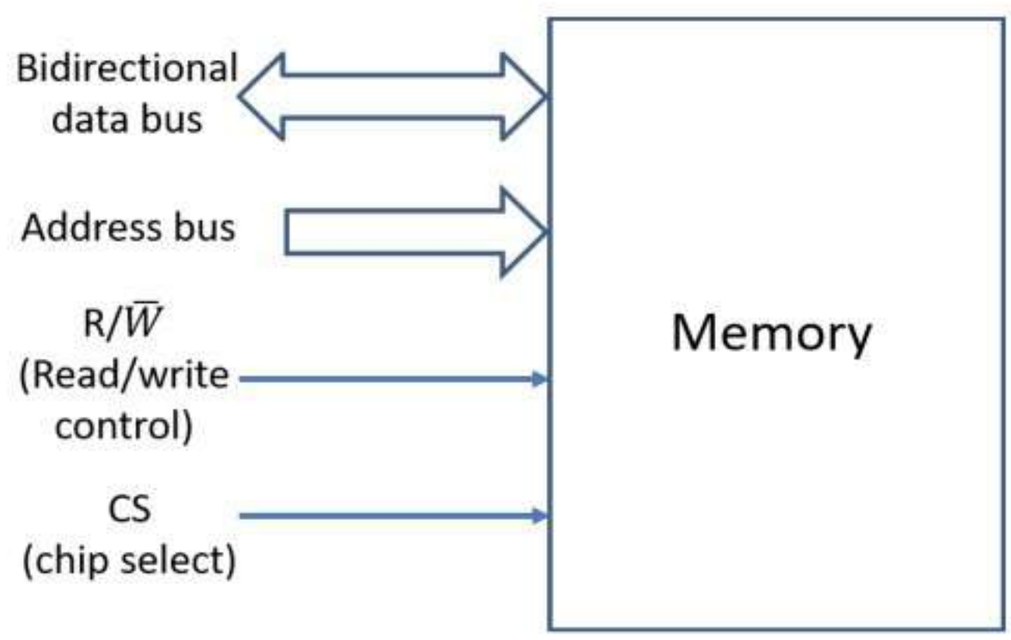
Memory organization and operation

- The number of inputs required to store the data into or read the data from any memory location is N.
- One set of N lines is required for storing the data into the memory, referred to as data inputs and another set of N lines is required for reading the data already stored in the memory, which is referred to as data outputs.
- The concept of bus is used to refer to a group of conductors carrying related set of signals.
- Therefore, the set of lines meant for data inputs is input data bus and for data outputs is output data bus.
- Input and output data buses are unidirectional, i.e. the data can flow in one direction only.
- In most of the memory chips available, the same set of lines is used for data input as well as data output and is referred to as bidirectional bus.
- This means that the data bus is time multiplexed.
- It is used as input bus for some specific time and as output bus for some other time depending upon a Read/Write control input as shown in figure.



- A number of control inputs are required to give commands to the device to perform the desired operation.
- For example, a command signal is required to tell the memory whether a read or a write (R/$\overline{W}$ in figure) operation is desired.
- When R/$\overline{W}$ is HIGH, the data bus will be used for reading the memory (output bus) whereas when R/$\overline{W}$ is LOW, the bus will be acting in the input direction and the data on the bus will go into the memory.
- Other command includes inputs chip enable (CE), chip select (CS), etc.
- There are mainly two types of operations performed by memory unit.

1. Write operation
   - The chip select signal is applied to the CS terminal.
   - The word to be stored is applied to the data-input terminal.
   - The address of the desired memory location is applied to the address-input terminals.
   - A write command signal is applied to the write control input terminal with R/$\overline{W}$ = 0.
2. Read operation
   - The chip select signal is applied to the CS terminal.
   - The address of the desired memory location is applied to the address-input terminals.
   - A read command signal is applied to the read control input terminal with R/$\overline{W}$ = 1.

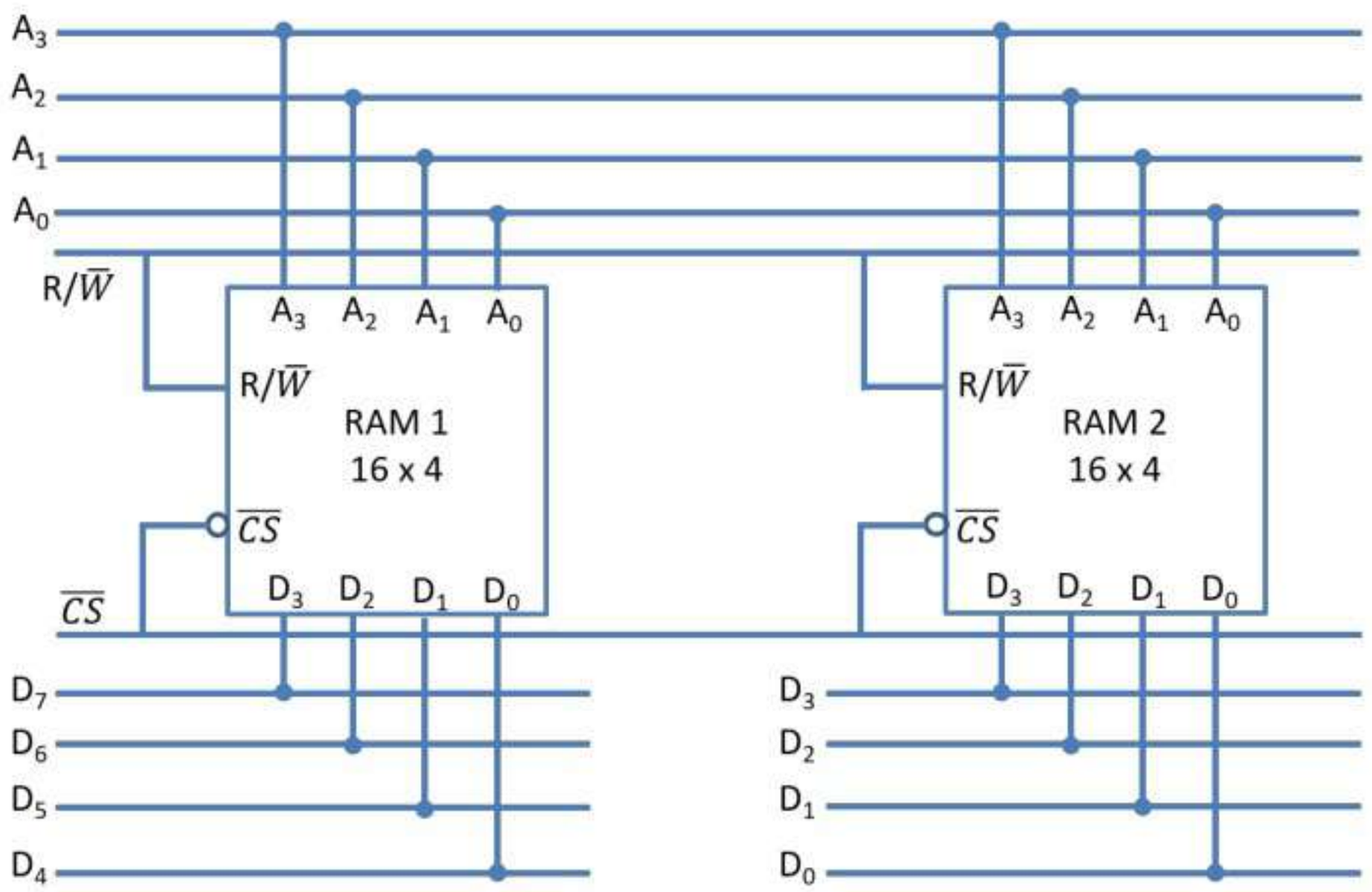
Memory expansion

- In many applications, the required memory capacity, i.e. the number of words and/or word size, can not be satisfied by a single available memory IC chips.
- Therefore, several chips have to be combined suitably to provide the desired number of words and/or word size.

Expanding word size

- If it is required to have a memory of word size n and the word size of the available memory ICs is N (n > N), then a number of similar ICs can be combined together to achieve the desired word size.
- The number of IC chips required is an integer, next higher to the value n/N.
- These chips are to be connected in the following way:
  1. Connect the corresponding address lines of each chip individually, i.e. A_0 of each chip is connected together and it becomes A_0 of the overall memory. Similarly, connect other address lines together.
  2. Connect the RD input of each IC together and it becomes the read input for the overall memory. Similarly, connect the WR and CS inputs.

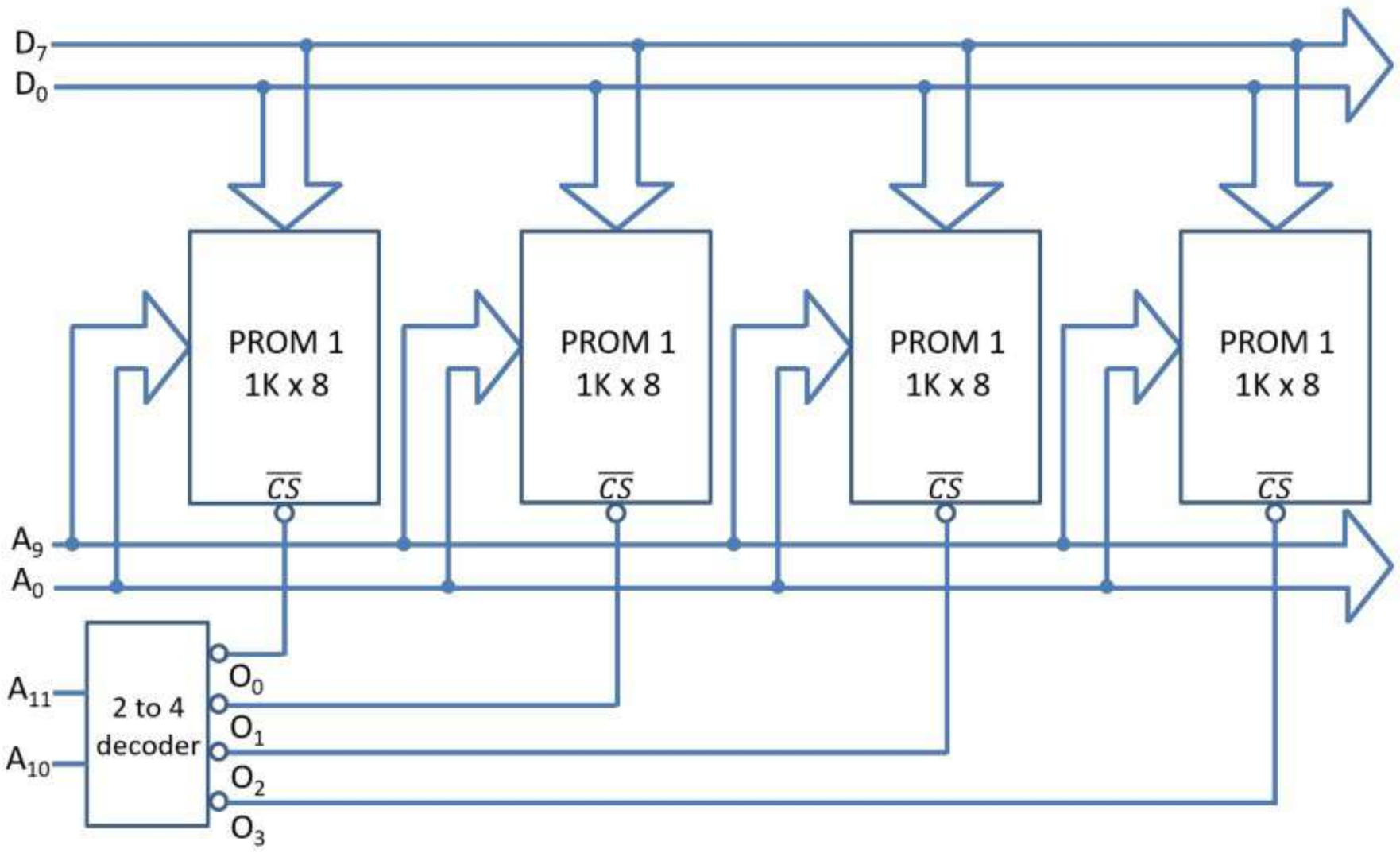
Example: Show how to combine several 16 x 4 RAM to form a 16 x 8 RAM.
Solution: n = 8 and N = 4, so we require n/N = 2 chips to obtain desired memory.



Expanding word capacity

- To obtain a memory of capacity m words, using the memory chips with M words each, the number of chips required is an integer next higher to the value m/M.
- These chips are to be connected in the following way:
  1. Connect the corresponding address lines of each chip individually.
  2. Connect the RD input of each chip together. Similarly, connect the WR inputs.
  3. Use a decoder of proper size and connect each of its outputs to one of the CS terminals of memory chips.

Example: Show how to combine several 1K x 8 PROMs to produce 4K x 8 PROM.
Solution: 1K x 8 PROM has 10 number of address lines because 2^{10} = 1024 (1K).
We need total 4 number of 1K x 8 PROM chips to make one 4K x 8 PROM chip.



A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	1	1	1	1	1	1	1	1

Memory chip	Starting address	Ending address
PROM 1	000 H	3FF H
PROM 2	400 H	7FF H
PROM 3	800 H	BFF H
PROM 4	C00 H	FFF H

Read only memory (ROM)

- A read-only memory (ROM) is a semiconductor memory device used to store information which is permanent in nature.
- It has become an important part of many digital systems because of its low cost, high speed, system-design flexibility and data non-volatility.
- The read-only memory has a variety of applications in digital systems, such as implementation of combinational logic and sequential logic, character generation, look-up table, microprocessor program storage, etc.
- ROMS are well-suited for LSI manufacturing processes and are available in many forms.
- Two major semiconductor technologies are used for the manufacturing of ROM integrated circuits, viz. bipolar technology and MOS technology, which differ primarily in access time.

- In general, bipolar devices are faster and have higher drive capability, whereas MOS devices require less silicon area and consume less power.
- With improvements in MOS technology, it is now possible to make MOS memories with speeds comparable to those of bipolar memories.
- The process of entering information into a ROM is referred to as programming the ROM.
- Depending on the programming process employed, the ROMS are categorized as:

1. *Mask programmable read-only memories*, which are referred to as ROMS. In these memories, the data pattern must be programmed as part of the fabrication process. Once programmed, the data pattern can never be changed. These are highly suited for very high-volume usage due to their low cost.

2. *Programmable read-only memories*, which are referred to as PROMs. A PROM is electrically programmable, i.e. the data pattern is defined after final packaging rather than when the device is fabricated. The programming is done with an equipment referred to as PROM programmer. The programming techniques used will be discussed later.

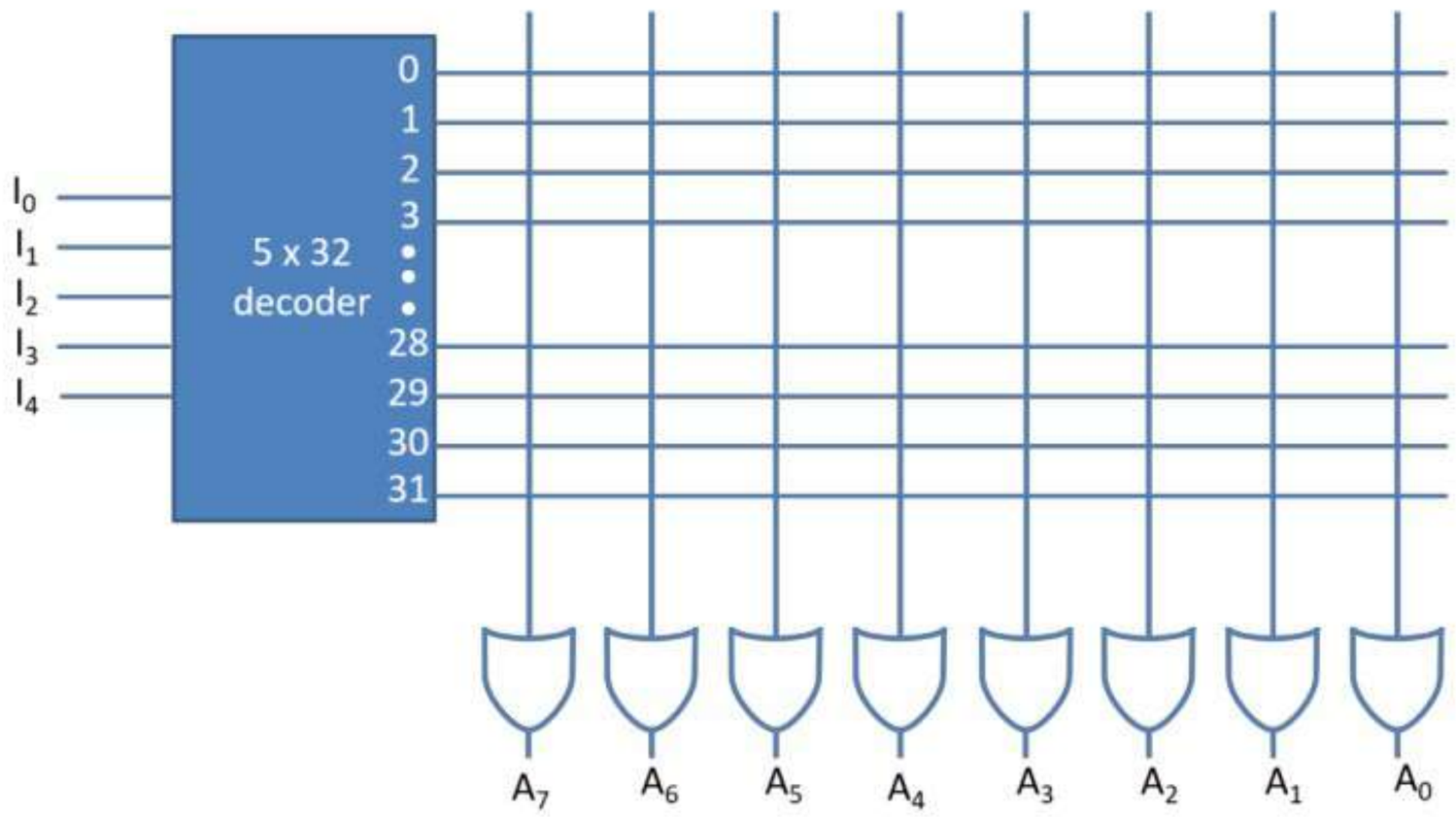
3. *Erasable programmable read-only memories*, which are referred to as EPROMs. As the name suggests, in these memories, data can be written any number of times, i.e. they are reprogrammable. Reprogrammable ROMs are possible only in MOS technology. For erasing the contents of the memory, one of the following two methods are employed:
   (a) Exposing the chip to ultraviolet radiation for about 30 minutes.
   (b) Erasing electrically by applying voltage of proper polarity and amplitude. Electrically erasable PROM is also referred to as EIPROM or EAROM (Electrically alterable ROM).

ROM as PLD

ROM organization

- k inputs – provide address for the memory
- n outputs – data bits of the stored word selected by address
- k address input lines specify 2^k words
- ROM does not have data inputs because it does not have write operation.
- Consider, for example, a 32 x 8 ROM.
- The unit consists of 32 words of 8 bits each.
- There are five input lines that form the binary numbers from 0 through 31 for the address.
- The five inputs are decoded into 32 distinct outputs by means of a 5 x 32 decoder.
- Each output of the decoder represents a memory address.
- The 32 outputs of the decoder are connected to each of the 8 OR gates.
- Each OR gate must be considered as having 32 inputs.
- Since each OR gate has 32 input connections and there are 8 OR gates, the ROM contains 32 x 8 = 256 internal connections.
- In general, a 2^k x n ROM will have an internal k x 2^k decoder and n OR gates.
- Each OR gate has 2^k inputs, which are connected to each of the outputs of the decoder.

Internal logic of 32 x 8 ROM



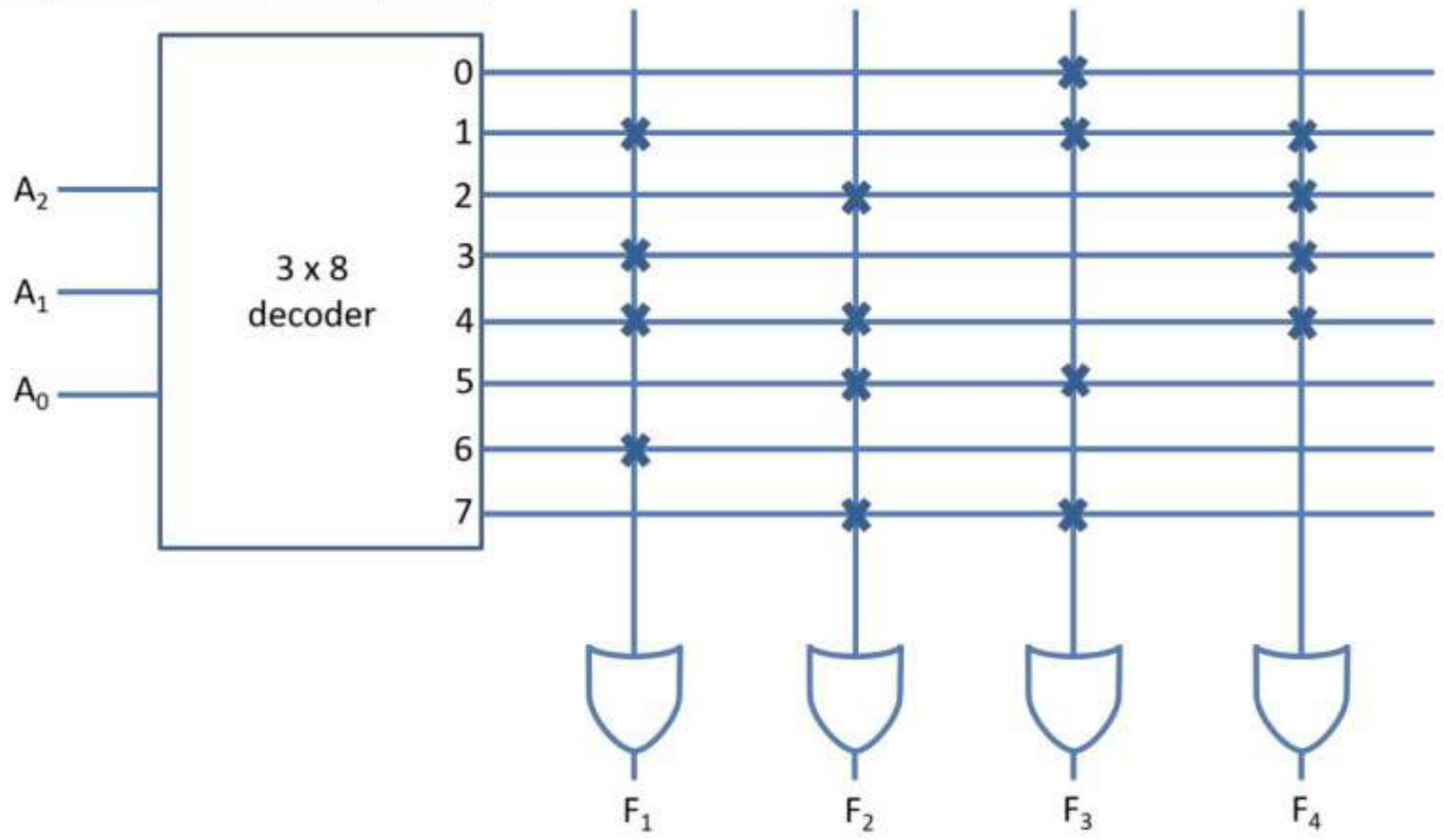
Example: Implement following functions using ROM.

$F_1 = \sum_m(1,3,4,6)$ $F_2 = \sum_m(2,4,5,7)$

$F_3 = \sum_m(0,1,5,7)$ $F_4 = \sum_m(1,2,3,4)$

Solution: First we have to decide that which decoder has been used to implement given example. We have 3 variable functions, so 3-to-8 decoder will be used.

A_2	A_1	A_0	F_1	F_2	F_3	F_4
0	0	0	0	0	1	0
0	0	1	1	0	1	1
0	1	0	0	1	0	1
0	1	1	1	0	0	1
1	0	0	1	1	0	1
1	0	1	0	1	1	0
1	1	0	1	0	0	0
1	1	1	0	1	1	0



Random access memory (RAM)

- Many digital systems require memories in which it should be possible to write into, or read from, any memory location with the same speed.
- In such memories, the data stored at any location can be changed during the operation of the system.
- This type of memory is known as a read/write memory and is usually referred to as RAM (random-access memory).
- The read-write memories (RWM)/random-access memories (RAM) are fabricated using bipolar devices or unipolar (MOS) devices.
- There are two types of RAMs. These are static RAM (SRAM) and dynamic RAM (DRAM).
- Bipolar RAMs are static, whereas the MOS RAMs can be static or dynamic.
- The basic storage cell of a static RAM is a bistable circuit, i.e., a latch, which simply consists of two cross-coupled inverters.
- A RAM is an array of these storage cells requiring as many FLIP-FLOPs as the bit storage capacity of the RAM, which is usually a large number.
- The storage cell of a DRAM is simply a capacitor, therefore, only MOS devices can be used for dynamic random-access memories.
- Since capacitors leak charge, therefore, the voltage stored in it gets reduced with time which requires periodic refreshing.
- In general, bipolar RAMs are faster than the MOS RAMs.
- With improvements in the MOS technology, it has become possible to make MOS RAMS with speeds (access time) comparable to those of bipolar RAMs.

Static RAM v/s Dynamic RAM

Static RAM	Dynamic RAM
1. SRAM has lower access time, so it is faster compared to DRAM.	1. DRAM has higher access time, so it is slower than SRAM.
2. SRAM is costlier than DRAM.	2. DRAM costs less compared to SRAM.
3. SRAM requires constant power supply, which means this type of memory consumes more power.	3. DRAM offers reduced power consumption, due to the fact that the information is stored in the capacitor.
4. Due to complex internal circuitry, less storage capacity is available compared to the same physical size of DRAM memory chip.	4. Due to the small internal circuitry in the one-bit memory cell of DRAM, the large storage capacity is available.
5. SRAM has low packaging density.	5. DRAM has high packaging density.
6. No need to refresh periodically.	6. Due to capacitor used as storage element, information may lose over period of time. So, need to refresh periodically.
7. Uses an array of 6 transistors for each memory cell.	7. Uses a single transistor and capacitor for each memory cell.

RAM v/s ROM

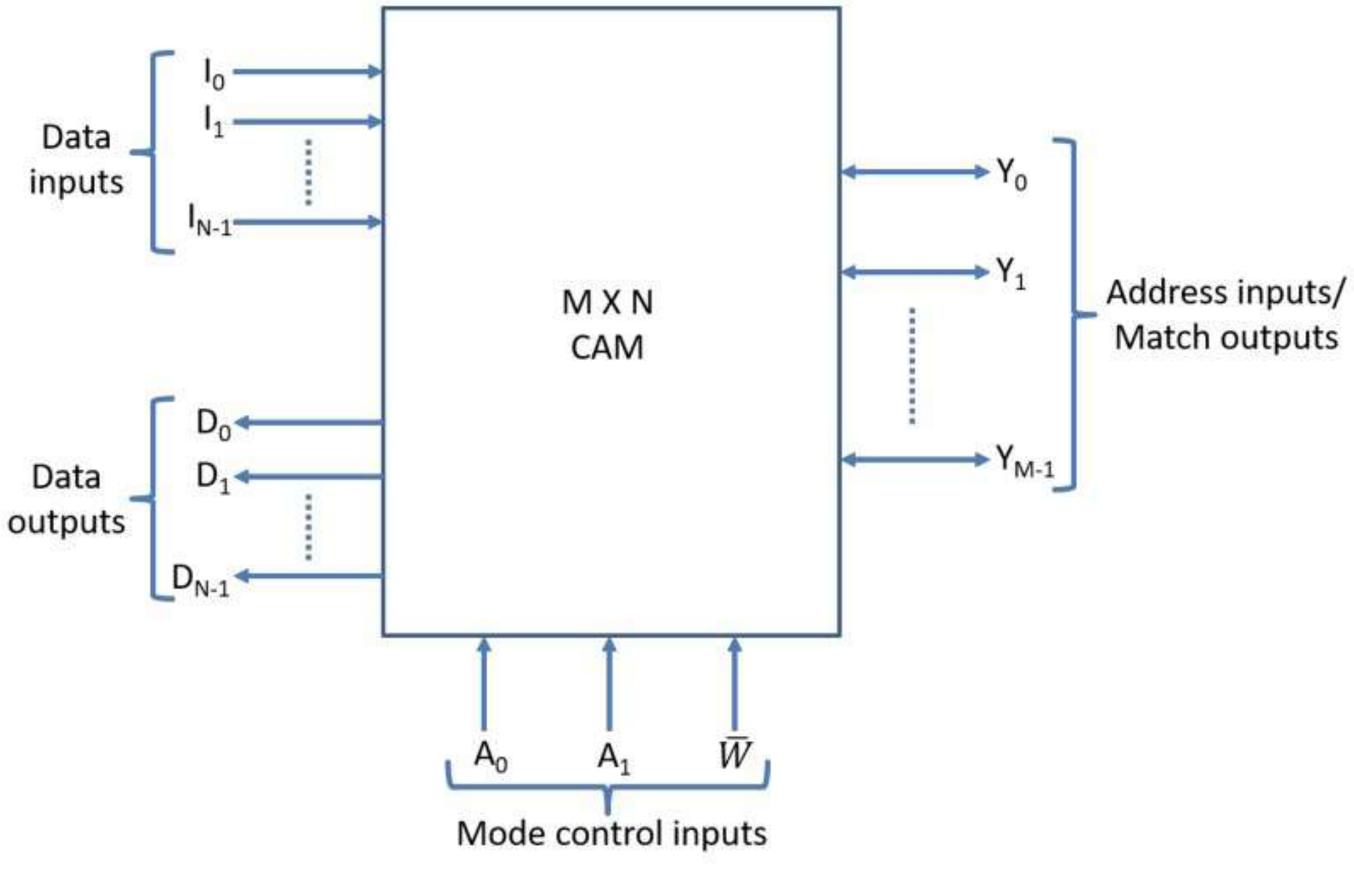
Parameter	RAM	ROM
Data	The data is not permanent but it can be altered any number of times.	The data is permanent. It can be altered but only a limited number of times that too at slow speed.
Speed	It is a high-speed memory.	It is much slower than the RAM.
CPU Interaction	The CPU can access the data stored on it.	The CPU cannot access the data stored on it. In order to do so, the data is first copied to the RAM.
Size and Capacity	Large size with higher capacity.	Small size with less capacity.
Usage	Primary memory (DRAM DIMM modules), CPU Cache (SRAM).	Firmware like BIOS or UEFI. RFID tags, microcontrollers, medical devices, and at places where a small and permanent memory solution is required.
Cost	It doesn't come cheap.	Way cheaper than RAM.

Content addressable memory (CAM)

- The content addressable memory (CAM) is a special purpose random access memory device that can be accessed by searching for data content.
- For this purpose, it is addressed by associating the input data, referred to as key, simultaneously with all the stored words and produces output signals to indicate the match conditions between the key and the stored words.
- This operation is referred to as association or interrogation and this type of memory is also known as associative memory.
- After identifying the locations whose contents match the key, read or write operations can be performed to these locations.
- The key to be used may either consist of the entire data word or only some specific bits of the data word, i.e. the other bits can be masked.
- A CAM differs from the conventional memory organization in that the addressing of a location in the latter has no relation to the memory content.
- A CAM has the ability to search out or interrogate stored data on the basis of its contents and, therefore, can be a powerful asset in many applications.
- For example, consider a list containing the names of persons, their ages, professions, and nationalities stored in a CAM.
- If one is interested in finding out engineers in the list, the CAM is able to check every memory location simultaneously by using the coded form for engineer as the key.
- On the other hand, if it is required to find the engineers of Indian nationality, the key will consist of the combination of the codes corresponding to engineer and Indian nationality.
- All the memory locations with engineers of Indian nationality will be identified and the remaining data (name and age) can then be retrieved by using the read operation.
- To do the same search process with a conventional memory, each memory word is to be read out and compared with the key.
- This search is a serial process and hence time consuming. Thus, CAMS are better suited for information retrieval than the conventional memories.

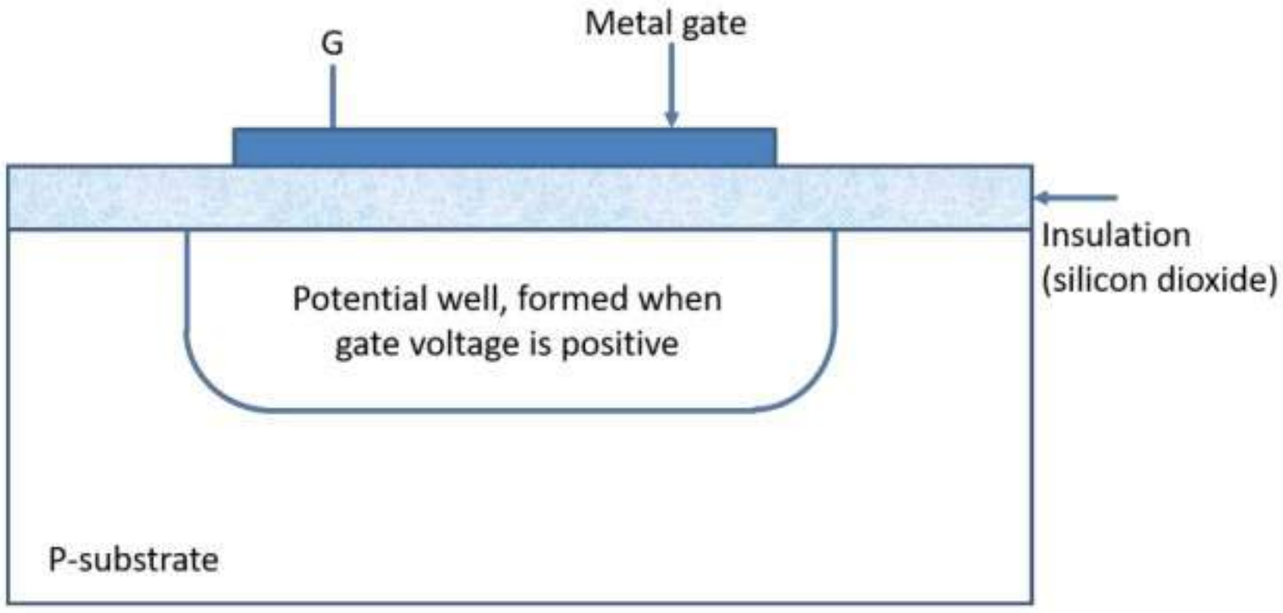
- CAMS are manufactured using MOS, CMOS, or bipolar technologies. The most popular CAMS use ECL circuitry because of its high-speed operation.

Operation of CAM



- A CAM can perform three basic operations: read, write and associate.
- Figure shows a block diagram of a CAM. Its storage capacity is M x N bits and is organized as M words of N bits each.
- It has N data input and N data output lines (one line for each bit of a word). The data input lines I_0 through I_{N-1} are used to input data to be written into the memory and for key word in case of associate operation.
- Data are read out of the CAM at the data output lines D_0 through D_{N-1}.
- The Y lines (Y_0 through Y_{M-1}) are bidirectional. During a read or write operation, these lines are used to select the storage location.
- There is one address input line for each word in the CAM. For example, Y_0 is the address line for memory location 0, Y_1, for memory location 1 and so on.
- Notice that linear selection addressing is used in CAMS rather than coincident selection addressing.
- The Y lines serve as match output lines one for each memory location, when an association operation is performed.
- For example, if the keyword matches with the word stored in memory locations 5 and 8, lines Y_5 and Y_8 will become HIGH to indicate the match condition.
- The more control inputs are used to select the required operation.
- The read and write operations are performed in a manner similar to that used for RAM.
- However, during the write operation, the input data also appear at the data outputs.
- The reading of the data is non-destructive.
- The word length and/or word size can be expanded by suitably connecting the available CAM chips in manner similar to the one used for RAMs and ROMs expansion.

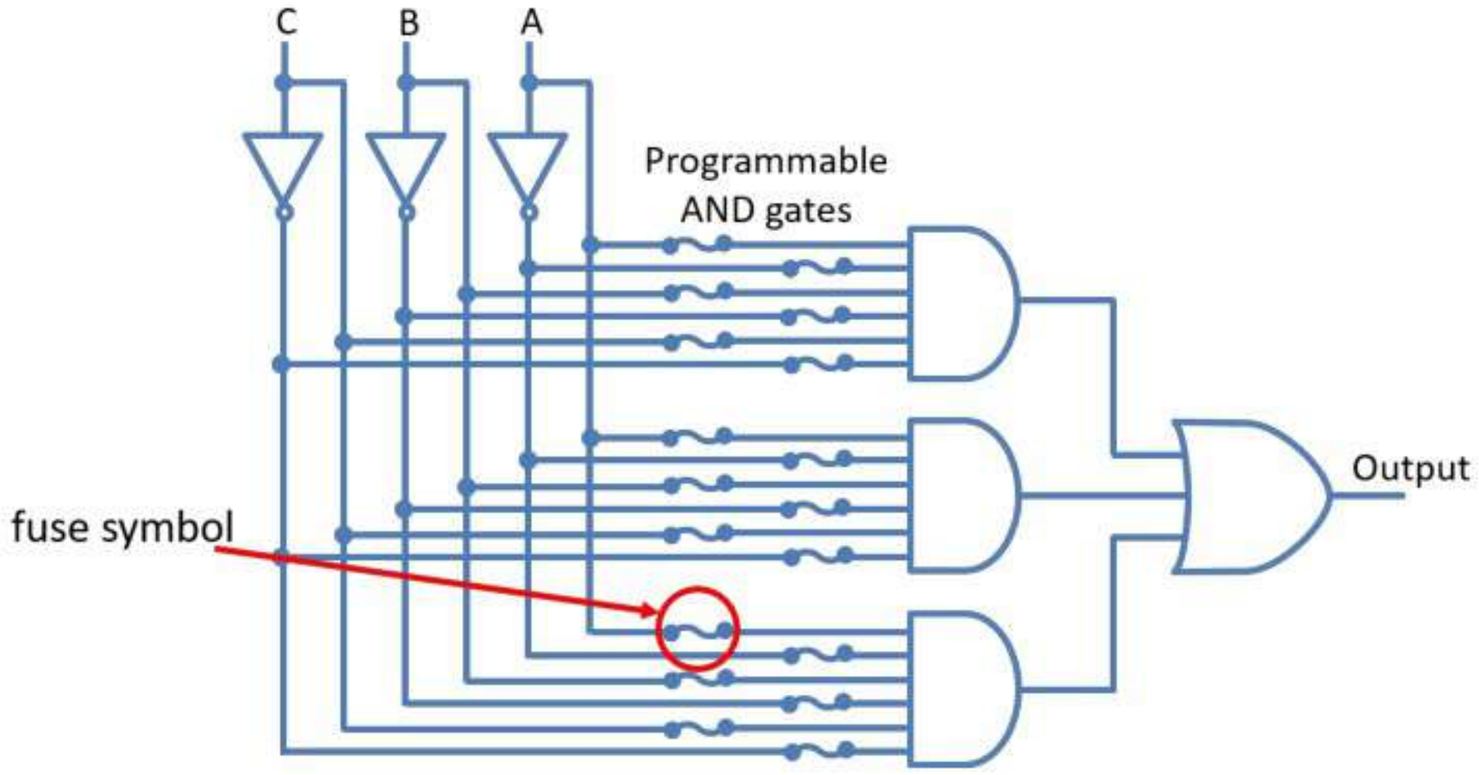
Charge coupled device memory (CCD)



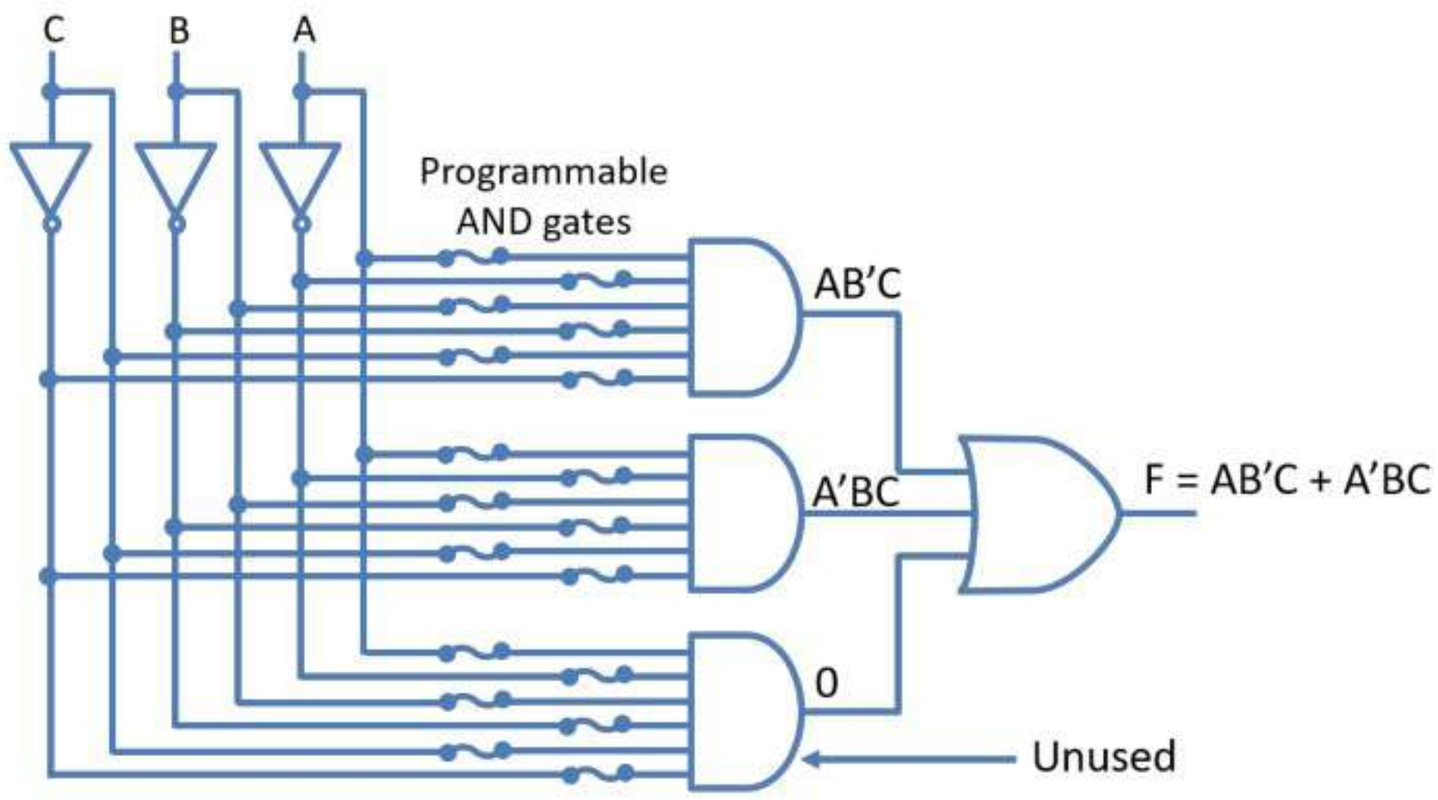
- The charge-coupled device (CCD) memory is a type of dynamic memory, in which packets of charges (electrons) are continuously transferred from one MOS device to another.
- The structure of a single MOS device is quite simple and is shown in figure.
- When a high voltage is applied to the metal gate, holes are repelled from a region beneath the gate in the P-type substrate.
- This region called a potential well is then capable of accepting a packet of negative charges.
- Data in the form of charge is transferred from one device to an adjacent one by clocking their gates.
- The CCD memory is inherently serial. Practical memories are constructed in the form of shift registers, each shift register being a line of CCDs.
- By controlling the timing of the clock signals applied to the shift registers, data can be accessed one bit at a time from a single register or several bits at a time from multiple registers.
- The principle advantage of the CCD memory is that, its single cell structure makes it possible to construct large capacity memories at low cost.
- On the other hand. like other dynamic memories, it must be periodically refreshed and driven by rather complex, multi-phase clock signals.
- Since data are stored serially, the average access time is long compared with the semiconductor RAM memory.

Programmable array logic (PAL)

- Programmable array logic (a registered trade mark of Monolithic Memories) is a particular family of programmable logic devices (PLDs) that is widely used and available from a number of manufacturers.
- The PAL circuits consist of a set of AND gates whose inputs can be programmed and whose outputs are connected to an OR gate, i.e. the inputs to the OR gate are hard-wired, i.e. PAL is a PLD with a fixed OR array and a programmable AND array.
- Because only the AND gates are programmable, the PAL is easier to program but is not as flexible as the PLA. Some manufacturers also allow output inversion to be programmed.
- Thus, like AND-OR and AND-OR-INVERT logic, they implement a sum of products logic function.
- Figure-1 below shows a small example of the basic structure.
- The fuse symbols represent fusible links that can be burned open using equipment similar to a PROM programmer.

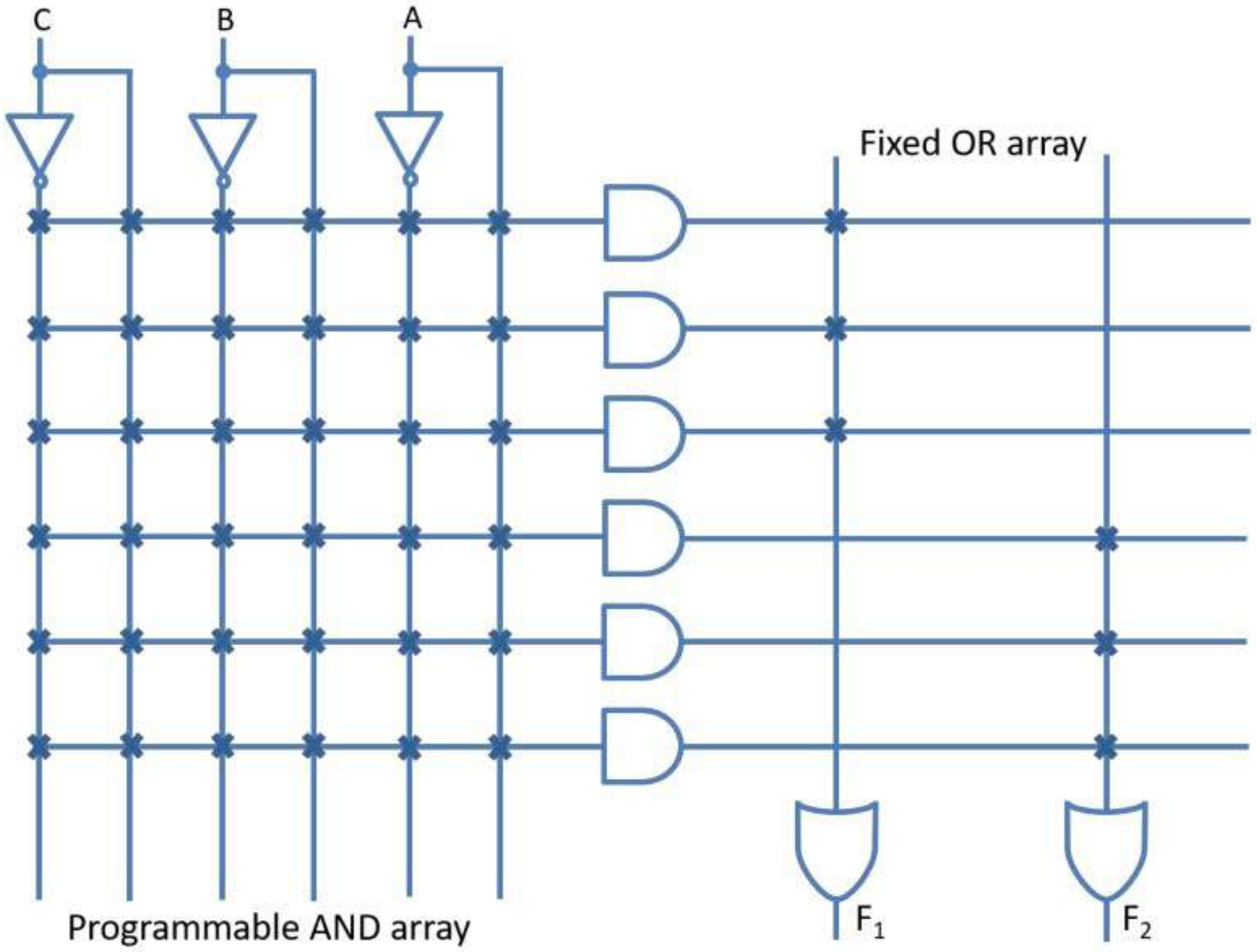


- Note that every input variable and its complement can be left either connected or disconnected from every AND gate.
- We then say that the AND gates are programmed.
- Figure-2 below shows how the circuit is programmed to implement F = A'BC + AB'C.
- Note this important point. All input variables and their complements are left connected to the unused AND gate, whose output is, therefore, AA'BB'CC' = 0.
- The 0 has no effect on the output of the OR gate. On the other hand, if all inputs to the unused AND gate were burned open, the output of the AND gate would 'float' HIGH (logic 1), and the output of the OR gate in that case would remain permanently 1.
- The actual PAL circuits have several groups of AND gates, each group providing inputs to separate OR gates.

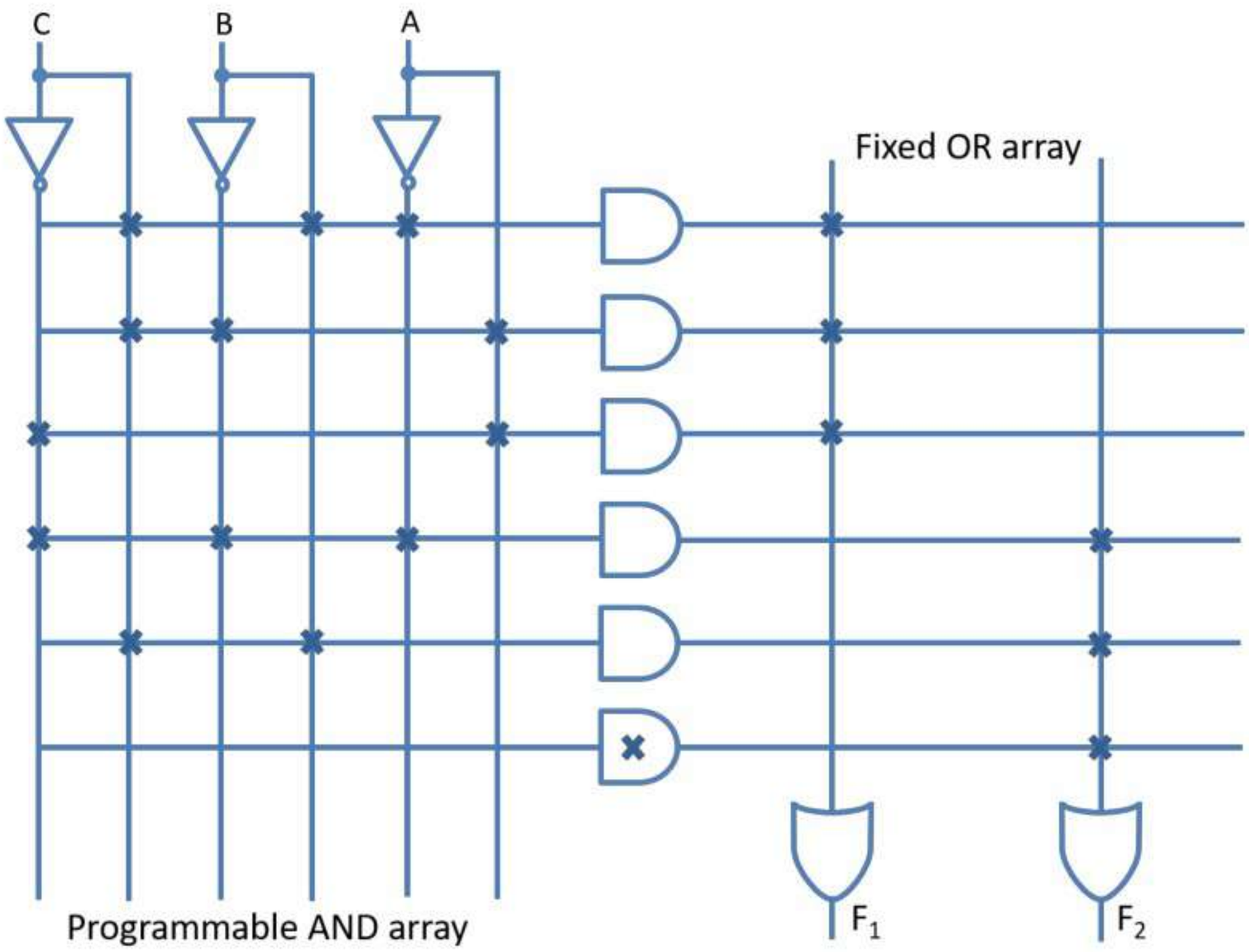


- Figure-3 shows an example of how the PAL structure is represented using the abbreviated connections.
- It is a 3-input 3-wide AND-OR structure. In this example, each function can have three minterms or product terms.
- Notice that there are six AND gates, which implies only six chosen products of not more than three variables ABC.
- Inputs to the OR gates at the outputs are fixed as shown by x marked on the vertical lines.
- The inputs to the AND gates are marked on the corresponding line by the x.

- Removing the x implies blowing off the corresponding fuse which in turn implies that the corresponding input variable is not applied to the particular AND gate.
- In this example, the circuit is unprogrammed because all the fusible links are intact.
- Note that, the 3-input OR gates are drawn with a single input line.



Example: Implement following functions using PAL: $F_1 = A'BC + AC' + AB'C$ and $F_2 = A'B'C' + BC$.



PAL Programming table

- The fuse map of a PAL can be specified in a tabular form. The PAL programming table consists of three columns.
- The first column lists the product terms numerically. The second column specifies the required paths between inputs and AND gates. The third column specifies the outputs of the OR gates.
- For each product term the inputs are marked with 1, 0, or – (dash).
- If a variable in the product term appears in its true form, the corresponding input variable is marked with a 1.
- If it appears in complemented form, the corresponding input variable is marked with a 0.
- If the variable is absent in the product term, it is marked as a – (dash).
- The paths between the inputs and the AND gates are specified under the column heading *inputs* in the programming table.
- A 1 in the input column specifies a connection from the input variable to the AND gate.
- A 0 in the input column specifies a connection from the complement of the variable to the input of the AND gate.
- A – (dash) specifies a blown fuse in both the input variable and its complement.
- It is assumed that a open terminal in the input of an AND gate behaves like a 1.
- The outputs of the OR gates are specified under the column heading *outputs*.
- The size of a PAL is specified by the number of inputs, the number of product terms, and the number of outputs.
- For n inputs, k product terms, and m outputs the internal logic of the PAL consists of n buffer inverter gates, k AND gates, and m OR gates.
- When designing a digital system with a PAL, there is no need to show the internal connections of the unit.
- All that is needed is a PAL programming table from which the PAL can be programmed to supply the required logic.

Example: Implement the following Boolean functions using PAL with four inputs and 3-wide AND-OR structure. Also write the PAL programming table.

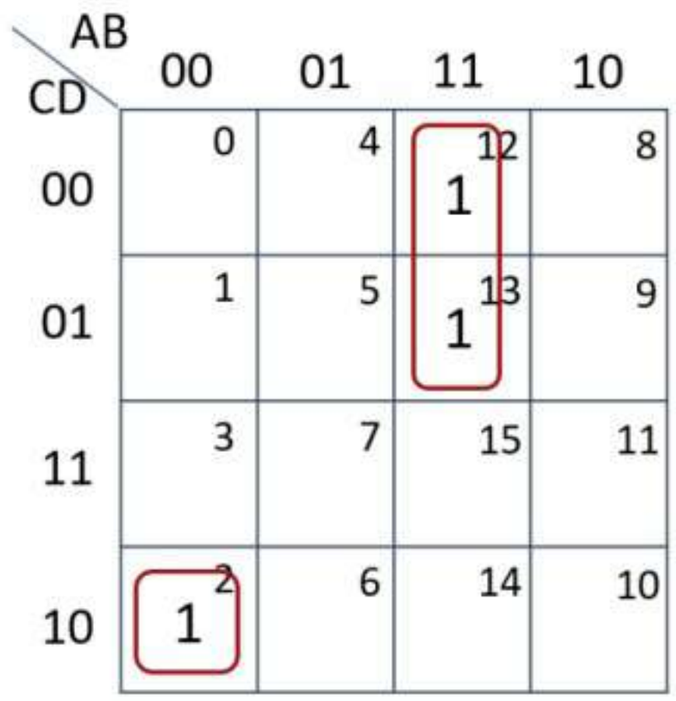
$F_1(A, B, C, D) = \sum_m(2, 12, 13)$

$F_2(A, B, C, D) = \sum_m(7, 8, 9, 10, 11, 12, 13, 14, 15)$

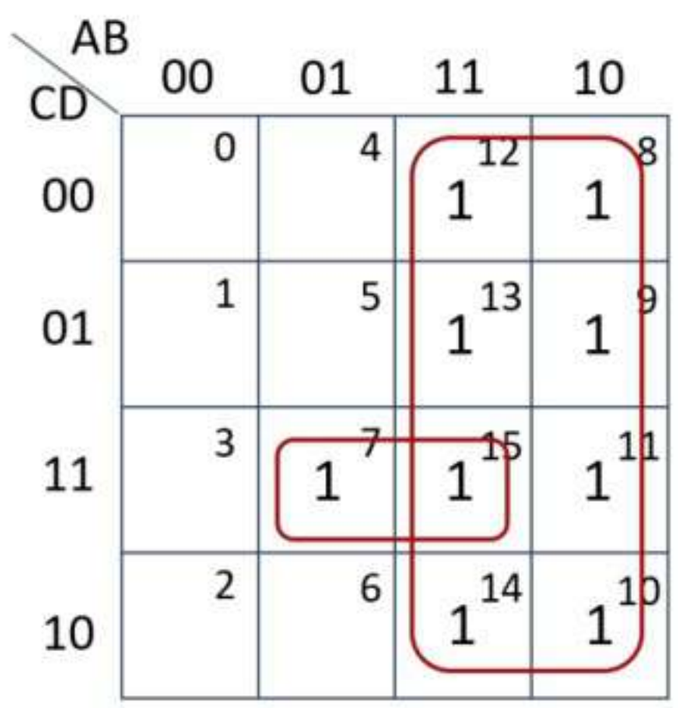
$F_3(A, B, C, D) = \sum_m(0, 2, 3, 4, 5, 6, 7, 8, 10, 11, 15)$

$F_4(A, B, C, D) = \sum_m(1, 2, 8, 12, 13)$

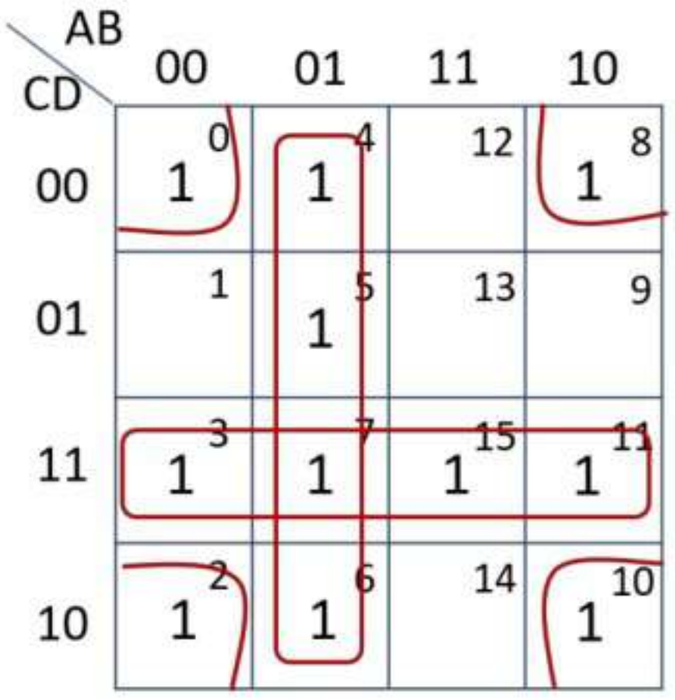
Solution:



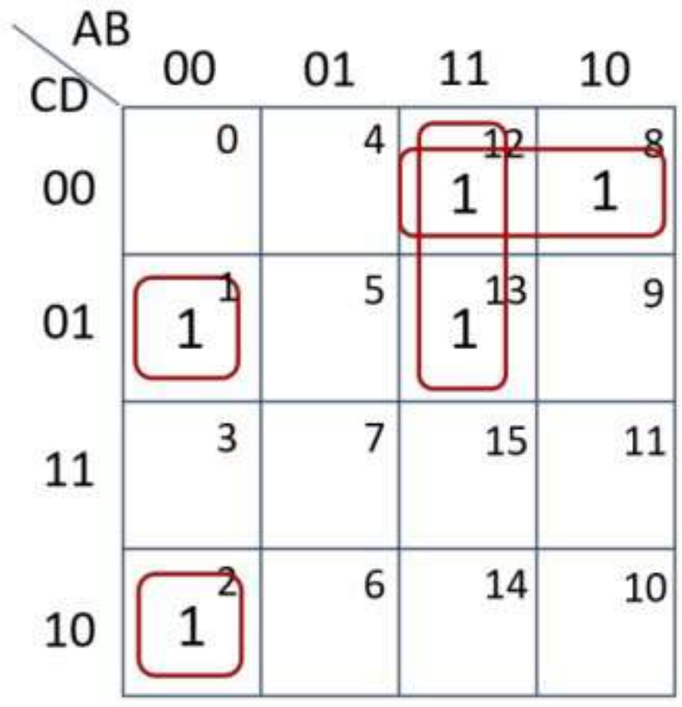
$F_1 = ABC' + A'B'CD'$



$F_2 = A + BCD$

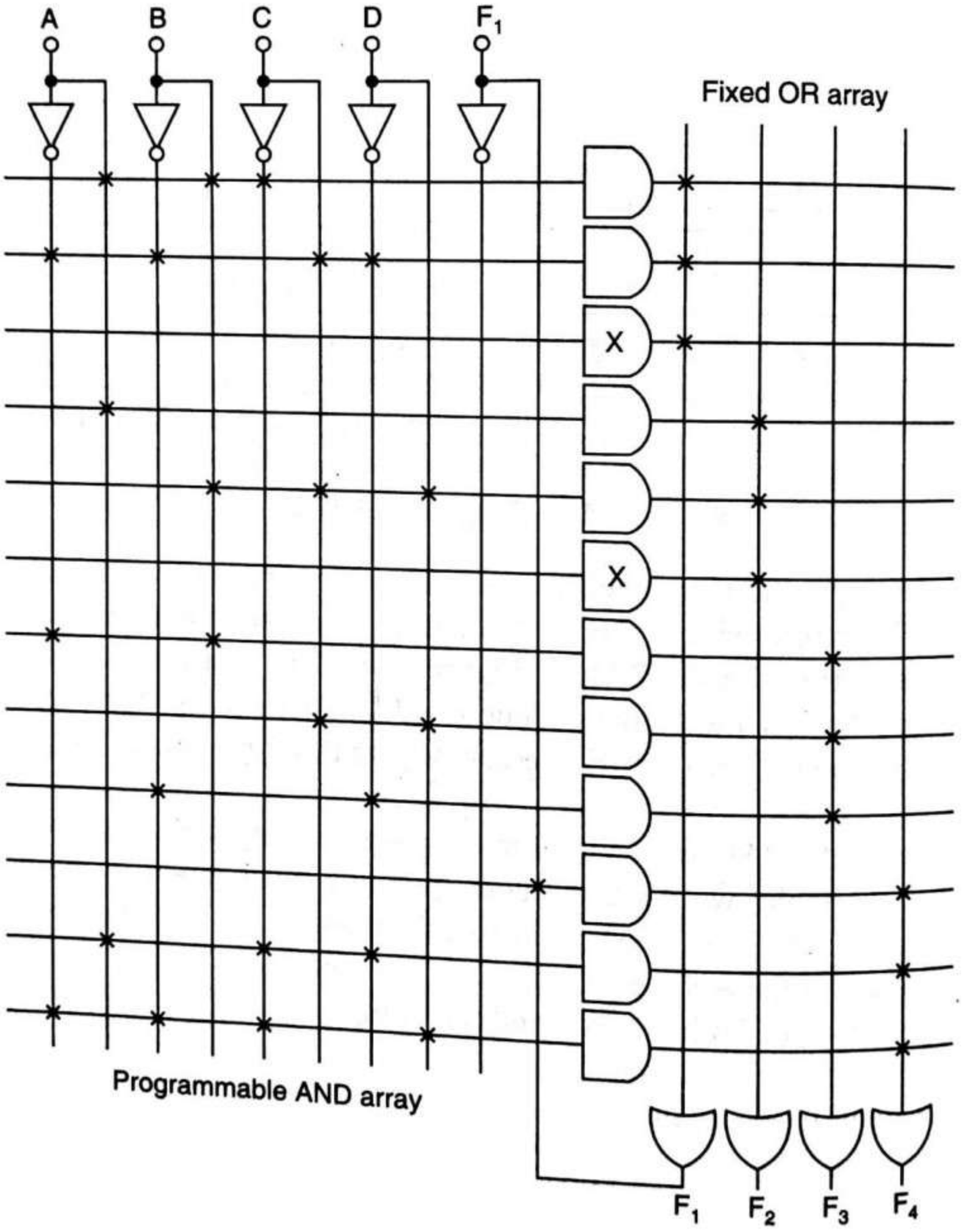


$F_3 = CD + A'B + B'D'$



$F_4 = ABC' + AC'D' + A'B'C'D + A'B'CD'$
$= F_1 + AC'D' + A'B'C'D$

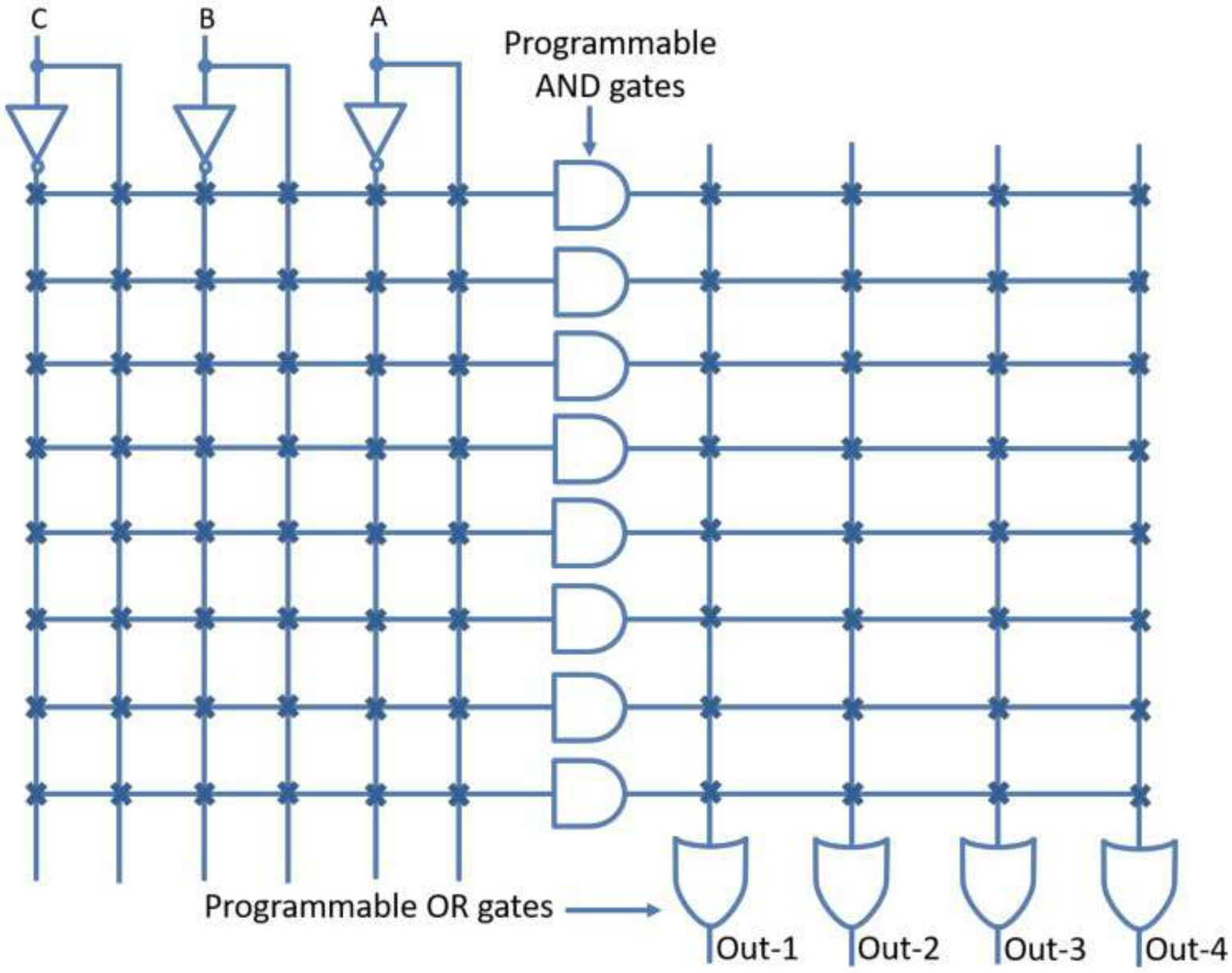
Product term	AND Inputs					Outputs
	A	B	C	D	F_1	
1	1	1	0	-	-	$F_1 = ABC' + A'B'CD'$
2	0	0	1	0	-	
3	-	-	-	-	-	
4	1	-	-	-	-	$F_2 = A + BCD$
5	-	1	1	1	-	
6	-	-	-	-	-	
7	0	1	-	-	-	$F_3 = CD + A'B + B'D'$
8	-	-	1	1	-	
9	-	0	-	0	-	
10	-	-	-	-	1	$F_4 = F_1 + AC'D' + A'B'C'D$
11	1	-	0	0	-	
12	0	0	0	1	-	



Programmable logic array (PLA)

- The PLA represents another type of programmable logic but with a slightly different architecture.
- The PLA combines the characteristics of the PROM and the PAL by providing both a programmable OR array and a programmable AND array, i.e. in a PLA both AND gates and OR gates have fuses at the inputs.
- A third set of fuses in the output inverters allows the output function to be inverted if required.
- Usually X-OR gates are used for controlled inversion. This feature makes it the most versatile of the three PLDs.
- However, it has some disadvantages. Because it has two sets of fuses, it is more difficult to manufacture, program and test it than a PROM or a PAL.
- Figure demonstrates the structure of a three-input, four-output PLA with every fusible link intact.

- Like ROM, PLA can be mask programmable or field programmable. With a mask programmable PLA, the user must submit a PLA programming table to the manufacturer.
- This table is used by the vender to produce a user made PLA that has the required internal paths between inputs and outputs.
- A second type of PLA available is called a field programmable logic array or FPLA.
- The FPLA can be programmed by the user by means of certain recommended procedures.

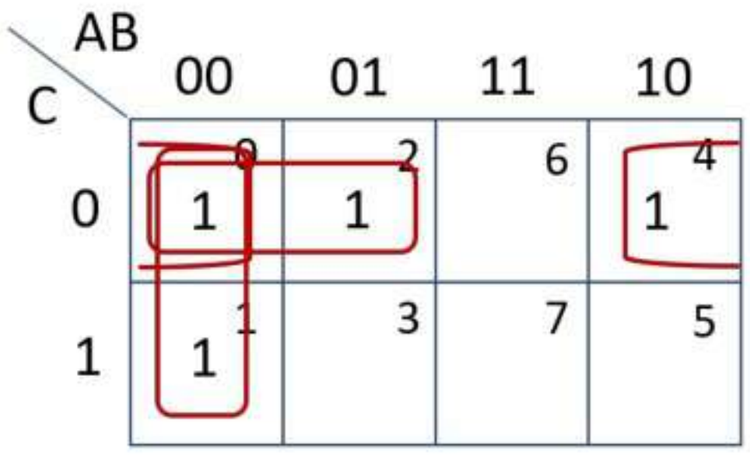


Example: Implement the following two Boolean functions with a PLA:

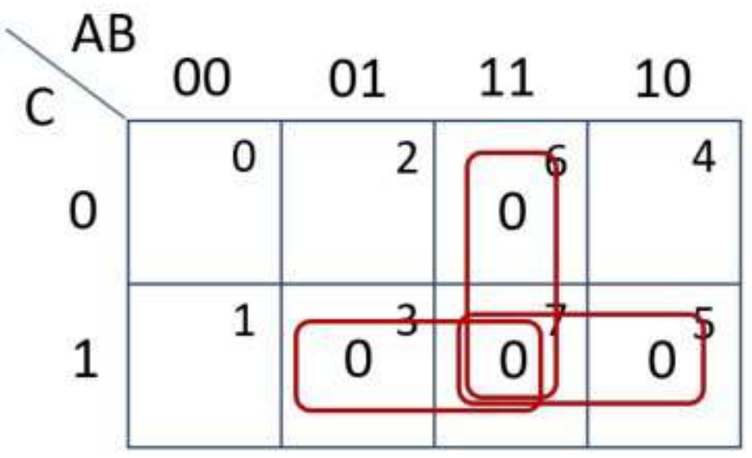
$F_1(A, B, C) = \sum_m(0, 1, 2, 4)$

$F_2(A, B, C) = \sum_m(0, 5, 6, 7)$

Solution:



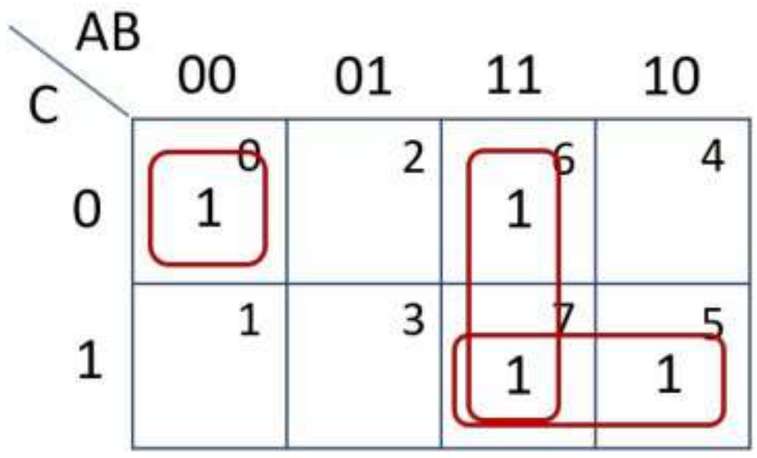
$F_1(T) = A'C' + B'C' + A'B'$



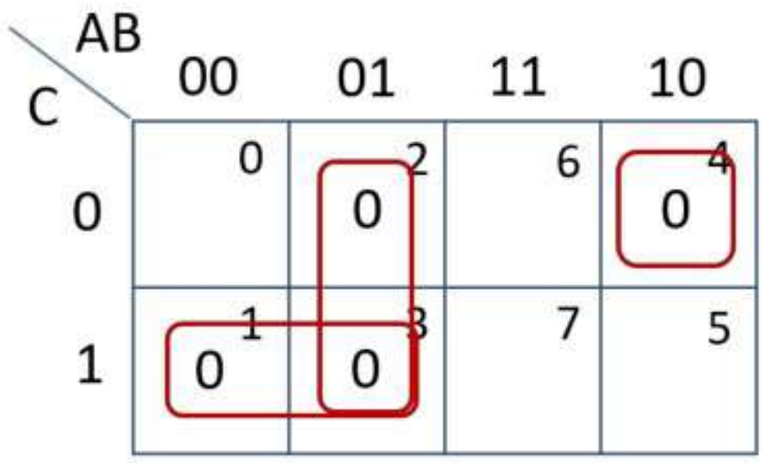
$F_1 = (A'+B')\,(B'+C')\,(A'+C')$

$F_1' = AB + AC + BC$

$F_1(C) = (AB + AC + BC)'$



$F_2(T) = A'B'C' + AB + AC$

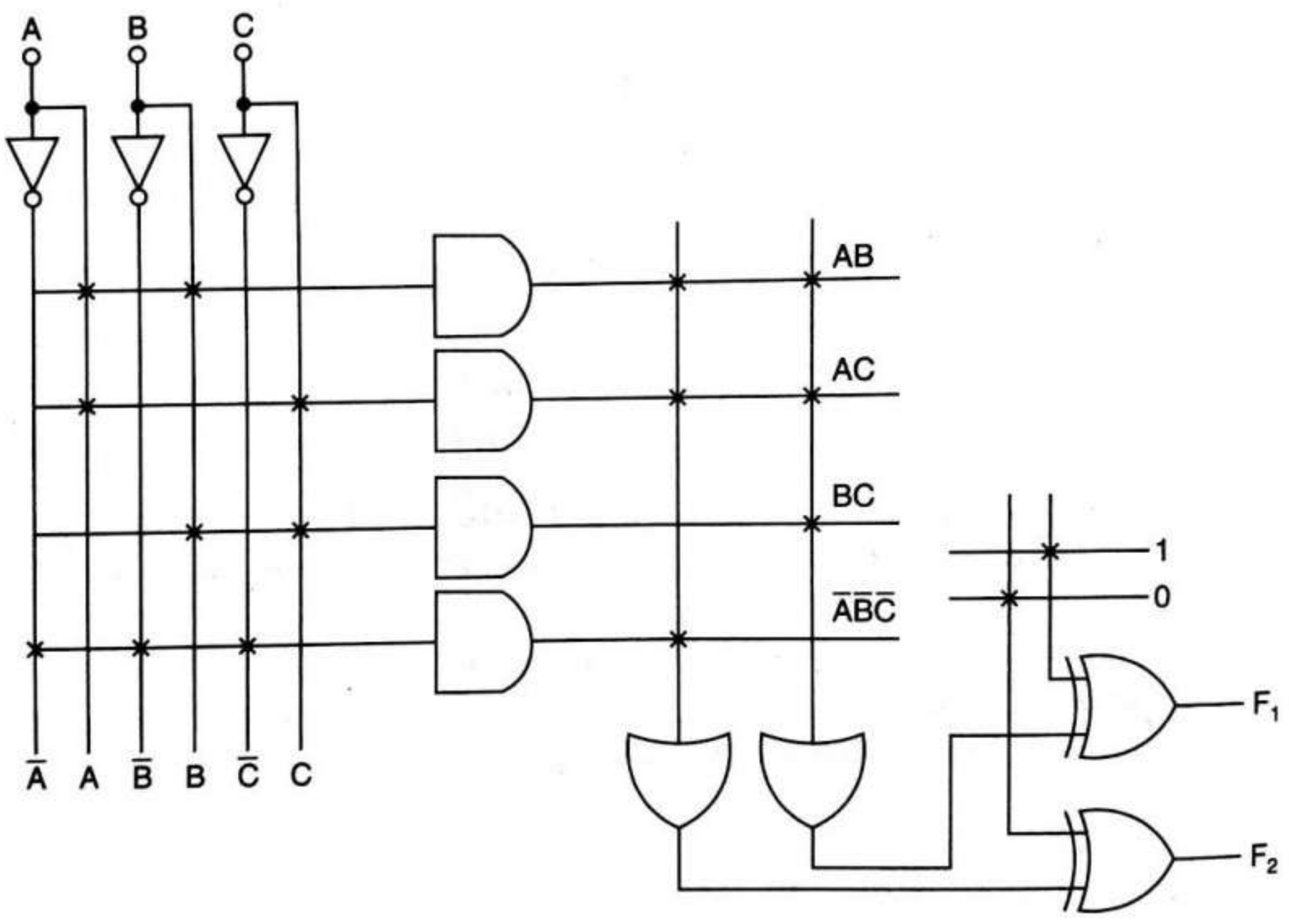


$F_2 = (A+B')\,(A+C')\,(A'+B+C)$

$F_2' = A'B + A'C + AB'C'$

$F_2(C) = (A'B + A'C + AB'C')'$

Product term		Inputs			Outputs	
		A	B	C	$F_1(C)$	$F_2(T)$
1	AB	1	1	-	1	1
2	AC	1	-	1	1	1
3	BC	-	1	1	1	-
4	A'B'C'	0	0	0	-	1

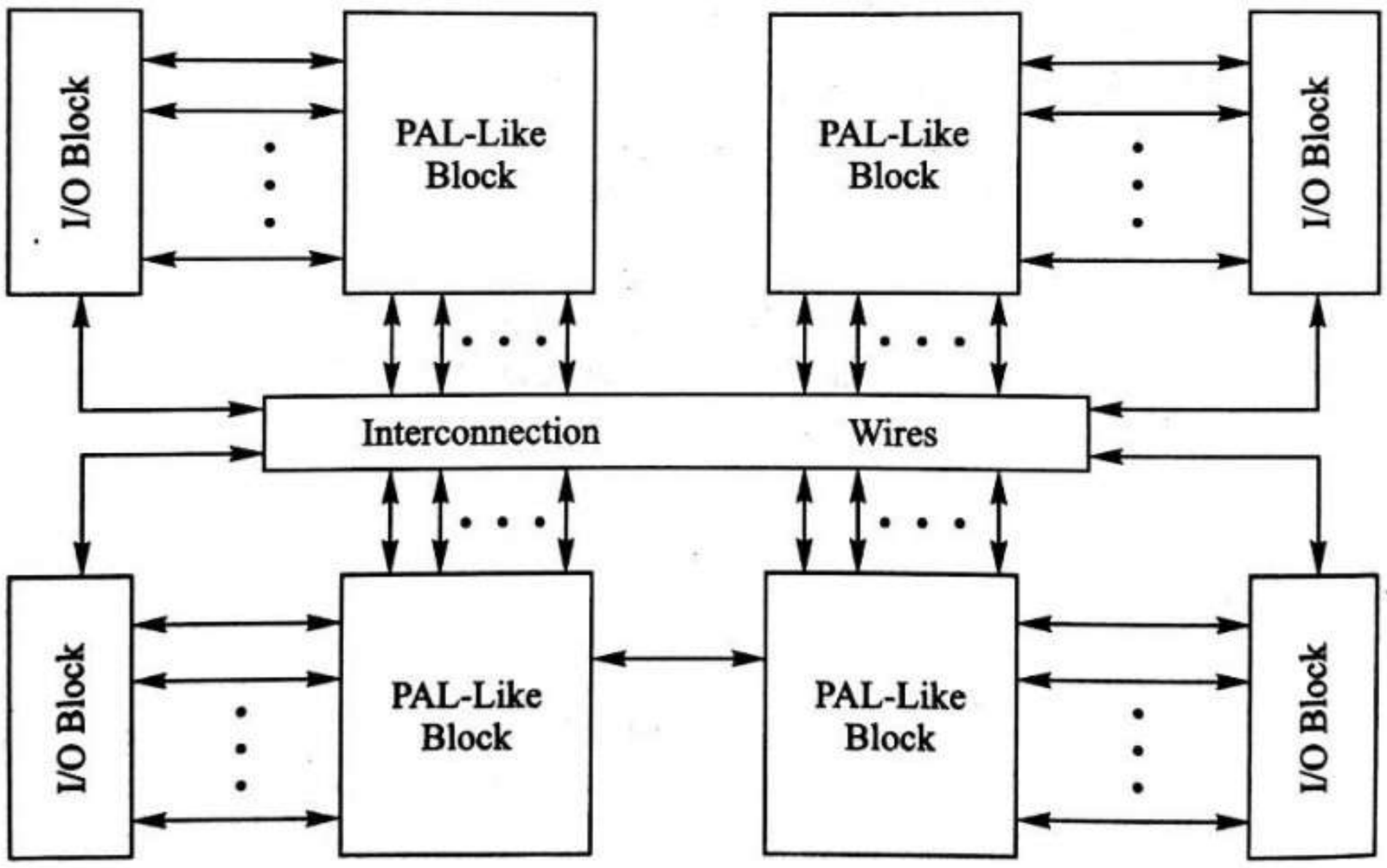


Complex programmable logic device (CPLD)

- The simple programmable logic devices (SPLDs), such as PALs, EEPLDs, and GALs etc. have limited number of inputs, product terms, and outputs.
- These devices, therefore, can support up to about 32 total number of inputs and outputs only.
- For implementation of circuits that require more inputs and outputs than that are available in a single SPLD chip, either multiple SPLD chips can be employed or more sophisticated type of chip, referred to as *complex programmable logic device* (CPLD) can be used.
- The expansion of PLD using multiple SPLD chips have the following disadvantages:
  - PC board area requirement increases with the number of chips.
  - Connecting wires will result in adverse capacitive effects.
  - Power requirement increases with the number of chips.
  - The system cost increases.
- Another method of increasing the I/O and product terms can be designing of PLDs using the architecture of SPLDs.
- This approach was discarded by the designers because of the following problems associated with this approach
  - increase in capacitive effects
  - increase in leakage currents
  - decrease in speed
  - cost effectiveness
- In view of the above difficulties, complex programmable logic devices (CPLDs) were evolved.
- A CPLD is just a collection of individual PLDs on a single chip and programmable interconnection structure.
- By using programming methods, the resources available in various PLDs can be shared in different ways to design complex logic functions.
- The complexity of any digital IC chip can be specified in terms of number of equivalent 2-input NAND gates.
- A typical PAL has 8 macro-cells, if each macro-cell represents about 20 equivalent gates, then the PAL can accommodate a circuit that needs up to about 160 gates.
- For circuits requiring a very large number of gates, CPLDs having large number of macro-cells (say 512 macro-cells) can implement circuits of up to about 10,000 equivalent gates.
- There are a number of manufacturers of CPLDs manufacturing a wide range of products with different features.

Block diagram

- Figure gives block diagram of a complex programmable logic device (CPLD).
- It consists of a number of PAL-like blocks, I/O blocks, and a set of interconnection wires.
- The PAL-like blocks are connected to a set of interconnection wires and each block is also connected to an I/O block to which a number of chip's input and output pins are attached.
- A PAL-like block usually consists of about 16 macro-cells.
- Each macro-cell consists of an AND-OR configuration, an EX-OR gate, a FLIP-FLOP, a multiplexer, and a tri-state buffer.
- Each AND-OR configuration usually consists of 5-20 AND gates and an OR gate with 5-20 inputs.
- An EX-OR gate is used to obtain the output of OR gate in inverted or non-inverted form depending upon its other input being 1 or 0 respectively.
- A D-FF stores the output of the EX-OR gate, a multiplexer selects either the output of the D-FF or the output of the EX-OR gate depending upon its select input.



Field programmable gate array (FPGA)

- The programmable logic devices (SPLDs and CPLDs) are based on similar basic architecture-the programmable array logic (PAL) or the programmable logic array (PLA).
- Over the years, programmable arrays have increased in size and complexity, and highly configurable output macro-cells have been added to enhance their flexibility and expandability.
- To increase the effective size and to add more functionality in a single programmable device, alternative architectures have been developed which are known as *field-programmable gate arrays* (FPGAs).
- The logic densities of FPGAs are much higher than those of CPLDs.
- They range in size from a few thousands to hundreds of thousands equivalent gates.
- From modern standards digital circuits with hundreds of thousands of gates is not too large.
- FPGA devices support implementation of relatively large complex logic circuits.
- The FPGAs do not contain AND, OR planes, instead they provide logic blocks for implementation of the required digital functions.
- The FPGA is composed of a number of relatively independent configurable logic blocks (CLBs), configurable I/O blocks, and programmable interconnection paths (known as routing channels).
- All the resources of the device are uncommitted and that these must be selected, configured and interconnected by a user to form a logic circuit for his application.
- The basic architecture of an FPGA is shown in figure.
- There are a number of manufacturers of FPGA devices.
- The various families of FPGAs manufactured by different manufacturers differ primarily in the number of logic modules (from few hundreds to hundreds of thousands), supply voltage range, power consumption, speed, architecture, process technology, number of pins, and type of packages, etc.
- The basic FPGA architecture consists of an array of configurable logic blocks (CLBs).

- The logic blocks are surrounded by configurable input/output blocks. There are rows and columns of programmable interconnection paths.
- The I/O blocks can be individually configured as input, output, or bidirectional.