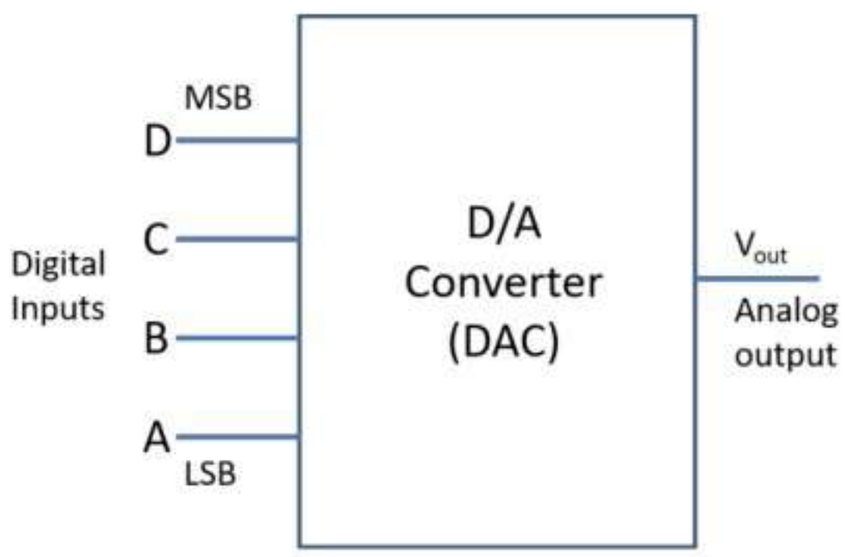
Basics of digital to analog converter

- Basically, D/A conversion is the process of converting a value represented in digital code, such as straight binary or BCD, into a voltage or current which is proportional to the digital value.
- Figure shows the symbol for a typical 4-bit D/A converter.
- Each of the digital inputs A, B, C, and D can assume a value 0 or a 1, therefore, there are $2^4 = 16$ possible combinations of inputs.
- For each input number 0000, 0001, . . .,1111, the D/A converter outputs a unique value of voltage.
- The analog output voltage V_{out} is proportional to the input binary number, that is,

  Analog output = K X digital input

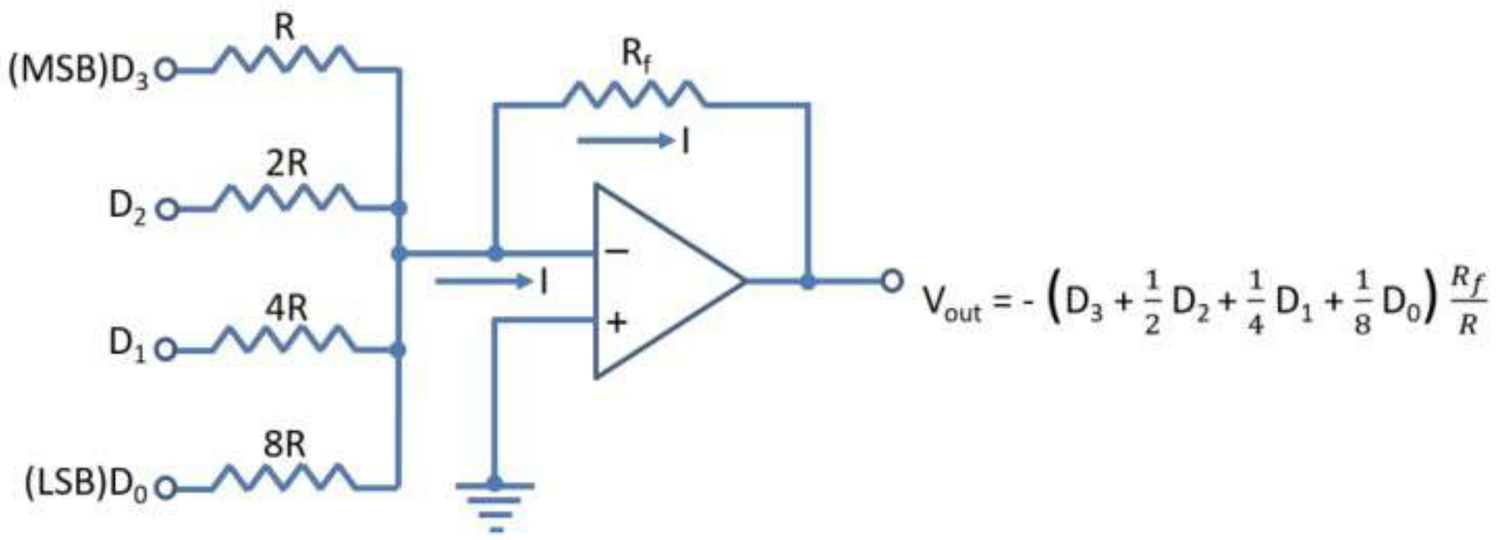
  where K is the proportionality factor and is a constant value for a given DAC.

- The analog output can, of course, be current or voltage.



- Strictly speaking, the output of a DAC is not a true analog quantity, because it can take on only specific values.
- In that sense, it is actually digital. Thus, the output of a DAC is a 'pseudo-analog' quantity.
- By increasing the number of input bits, the number of possible output values can be increased and also the step size (the difference between two successive output values) can be reduced, thereby producing an output that is more like an analog quantity
- When the binary counter is continually recycled through its 16 states by applying the clock Signal, the DAC output will be a staircase waveform with a step size of 1 V.
- When the counter is at 0000, the output of the DAC is minimum (0 V).
- When the counter is at 1111, the output of the DAC is maximum (15 V). This is the full-scale output.
- Digital-to-analog and analog-to-digital conversions form the very important aspects of digital data processing.
- Digital-to-analog conversion is a straightforward process and is considerably easier than the A/D conversion. In fact, a DAC is usually an integral part of any ADC.

Weighted-resistor type DAC



- The diagram of the weighted-resistor DAC is shown in figure.
- The operational amplifier is used to produce a weighted sum of the digital inputs, where the weights are proportional to the weights of the bit positions of inputs.
- Since the op-amp is connected as an inverting amplifier, each input is amplified by a factor equal to the ratio of the feedback resistance divided by the input resistance to which it is connected.
- The MSB D_3 is amplified by R_f/R, D_2 is amplified by $R_f/2R$, D_1 is amplified by $R_f/4R$ and D_0, the LSB is amplified by $R_f/8R$.
- The inverting terminal of the op-amp in figure acts as a virtual ground.
- Since the op-amp adds and inverts,

$$V_{out} = -\left(D_3 + \frac{D_2}{2} + \frac{D_1}{4} + \frac{D_0}{8}\right) x \left(\frac{R_f}{R}\right)$$

- The main disadvantage of this type of DAC is, that a different-valued precision resistor must be used for each bit position of the digital input.

Example: For the weighted-resistor DAC, determine (a) the weight of each input bit if the inputs are 0 V and 5 V, (b) the full-scale output, if $R_f = R = 1\ k\Omega$.

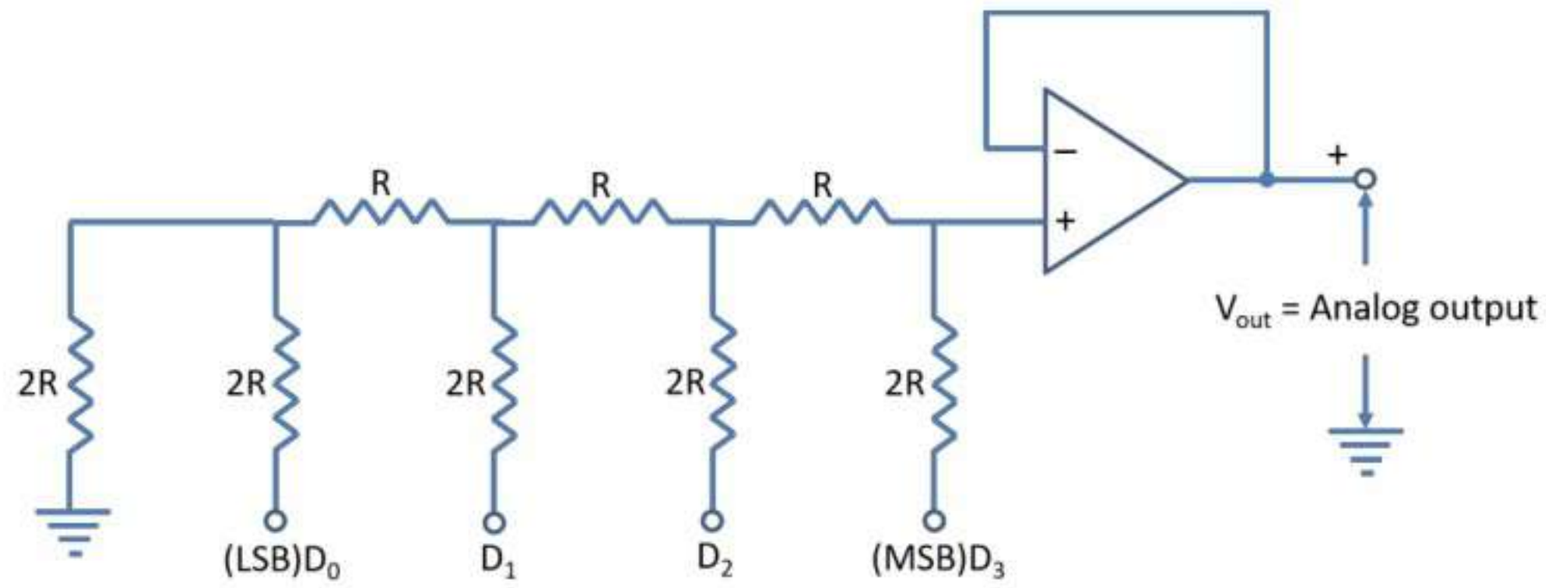
Solution: (a) If MSB passes with a gain of 1. so, its weight = 5 V; the next bit passes with a gain of 1/2. so, its weight = 2.5 V; the following bit passes with a gain of 1/4. so, its weight = 1.25 V; the LSB passes with a gain of 1/8. so, its weight = 0.625 V.

(b) Therefore, the full-scale output when $R_f = R = 1\ k\Omega$

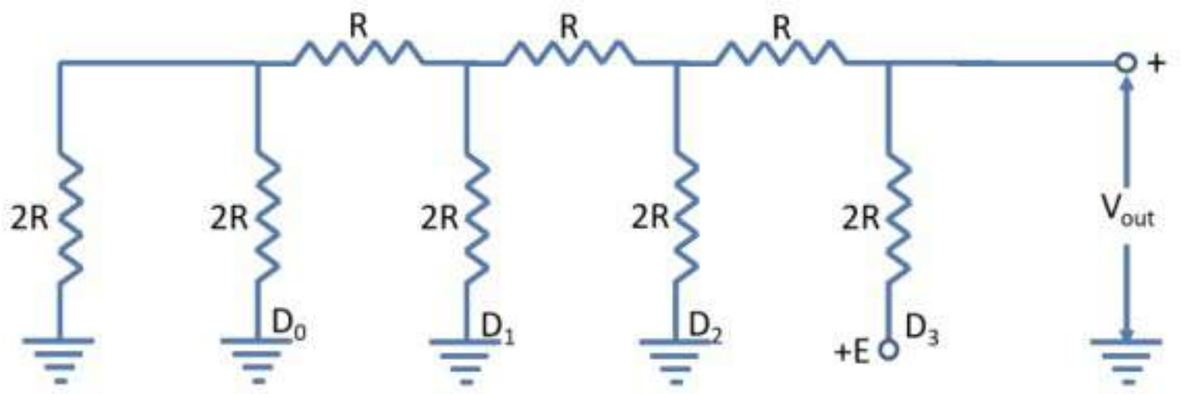
$$V_{out} = -\left(5 + \frac{5}{2} + \frac{5}{4} + \frac{5}{8}\right) = -9.375\ V$$

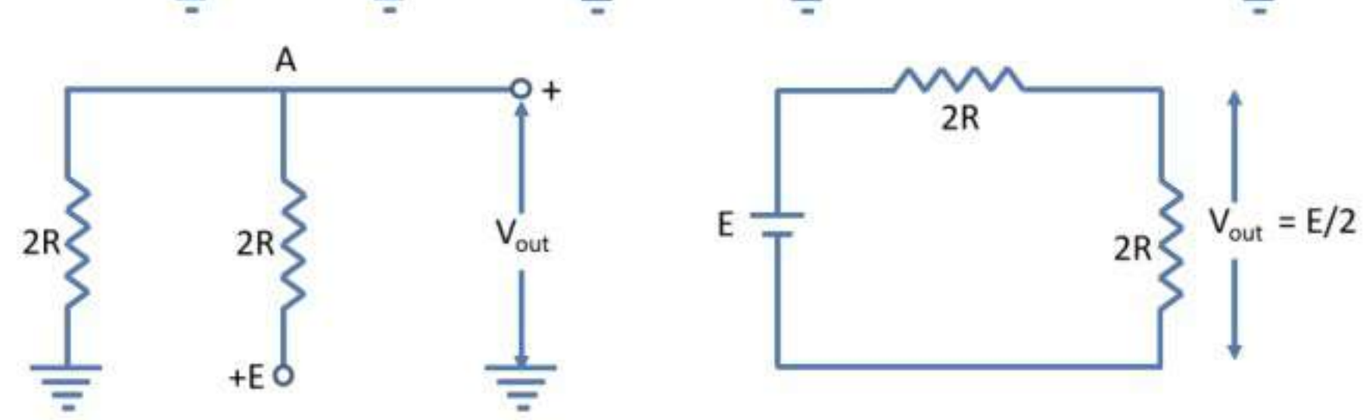
R-2R ladder type DAC

- The R-2R ladder type DAC is the most popular DAC. It uses a ladder network containing series-parallel combinations of two resistors of values R and 2R.
- The operational amplifier configured as voltage follower is used to prevent loading.
- Figure shows the circuit diagram of a R-2R ladder type DAC having 4-bit digital input.
- When a digital signal $D_3D_2D_1D_0$ is applied at the input terminals of the DAC, an equivalent analog signal is produced at the output terminal.

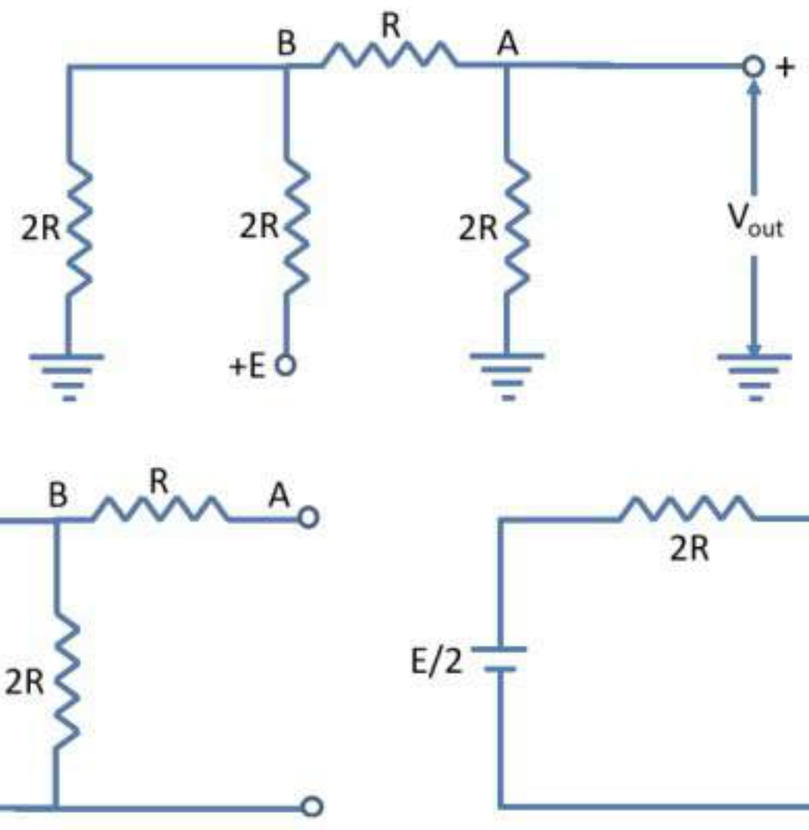


- ***Case 1: When the input is 1000***
  - Below figure illustrates the procedure to calculate V_{out} when the input is 1000.
  - At the left end of the ladder, 2R is in parallel with 2R, so that the combination is equivalent to R.
  - This R is in series with another R giving 2R. This 2R in parallel with another 2R is equivalent to R.
  - Continuing in this manner, we ultimately find that R_{eq} = 2R.
  - The output voltage, V_{out} = E/2.

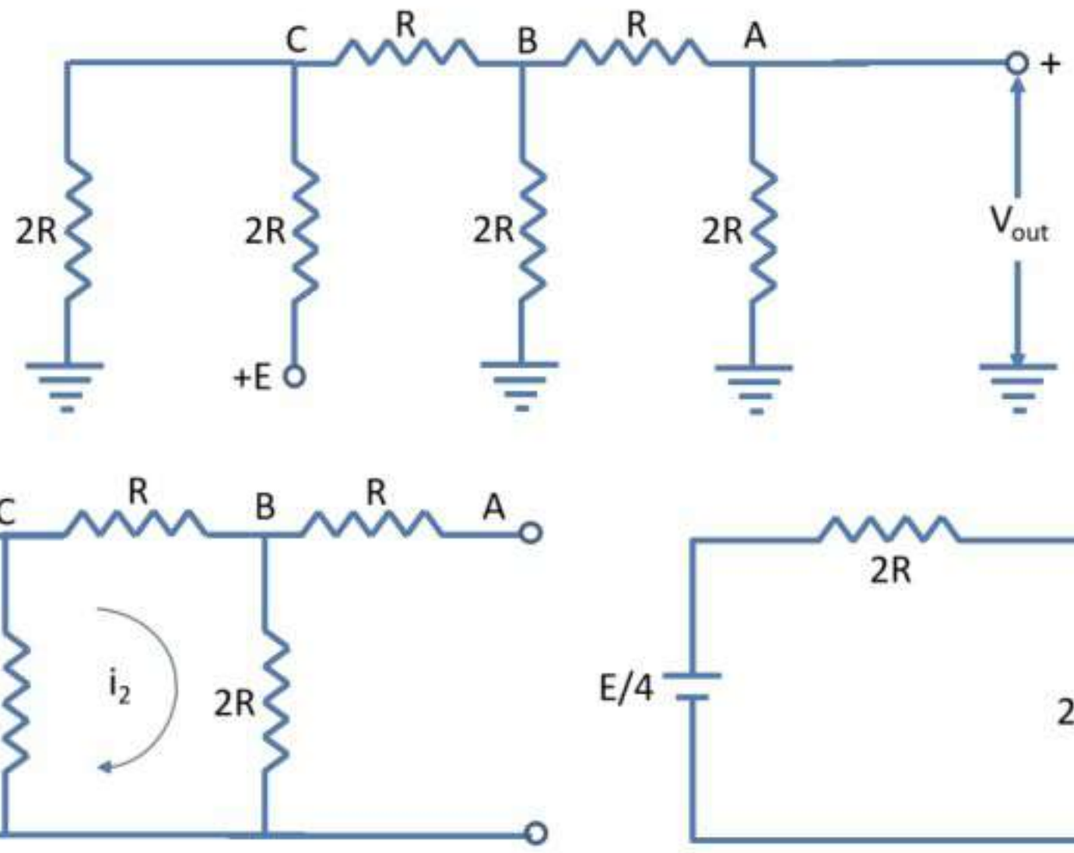




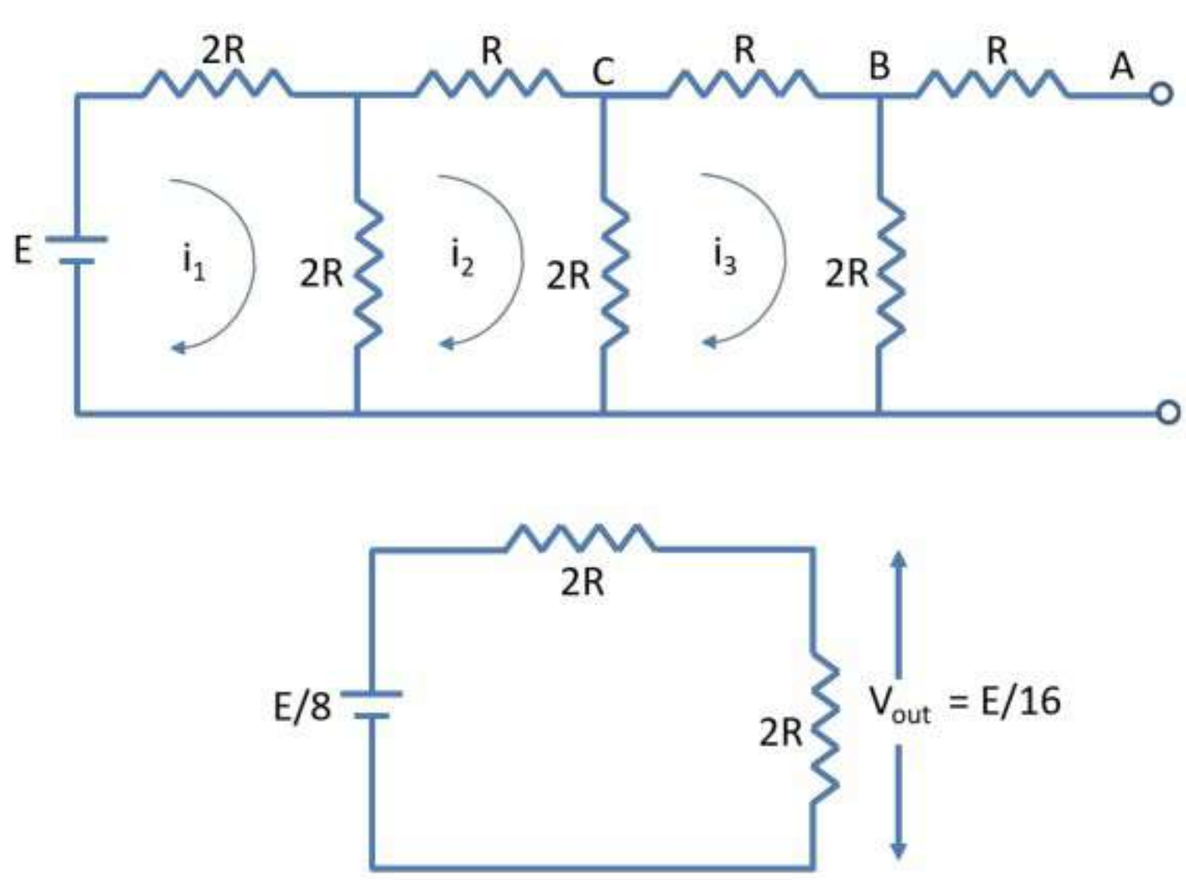
- ***Case 2: When the input is 0100***
  - Below figure illustrates the procedure to calculate V_{out} when the input is 0100.
  - Here, we find that to left of terminal B, R_{eq} = 2R. The output voltage, V_{out} = E/4



- ***Case 3: When the input is 0010***
  - Below figure illustrates the procedure to calculate V_{out} when the input is 0010.
  - Here, we find that to left of terminal C, R_{eq} = 2R. The output voltage, V_{out} = E/8.



- ***Case 4: When the input is 0001***
  - Below figure illustrates the procedure to calculate V_{out} when the input is 0001.
  - The output voltage, V_{out} = E/16.



Specifications for DAC

Resolution (step size):

- The resolution of a DAC is defined as the smallest change that can occur in an analog output as a result of a change in the digital input.
- The resolution of a DAC is also defined as the reciprocal of the number of discrete steps in the full-scale output of the DAC.
- The resolution is always equal to the weight of the LSB and is also referred to as the step size.
- The resolution or step size is the size of the jumps in the staircase waveform.

- The step size is the amount by which V_{out} will change as the digital input value is changed from one value to the next.
- The step size of the DAC is the same as the proportionality factor in the DAC input-output relationship.
- Although resolution can be expressed as the amount of voltage or current per step, it is also useful to express it as a percentage of the full-scale output as

$$\%\ resolution = \frac{step\ size}{full\ scale}\ X\ 100\%$$

Since, full-scale = number of steps x step size, resolution can be expressed as

$$\%\ resolution = \frac{1}{total\ number\ of\ steps}\ X\ 100\%$$

- In general, for an N-bit DAC, the number of different levels will be 2^N and the number of steps will be $2^N - 1$.
- The greater the number of bits, the greater will be the number of steps and the smaller will be the step size, and therefore, the finer will be the resolution.
- Of course, the cost of the DAC increases with the number of input bits.

Accuracy

- The accuracy of a DAC is usually specified in terms of its full-scale error and linearity error, which are normally expressed as a percentage of the converter's full-scale output.
- The full-scale error is the maximum deviation of the DAC's output from its expected (ideal) value, expressed as a percentage of the full-scale.
- The linearity error is the maximum deviation of the analog output from the ideal output.
- The accuracy and resolution of a DAC must be compatible.

Settling time

- The operating speed of a DAC is usually specified by giving its settling time.
- It is defined as the total time between the instant when the digital input changes and the time that the output enters a specified error band for the last time, usually ± 1/2 LSB around the final value after the change in digital input.
- It is measured as the time for the DAC output to settle within ± 1/2 step size of its final value.
- Generally, DACs with a current output will have shorter settling times than those with voltage outputs.

Offset voltage

- Ideally, the output of a DAC should be zero when the binary input is zero.
- In practice, however, there is a very small output voltage under this situation called the offset voltage.
- This offset error, if not corrected, will be added to the expected DAC output for all input cases.

Monotonicity

- A DAC is said to be monotonic if its output increases as the binary input is incremented from one value to the next.
- This means that the staircase output will have no downward steps as the binary input is incremented from 0 to full-scale value.

- The DAC is said to be non-monotonic, if its output decreases when the binary input is incremented.

Temperature sensitivity

- The analog output voltage for any fixed digital input varies with temperature.

Example: An 8-bit DAC produces V_{out} = 0.05 V for a digital input of 00000001. Find the full-scale output. What is the resolution? What is V_{out} for an input of 00101010?

Solution:

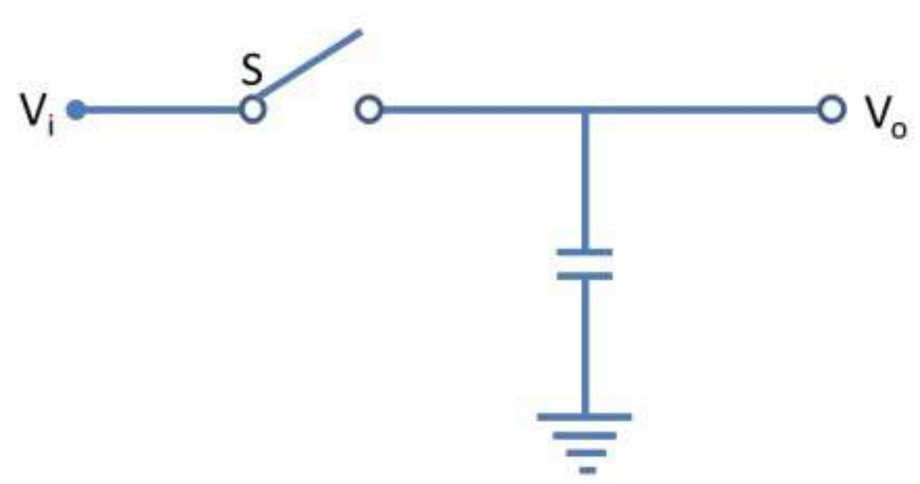
- Full-scale output = Step size x No. of steps
  = 0.05 x ($2^8 - 1$) = 0.05 x 255 = 12.75 V

- % resolution = 1 / 255 x 100 %
  = 0.392 %

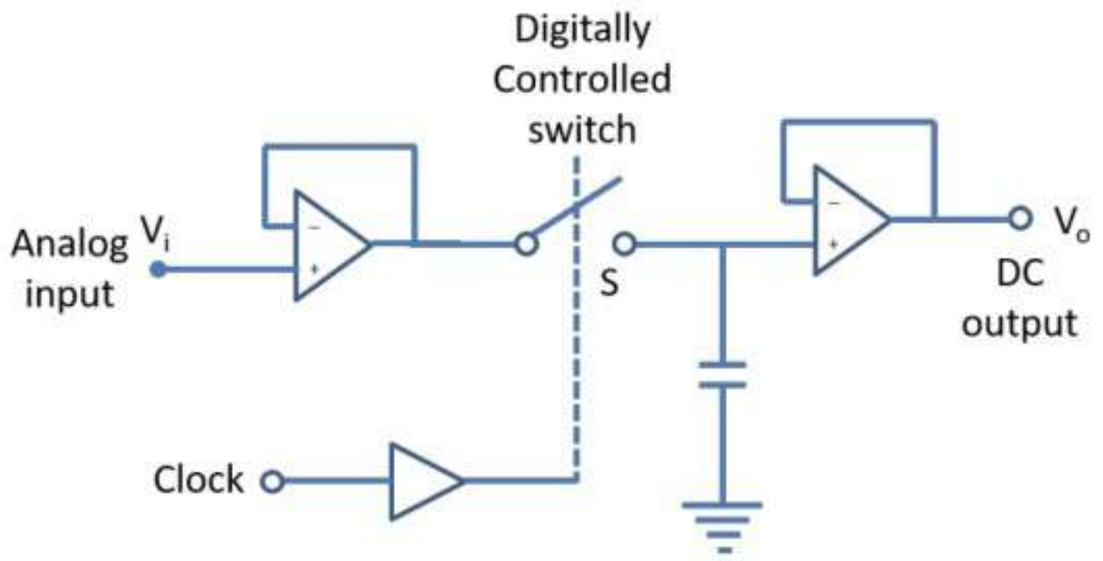
- V_{out} for an input of 00101010 = 42 x 0.05
  = 2.10 V

Sample and hold circuit

- A basic sample-and-hold circuit is shown in Fig.
- In this circuit the voltage across the capacitor follows the input signal voltage V_i during the time switch S is closed.
- The capacitor holds the instantaneous value of the signal voltage attained just before the switch is opened.
- Thus, for every T, the switch is closed for a short duration and then opened.



- The d.c voltage across the capacitor gives the value of the signal at the instant the switch is opened.
- This d.c voltage represents a sample of the signal and is converted to digital signal using A/D converter circuit during the hold period.
- Figure shows a practical S/H circuit in simplified form.
- It consists of two unity gain amplifiers A_1 and A_2 and a digitally controlled switch S.
- Analog input voltage is applied at the input of buffer amplifier A_1.
- The high input impedance of A_1 will prevent loading of the analog signal and its low output impedance will help in the fast charging of the capacitor C when the switch is closed.



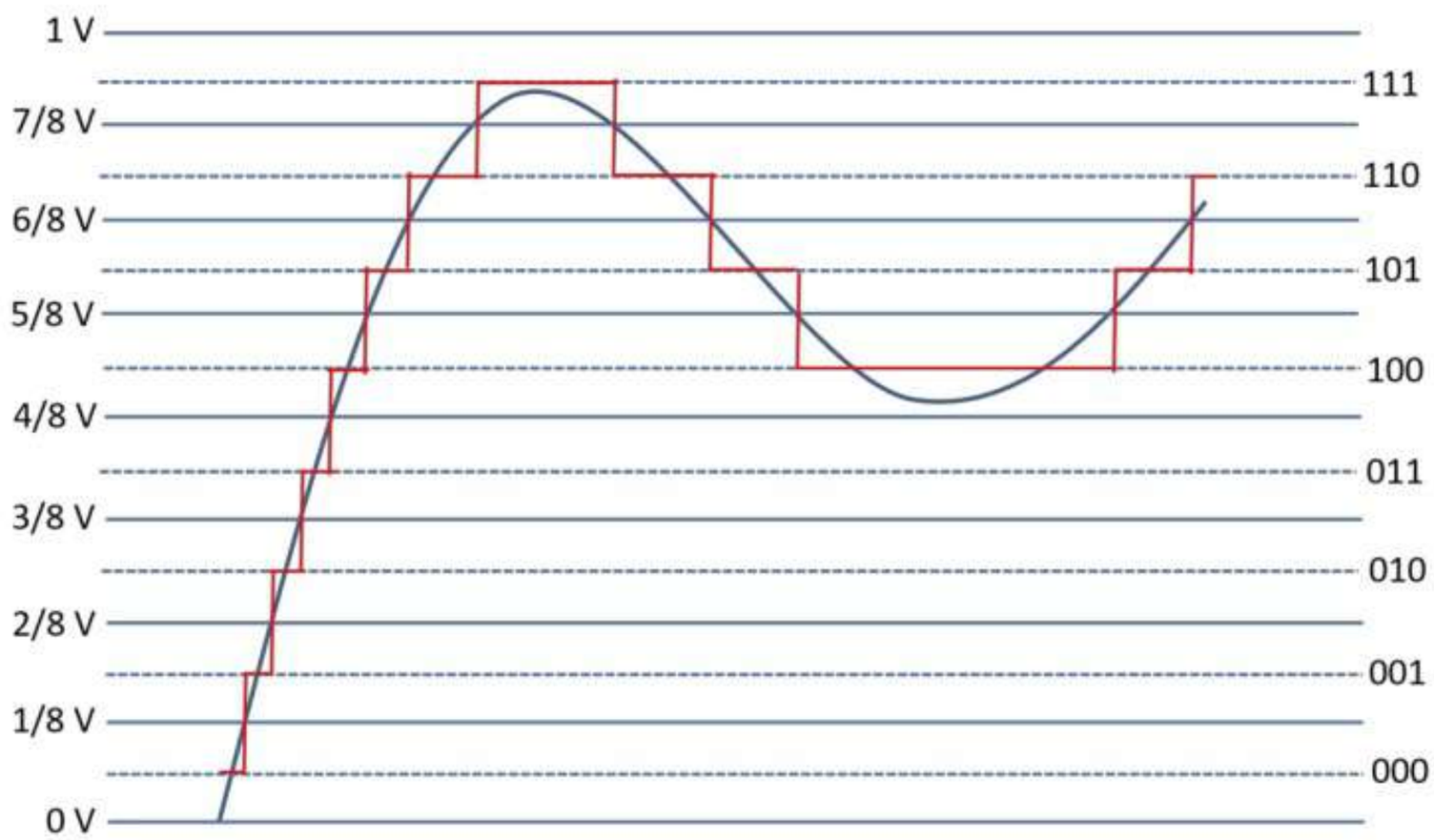
Practical Sample and hold circuit

- The switch is controlled by a clock generator which makes the switch operate at regular interval as required according to the sampling rate.
- The voltage across the capacitor is applied at the input of the analog-to-digital converter through buffer amplifier A_2.

- The high input impedance of A_2 avoids discharge of capacitor due to the loading effect of A/D converter.
- The accuracy of the circuit depends upon the holding of the charge in the capacitor, therefore, a capacitor with a very low leakage must be used.
- A capacitor with polycarbonate, polyethylene, or Teflon dielectric is preferred.
- Most of the other capacitors do not retain the stored charge for e sufficiently long duration due to polarization phenomenon.

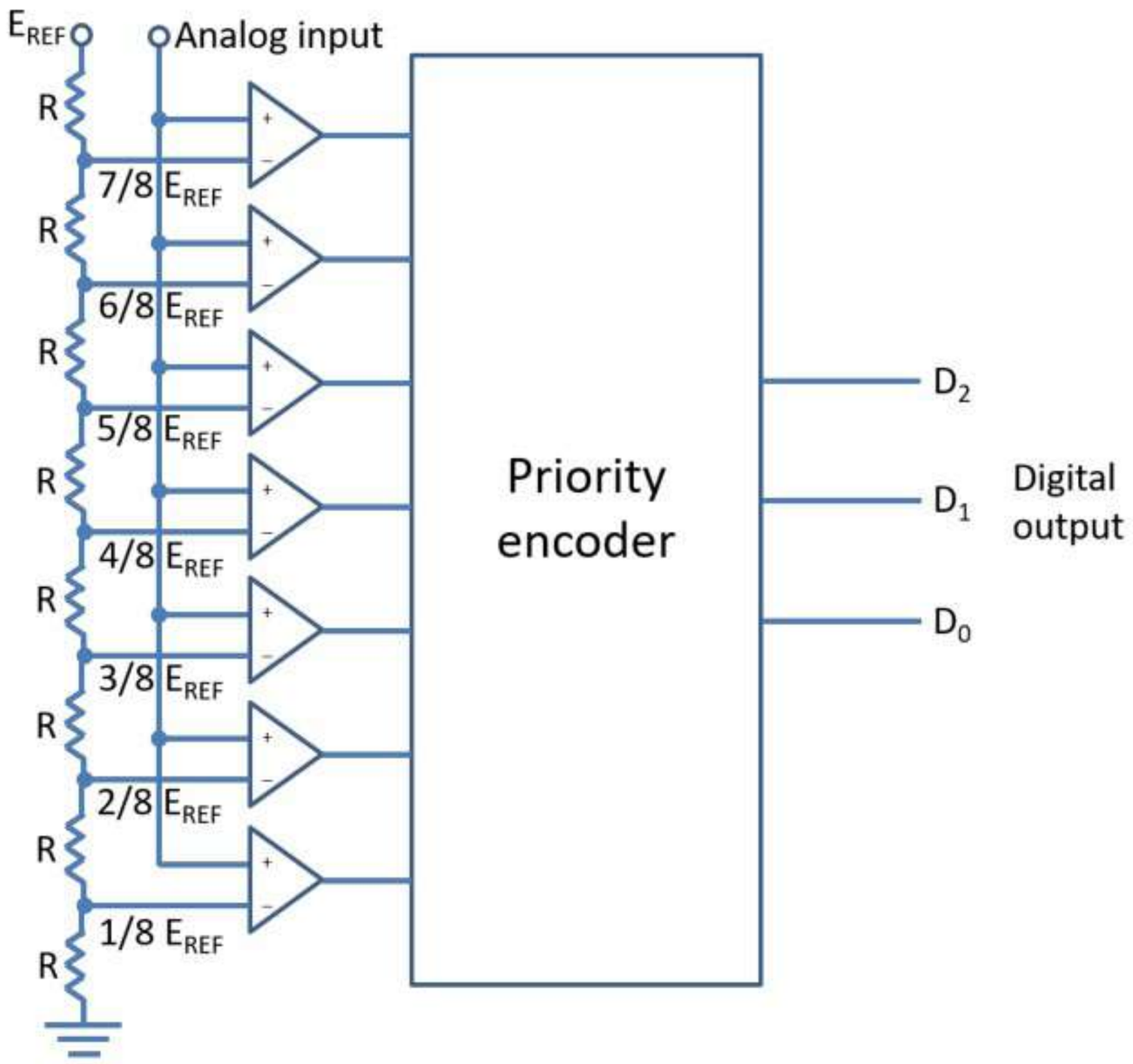
Quantization and encoding

- In a digital-to-analog converter, the possible number of digital inputs is fixed.
- For example, in a 3-bit D/A converter, there are 8 possible inputs.
- In contrast, in an analog-to-digital converter, the input analog voltage, can have any value in a range, but the digital output can have only 2^N discrete values for an N-bit A/D converter.
- Therefore, the whole range of analog voltage is required to be represented suitably in 2^N intervals.
- This process is known as quantization.
- Each interval is then assigned a unique N-bit binary code, which is referred to as encoding.



- Consider an analog voltage in the range of 0 to V and a 3-bit digital output for any voltage in this range.
- Let us divide the whole range of analog voltage in 8 intervals (3-bit output) of the size S = V/8.
- Each interval is assigned a 3-bit binary value.
- The intervals of the analog voltage and their corresponding digital values assigned are shown in above figure.
- From this, we observe that the whole range of voltage in an interval is represented by only one digital value.
- Therefore, there is an error referred to as quantization error, involved in this process of quantization.
- In this case, the maximum quantization error for any analog input voltage V_x in the given range is V/8.

Parallel comparator type ADC (Flash type ADC)



- The flash (or simultaneous or parallel) type A/D converter is the fastest type of A/D converter.
- This type of converter utilizes the parallel differential comparators that compare reference voltages with the analog input voltage.
- The main advantage of this type of converter is that the conversion time is less, but the disadvantage is that, an n-bit converter of this type requires 2^n -1 comparators, 2^n resistors, and a priority encoder.
- Figure shows a 3-bit flash type A/D converter which requires 7(= 2^3 - 1) comparators.
- A reference voltage E_{ref} is connected to a voltage divider that divides it into seven equal increment levels.
- Each level is compared to the analog input by a voltage comparator.
- For any given analog input, one comparator and all those below it will have a HIGH output.
- All comparator outputs are connected to a priority encoder, which produces a digital output corresponding to the input having the highest priority, which in this case is the one that represents the largest input.
- Thus, the digital output represents the voltage that is closest in value to the analog input.
- The voltage applied to the inverting terminal of the uppermost comparator in Figure is (by Voltage divider action),

$$\left(\frac{7R}{7R+R}\right) X\ E_{REF} = \frac{7}{8}\ X\ E_{REF}$$

Similarly, the voltage applied to the inverting terminal of the second comparator is

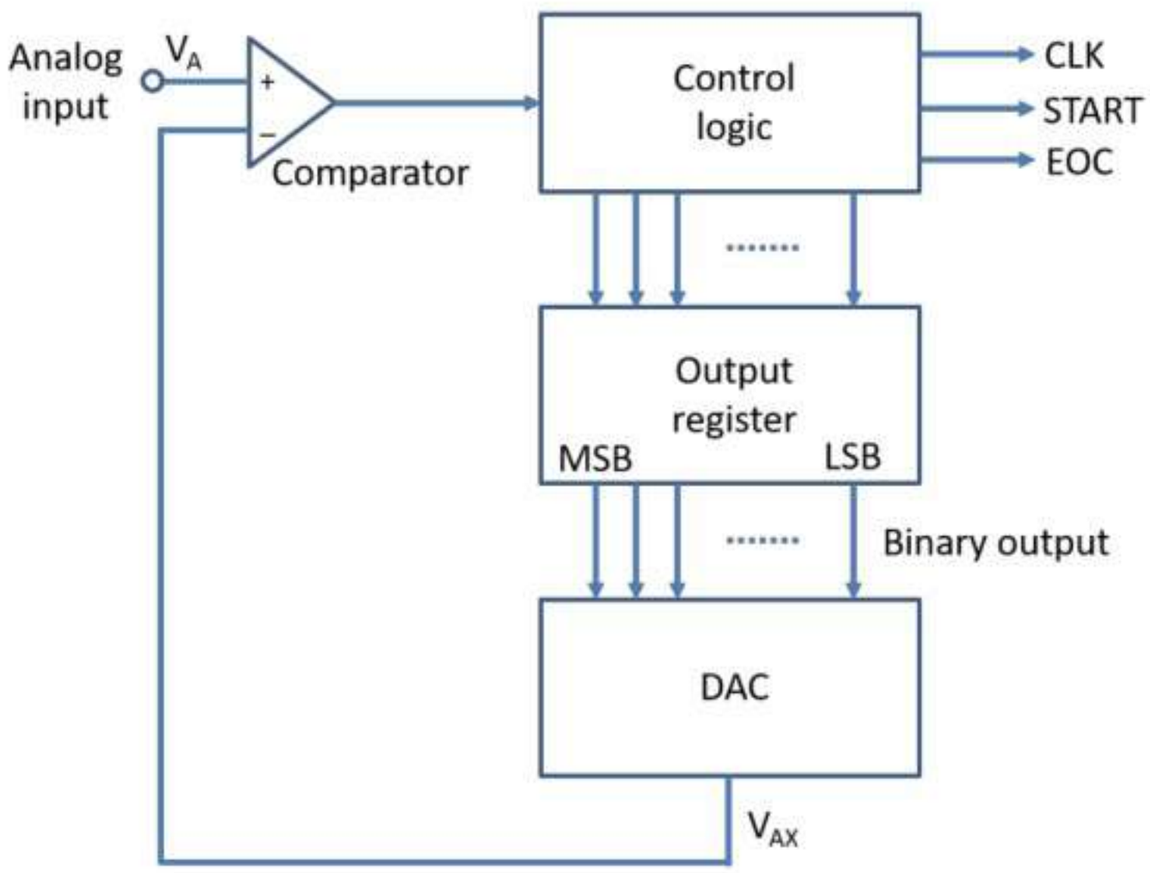
$$\left(\frac{6R}{6R+R}\right) X\ E_{REF} = \frac{6}{8}\ X\ E_{REF}$$

and so forth. The increment between voltages is $\frac{1}{8}\ X\ E_{REF}$.

- The flash converter uses no clock signal, because there is no timing or sequencing period.
- The conversion takes place continuously. The only delays in the conversion are in the comparators and the priority encoders.

Successive approximation type ADC

- The successive-approximation converter is one of the most widely used types of ADC.
- It has a much shorter conversion time than the other types, with the exception of the parallel type.
- It also has a fixed conversion time which is not dependent on the value of the analog input.



- Figure shows a basic block diagram of a 4-bit successive-approximation type ADC.
- It consists of a DAC, an output register, a comparator, and control circuitry or logic.
- The basic operation is as follows: The bits of DAC are enabled one at a time, starting with the MSB.
- As each bit is enabled, the comparator produces an output that indicates whether the analog input voltage is greater or less than the output of the DAC V_{AX}.
- If the D/A output is greater than the analog input, the comparator output is LOW, causing the bit in the control register to reset.
- If the D/A output is greater than the analog input, the comparator output is HIGH, and the bit is retained in the control register.
- The system enables the MSB first, then the next significant bit, and so on.
- After all the bits of the DAC have been tried, the conversion cycle is complete.
- The processing of each bit takes one clock cycle; so, the total conversion time for an N-bit SA-type ADC will be N clock cycle.

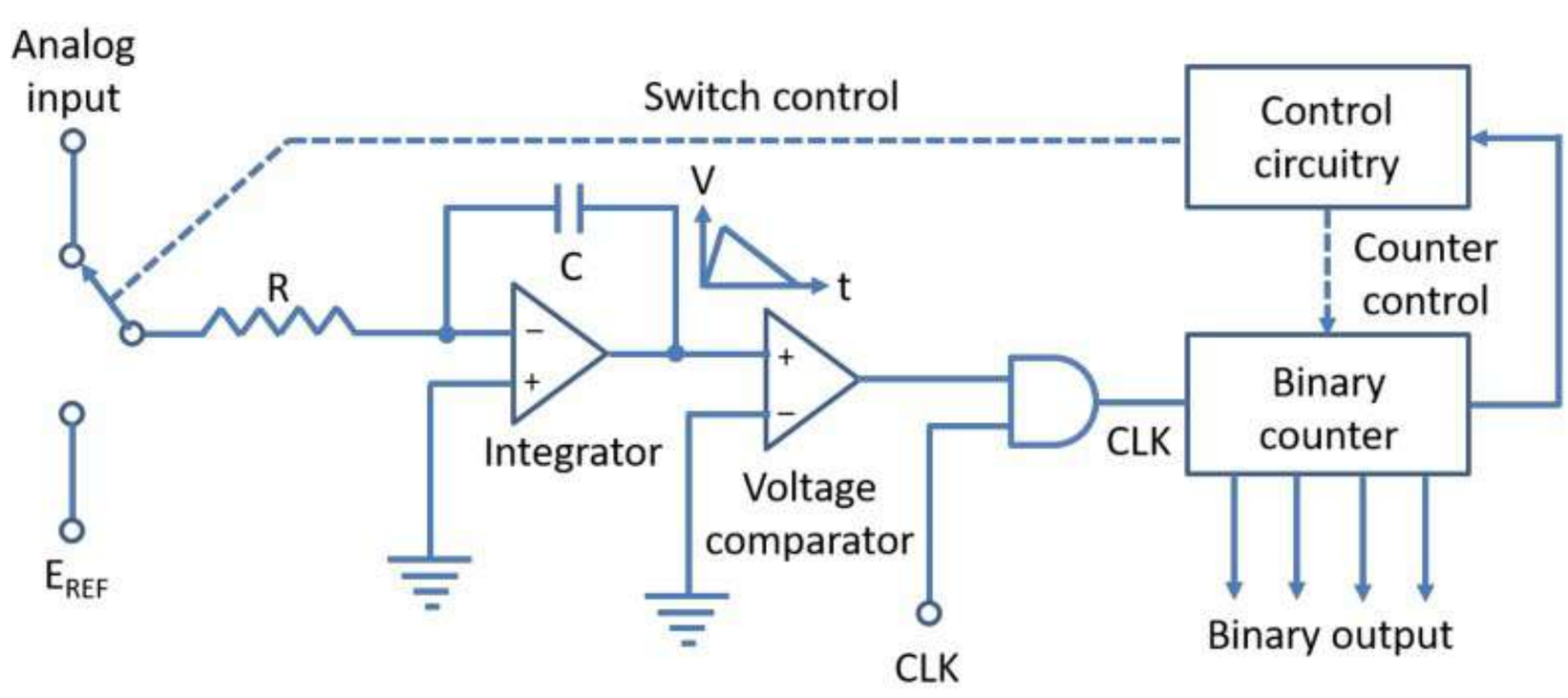
Example

- Let us assume that the output of the DAC ranges from 0 V to 15 V as its binary input ranges from 0000 to 1111, with 0000 producing 0 V and 0001 producing 1 V, and so on.
- Suppose that the unknown analog input voltage VA is 10.3 V.
- On the first clock pulse, the output register is loaded with 1000, which is converted by the DAC to 8 V.

- The voltage comparator determines that 8 V is less than the analog input (10.3 V); so, the control logic retains that bit.
- On the next clock pulse, the control circuitry causes the output register to be loaded with 1100.
- The output of the DAC is now 12 V, which the comparator determines as greater than the analog input.
- Therefore, the comparator output goes LOW. The control logic clears that bit; so, the output goes back to 1000.
- On the next clock pulse, the control circuitry causes the output register to be loaded with 1010.
- The output of the DAC is now 10 V, which the comparator determines as less than the analog input.
- Thus, on the next clock pulse, the control logic causes the output register to be loaded with 1011.
- The output of the DAC is now 11 V, which the comparator determines as greater than the analog input; so, the control logic clears that bit.
- Now the output of the ADC is 1010 which is the nearest integer value to the input (10.3 V).
- At this point, all of the register bits have been processed, the conversion is complete and the control logic activates its EOC output to signal that the digital equivalent of V_A is now in the output register.

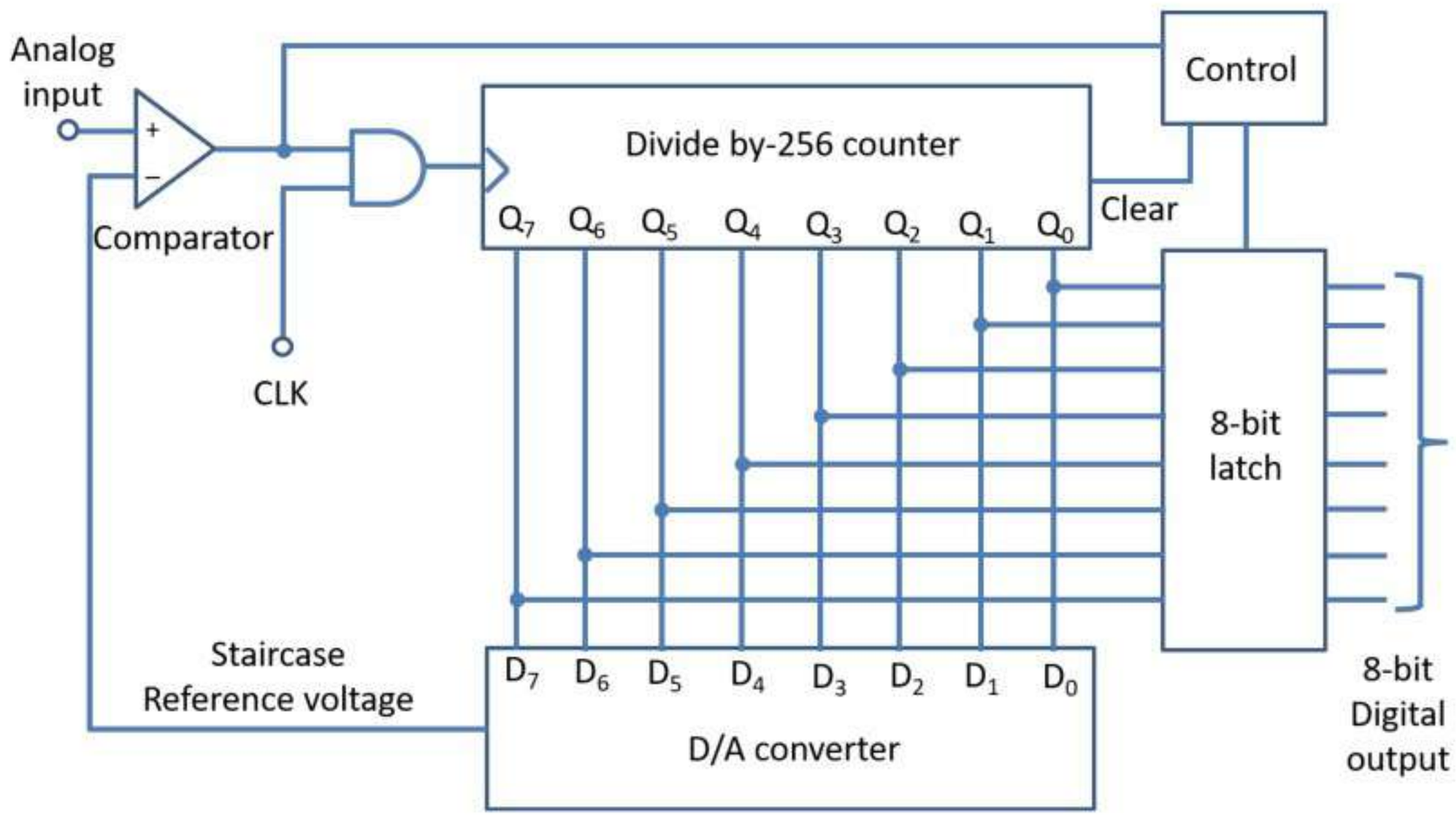
Dual-slope type ADC

- The dual-slope converter is one of the slowest converters, but is relatively inexpensive because it does not require precision components such as a DAC or VCO.
- Another advantage of the dual-slope ADC is its low sensitivity to noise, and to variations in its component values caused by temperature changes.
- Because of its large conversion time, the dual-slope ADC is not used in any data acquisition applications.
- The major applications of this type of converter are in digital voltmeters, multimeters, etc. where slow conversions are not a problem.
- Since it is not fast enough, its use is restricted to signals having low to medium frequencies.
- A dual-slope ADC uses an operational amplifier to integrate the analog input.
- The output of the integrator is a ramp, whose slope is proportional to the input signal E_{in}, since the components R and C are fixed.
- If the ramp is allowed to continue for a fixed time, the voltage it reaches in that time, depends on the slope of the ramp and, therefore, on the value of E_{in}.



- The basic principle of me integrating ADC is that, the voltage reached by the ramp controls the length of time that the binary counter is allowed to count.
- Thus, a binary number proportional to the value of E_{in} is obtained.
- In the dual-slope ADC, two integrations are performed.
- Figure shows the functional block diagram of a dual-slope ADC.
- Assume that the counter is reset and the output of the integrator is zero.
- A conversion begins with the switch connected to the analog input.
- Assume that the input is a negative voltage and is constant for a period of time; so, the output of the integrator is a positive ramp.
- The ramp is allowed to continue for a fixed time and the voltage it reaches in that time is directly dependent on the analog input.
- The fixed time is controlled by sensing the time when the counter reaches a particular count.
- At that time, the counter is reset and the control circuitry causes the switch to be connected to a reference voltage E_{REF}, having a polarity opposite to that of the analog input; in this case a positive reference voltage.
- Therefore, the output of the integrator is a negative going ramp, beginning from the positive value it reached during the first integration.
- The AND gate is enabled and the counter starts counting.
- When the ramp reaches 0 V, the voltage comparator switches to LOW, inhibiting the clock pulses and the counter stops counting.
- The binary count is latched, thus, completing one conversion.
- The count it contains at that time is proportional to the time required for the negative ramp to reach zero, which is proportional to the positive voltage reached during the first integration, which in turn is proportional to the analog input.
- The accuracy of the converter does not depend on the values of the integrator components or upon any changes in them.
- The accuracy does depend on E_{REF}; so, the reference voltage should be very precise.

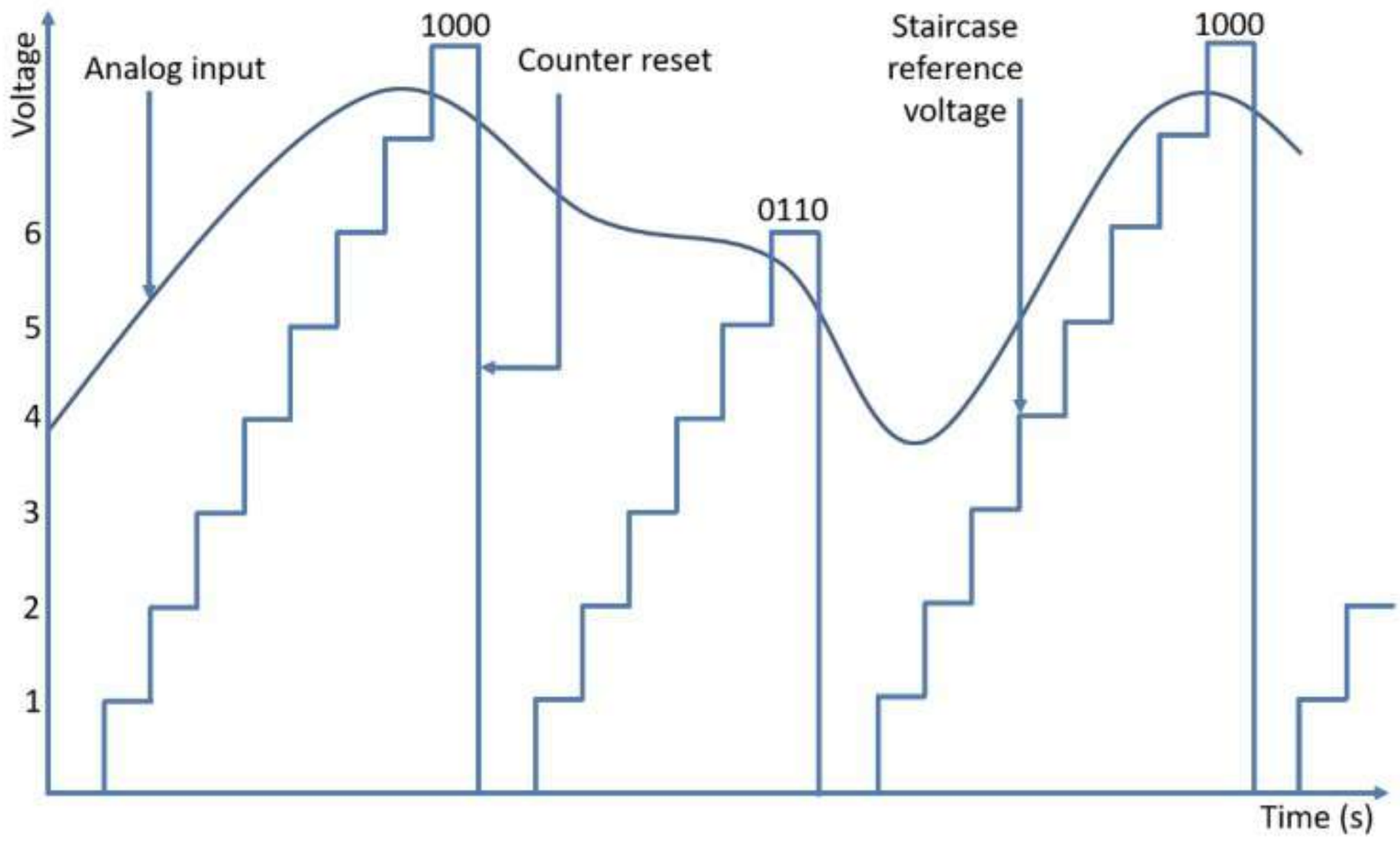
Counter type ADC



- This is the simplest type of the A/D converter.
- It employs a binary counter, a voltage comparator, a control circuit, an AND gate, latches, and a D/A converter as shown in above figure.
- It is also called a digital ramp ADC, because the waveform at the output of the DAC is a step-by-step ramp (actually a staircase).
- The analog signal to be converted is applied to the non-inverting terminal of the op-amp comparator.
- The output of the DAC is applied to the inverting terminal of the op-amp.
- Whenever the analog input signal is greater than the DAC output, the output of the op-amp is HIGH and whenever the output of the DAC is greater than the analog signal, the output of the comparator is LOW.
- The comparator output serves as an active-low end of the conversion signal.
- Assume that initially the counter is reset and, therefore, the output of the DAC is zero.
- Since the analog input is larger than the initial output of the DAC, the output of the comparator is HIGH and, therefore, the AND gate is enabled and, so, the clock pulses are transmitted to the counter and the counter advances through its binary states.
- These binary states are converted into reference analog voltage (which is in the form of a step) by the DAC.
- The counter continues to advance from one state to the next, producing successively larger steps in the reference voltage.
- When the staircase output voltage reaches the value of the analog signal, the comparator outputs a LOW, and the AND gate is disabled; so, the clock pulses do not reach the counter and the counter stops.
- The count it reached is the digital output proportional to the analog input.
- The control logic loads the binary count into the latches and resets the counter, thus, beginning another count sequence to sample the input value. The cycle thus repeats itself.
- The resolution of this ADC is equal to the resolution of the DAC it contains.
- The resolution can also be thought of as the built-in error and is often referred to as the quantization error. Thus,

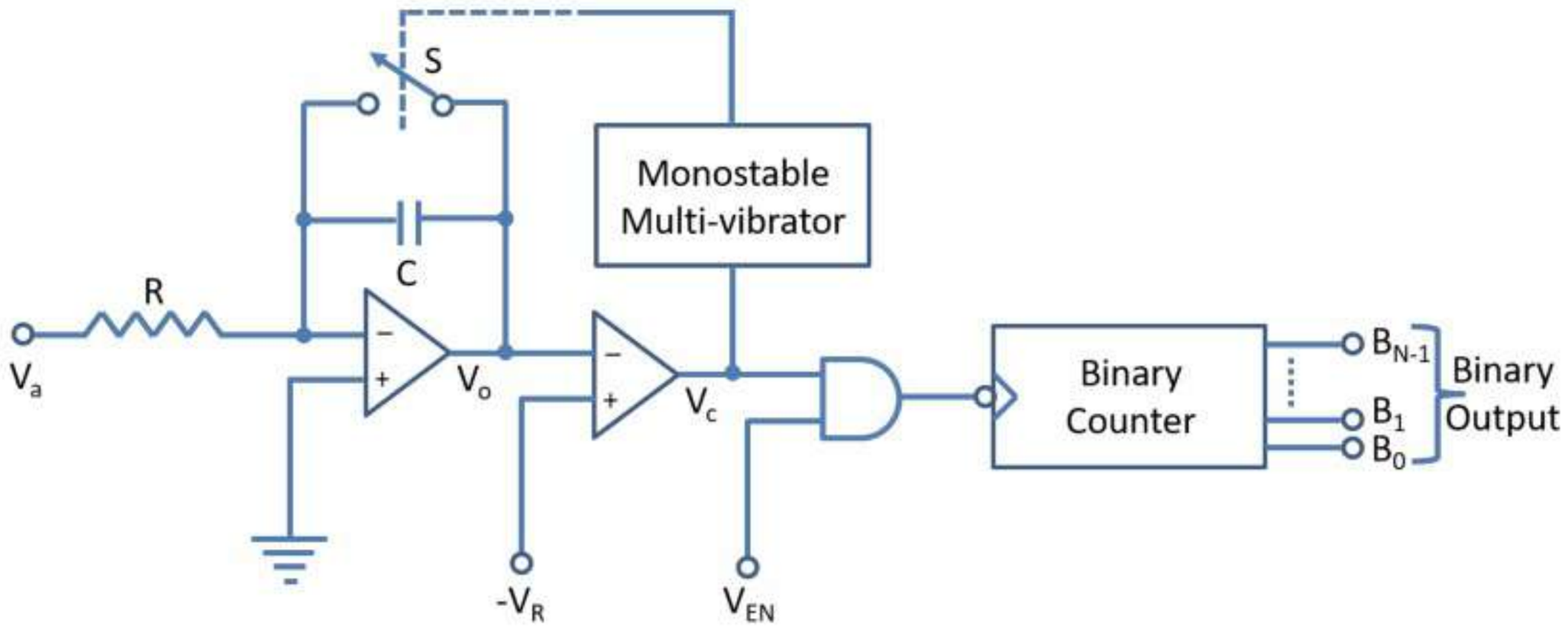
$$Resolution = \frac{FSR}{2^N}$$

where FSR is the full-scale reading and N is the number of bits in the counter.



- As in the DAC, the accuracy is not related to the resolution, but is dependent on the accuracy of the circuit components such as comparator, the DAC's precision resistors, etc.
- Figure above illustrates the output of a 4-bit DAC in an ADC over several cycles when the analog input is a slowly varying voltage.
- The principal disadvantage of this type of converter is that, the conversion time depends on the magnitude of the analog input.
- The larger the input, the more will be the number of clock pulses that must pass to reach the proper count, and, therefore, the larger will be the conversion time.
- For each conversion, the counter has to start from reset only and count up to the point at which the staircase reference voltage reaches the analog input voltage.
- This type of converter is considered quite slow in comparison with the other types.

A to D conversion using voltage to frequency conversion



- An analog voltage can be converted into digital form, by producing pulses whose frequency is proportional to the analog voltage.
- These pulses are counted by a counter for a fixed duration and the reading of the counter will be proportional to the frequency of the pulses, and hence, to the analog voltage.
- A voltage-to-frequency converter is shown in below figure.
- The analog voltage V_a is applied to an integrator whose output is applied at the inverting input terminal of a comparator.
- The non-inverting input terminal of the comparator is connected to a reference voltage $-V_R$.
- Initially, the switch S is Open and the voltage V_o decreases linearly with time ($V_o = -V_a t/\tau$).
- When the decreasing V_o reaches $-V_R$ at t = T, the comparator output V_C goes HIGH.
- This is used to close the switch S through a monostable multivibrator.
- When the switch S is closed, the capacitor C discharges, thereby returning the integrator output V_o to 0.
- Since the pulse width of the waveform V_a is very small, a monostable multivibrator is used to keep the switch S closed for a sufficient time to discharge the capacitor completely.
- The rate at which the capacitor discharges depends upon the resistance of the switch.
- Let the pulse width of the monostable multivibrator be T_d. Therefore, the switch S remains closed for T_d after which it opens and V_o starts decreasing again.
- If the integration time $T \gg T_d$, the frequency of the waveform V_o and V_C is given by

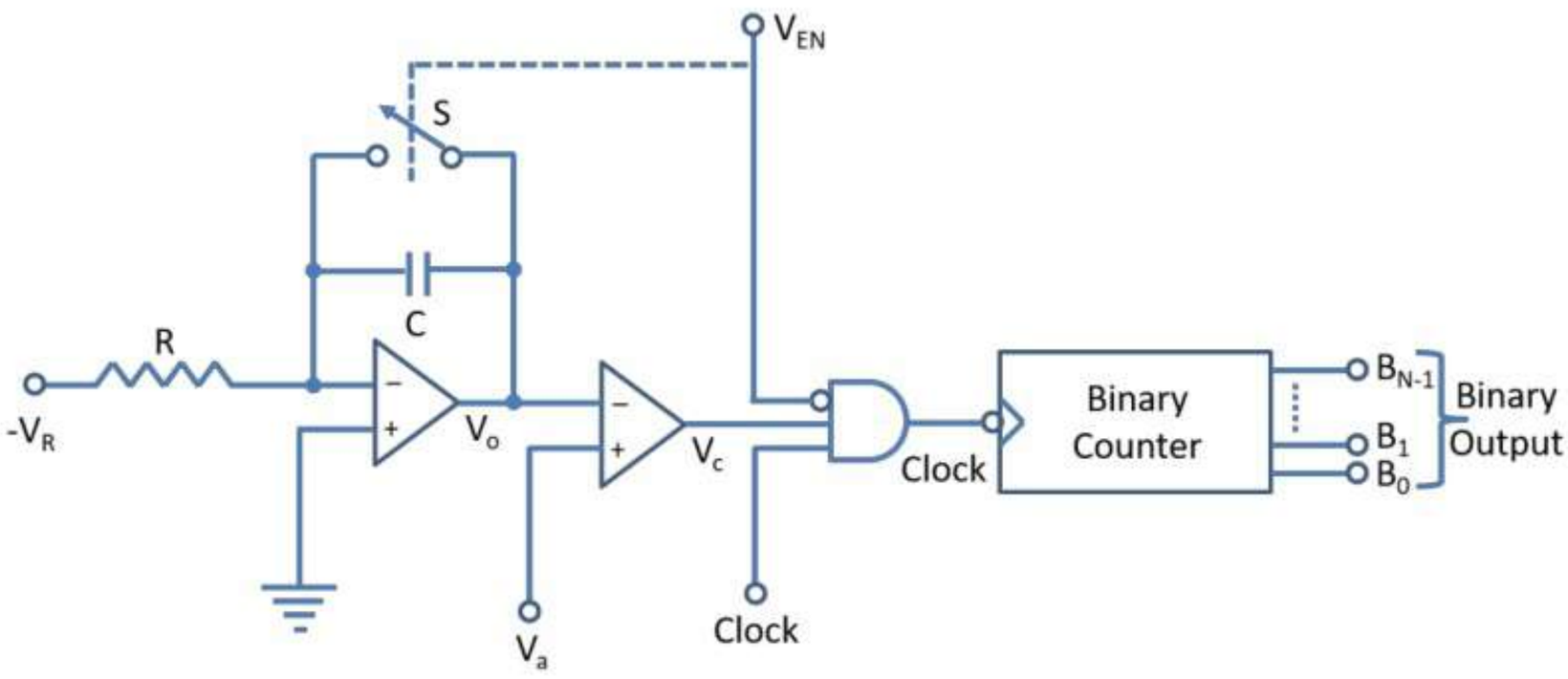
$$f = \frac{1}{T + T_d} = \frac{1}{T} = \frac{1}{\tau}\frac{V_a}{V_R}$$

- Thus, we obtain an output waveform whose frequency is proportional to the analog input voltage.
- An A/D converter using the voltage-to-frequency (V/F) converter is shown in figure.
- The output of the V/F converter is applied at the clock (CK) input of a counter through an AND gate. The AND gate is enabled for a fixed time interval T_1.
- The reading of the counter at t = T is given by

$$n = fT_1 = \frac{1}{\tau}\frac{V_a}{V_R}T_1$$

which is proportional to V_a.

A to D conversion using voltage to time conversion



- In an A/D converter using V/F converter, the cycles of a variable-frequency source are counted for a fixed period.
- Alternatively, it is possible to make an A/D converter by counting the cycles of a fixed-frequency source for a variable period.
- For this, the analog voltage is required to be converted to a proportional time period.
- An A/D converter, which operates on this principle, is shown in figure.
- A negative reference voltage $-V_R$ is applied to an integrator, whose output is connected to the inverting input terminal of the comparator.
- The analog voltage V_a is applied at the non-inverting input terminal of the comparator.
- The output of the comparator V_C is at logical level 1 as long as the output of the integrator V_o is less than V_a.
- When V_o crosses V_a at t = T, VC goes LOW.
- The AND gate is enabled when V_{EN} is LOW and switch S remains open.
- When V_{EN} goes HIGH, the switch S is closed, thereby discharging the capacitor.
- Also, the AND gate is disabled. When the AND gate is enabled, the clock pulses will reach the clock (CK) input terminal of the counter.
- The output of the counter is the digital output corresponding to V_a.
- The time T is given by

$$T = \frac{\tau}{V_R}V_a$$

which shows that T is proportional to V_a.

The counter reading is n at t = T, then

$$n = f_c T = \frac{f_c \tau}{V_R} V_a$$

where, f_c is the clock frequency. The count n is proportional to V_a.

Specifications for ADC

- Range of input voltage
- Input impedance
- Accuracy
- Conversion time
- Format of digital output