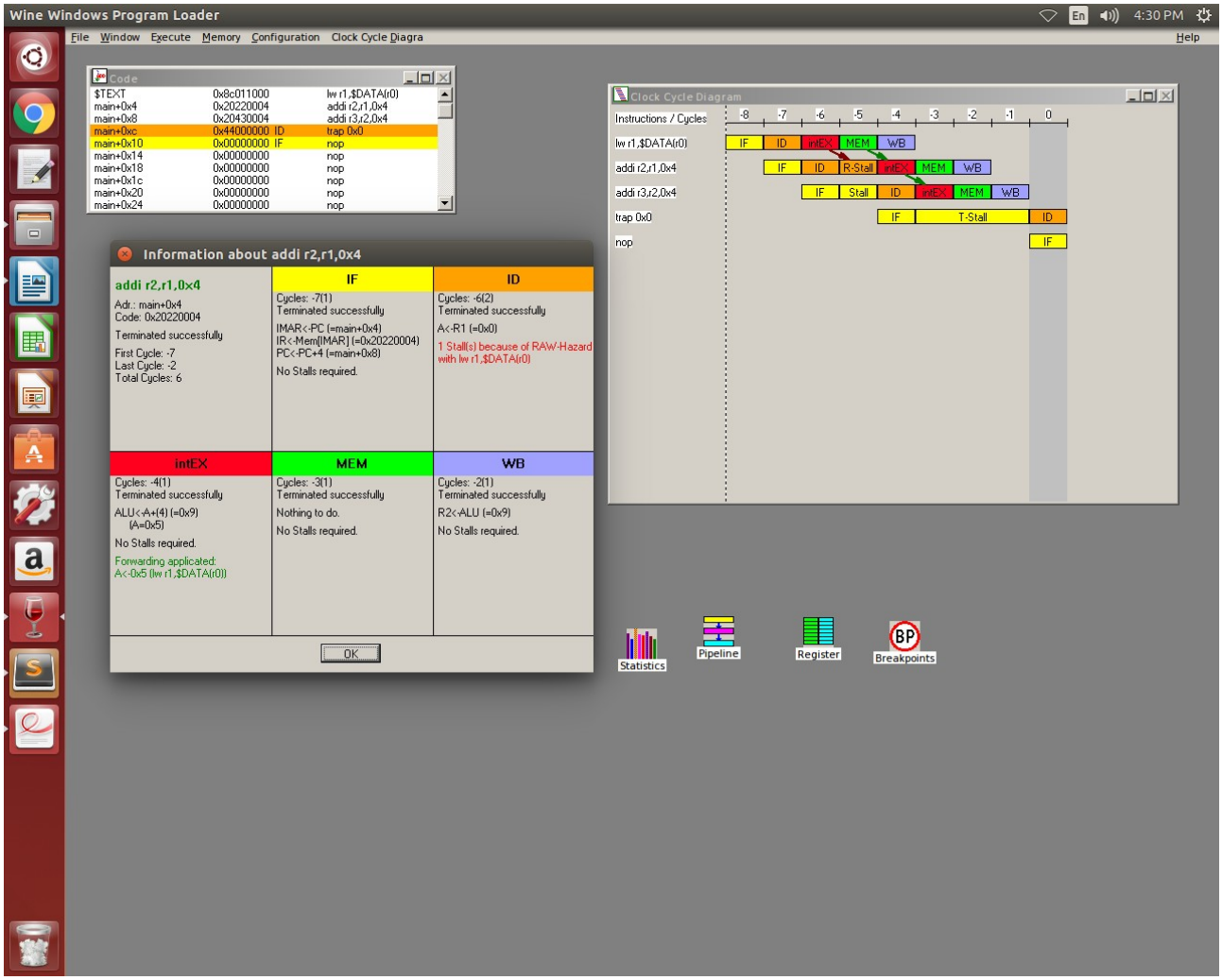
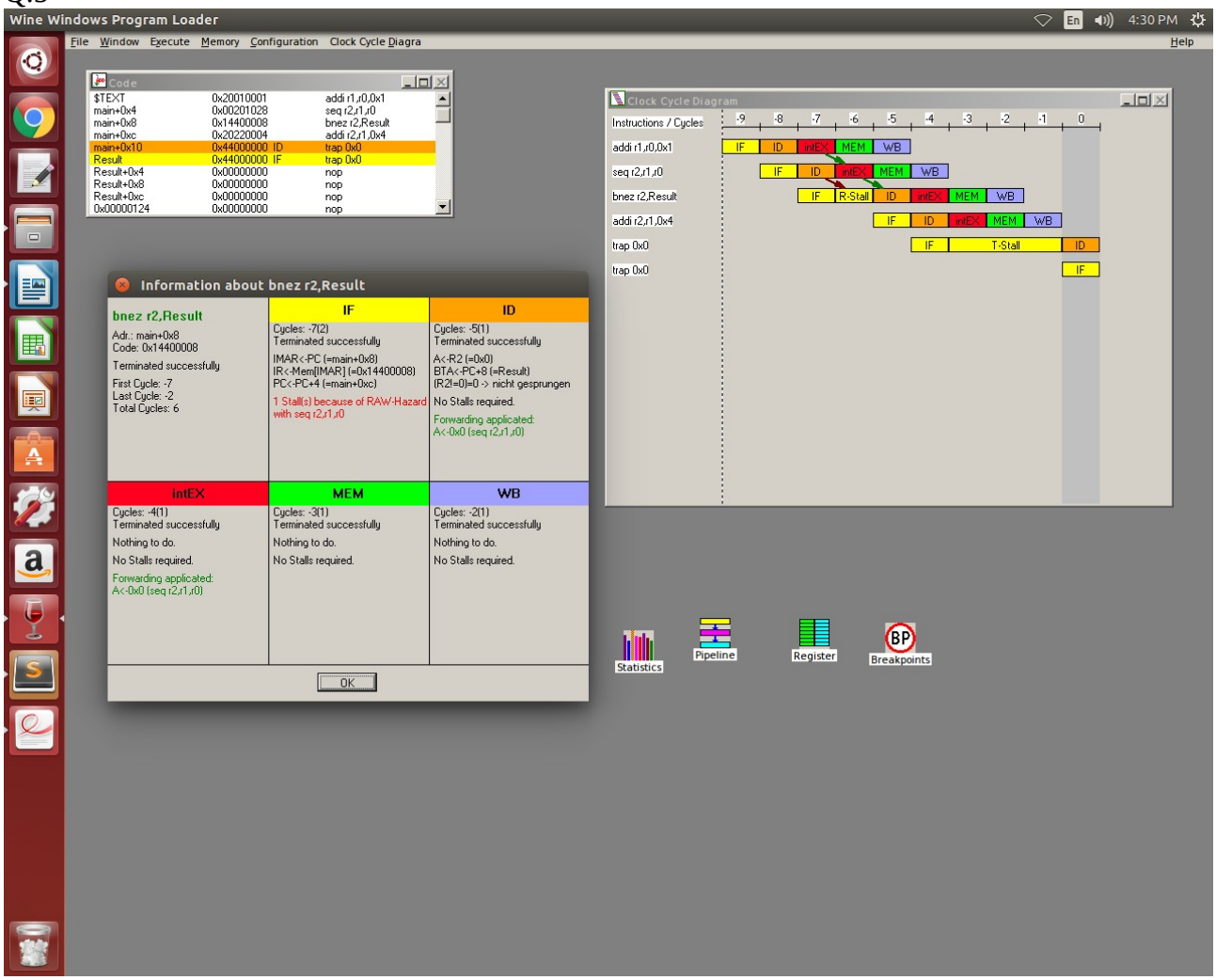
140050002

Q.2




Here because of RAW hazzard, instruction fetch must have stall.

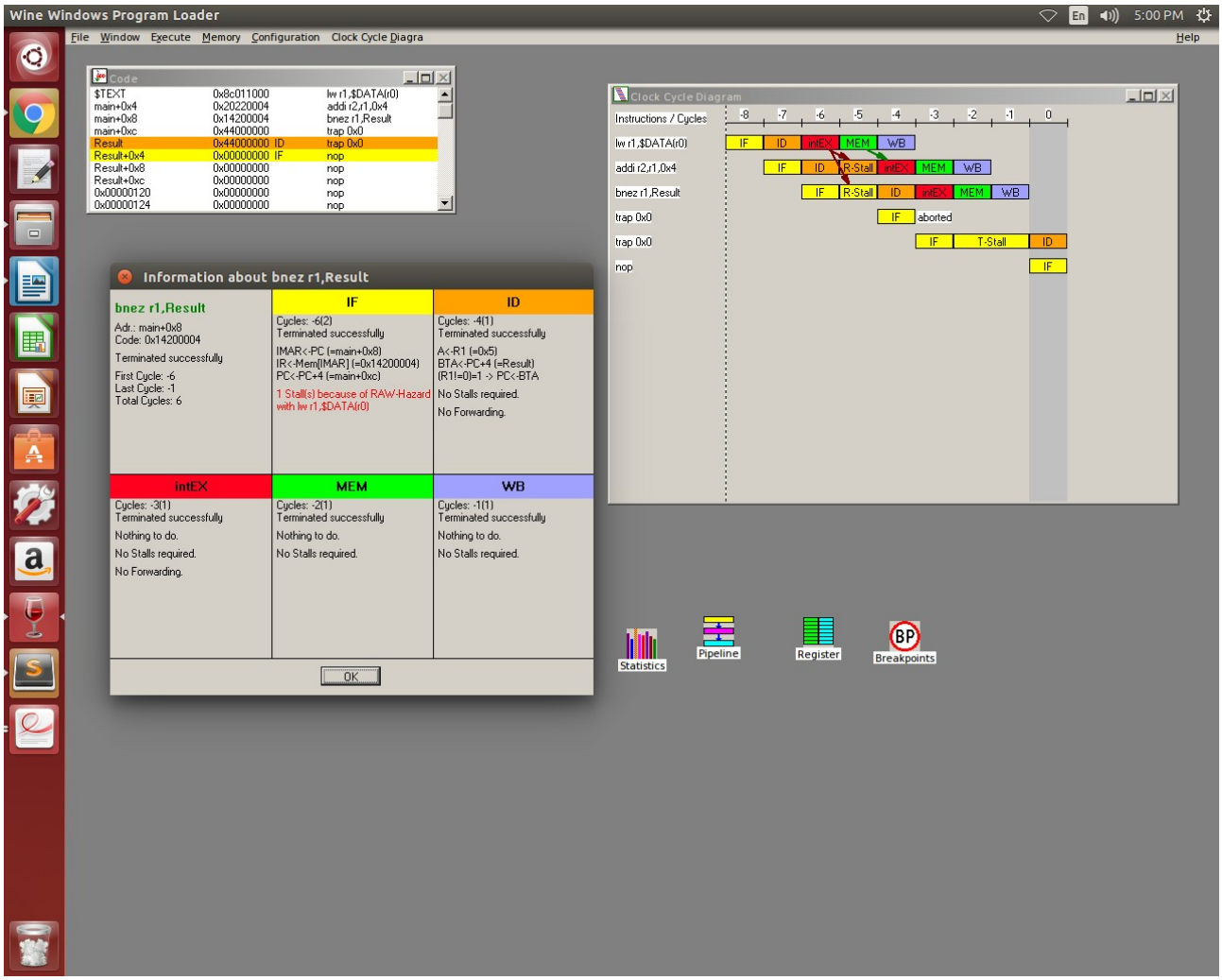
Q.5




Here since operand of benz is calculated in previous cycle in intEX, it's value must be forwarded to ID.

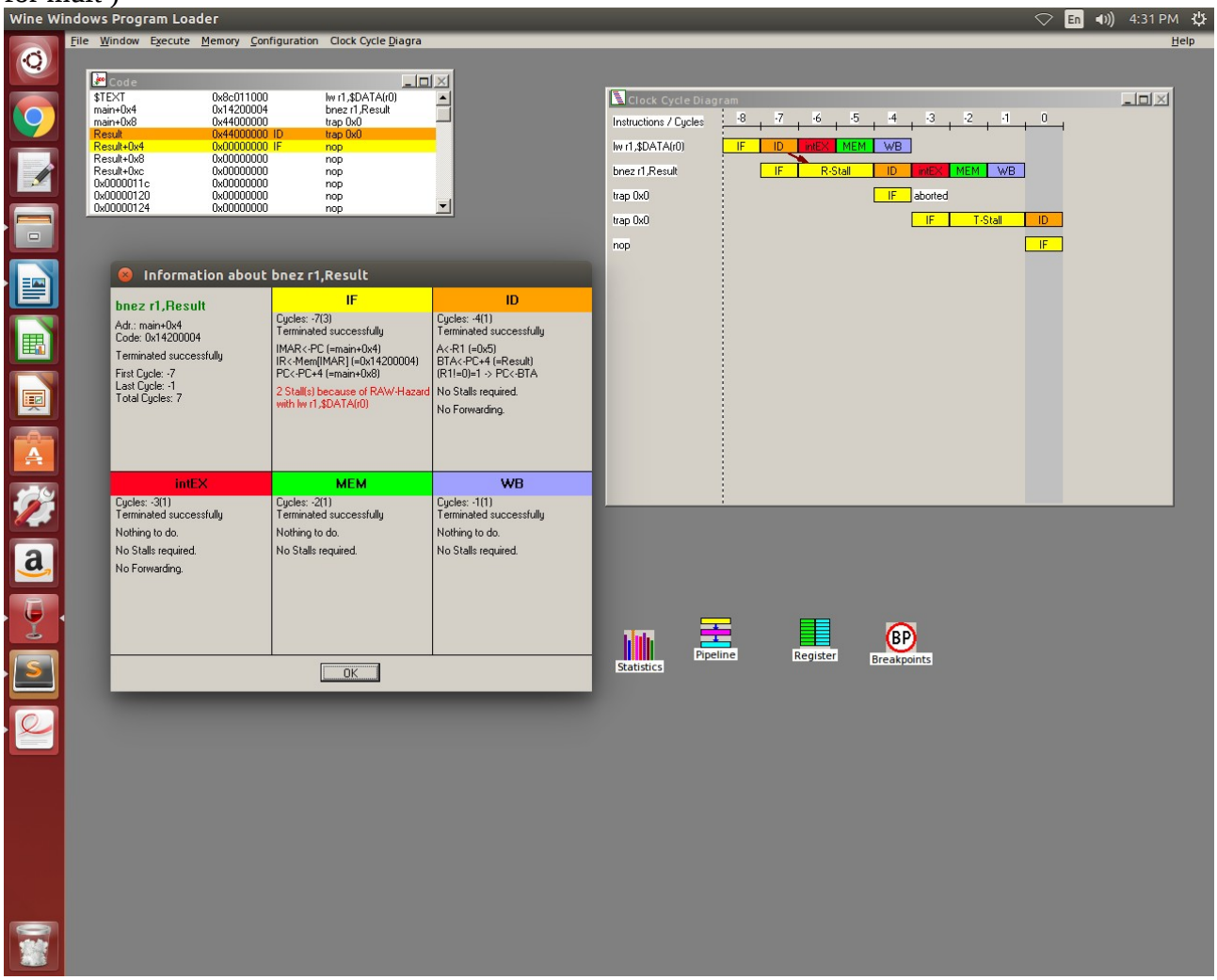
Q.6

NO such program possible.
Since we can use stall and data forwarding, MEM to ID is never required.



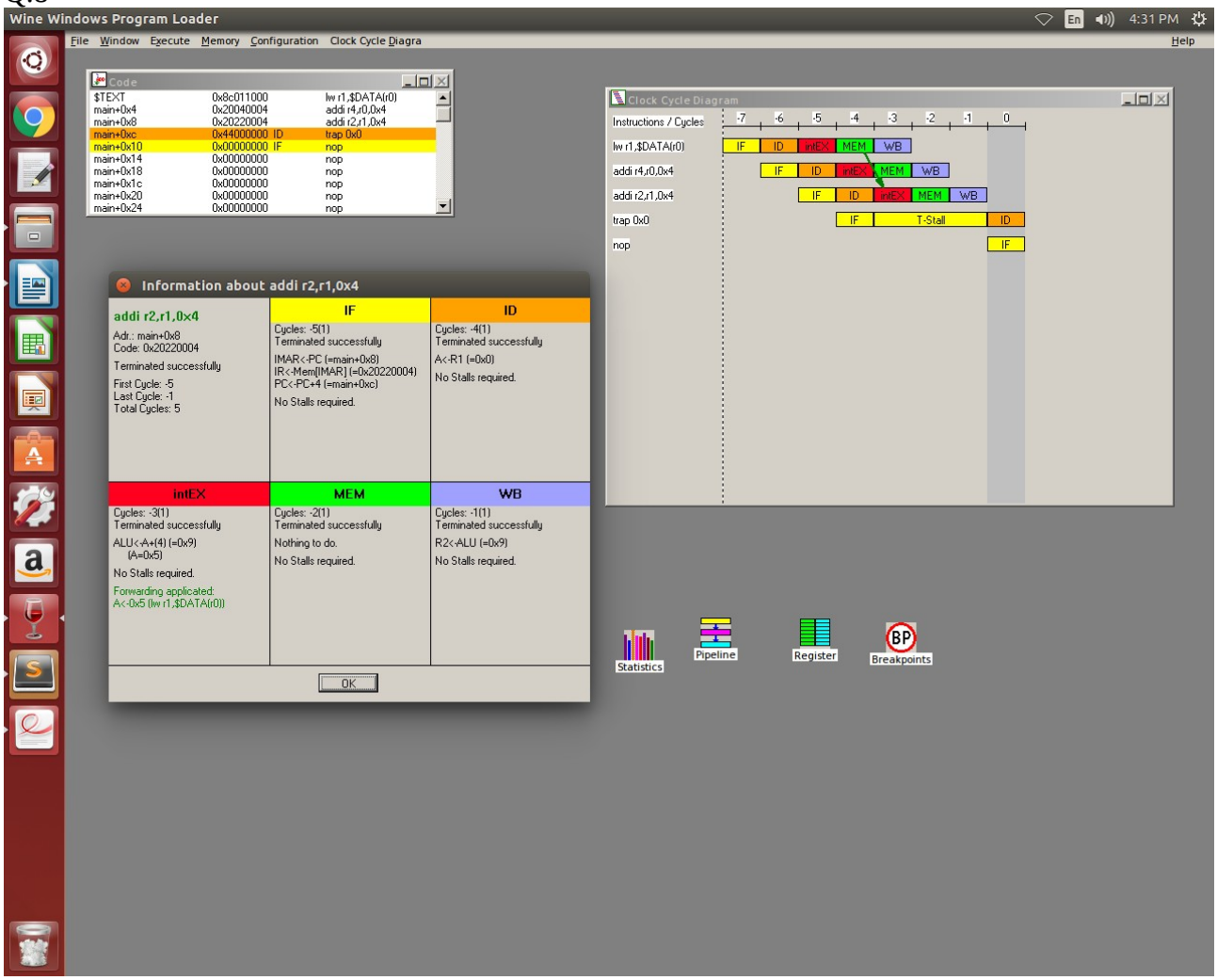

Here MEM to ID is possible but because of RAW hazard, we must stall in IF stage and thus MEM to ID is not required.

Q.7 ( without considering mult ; if mult like Q.9 we can stall as long as number of cycles required for mult )



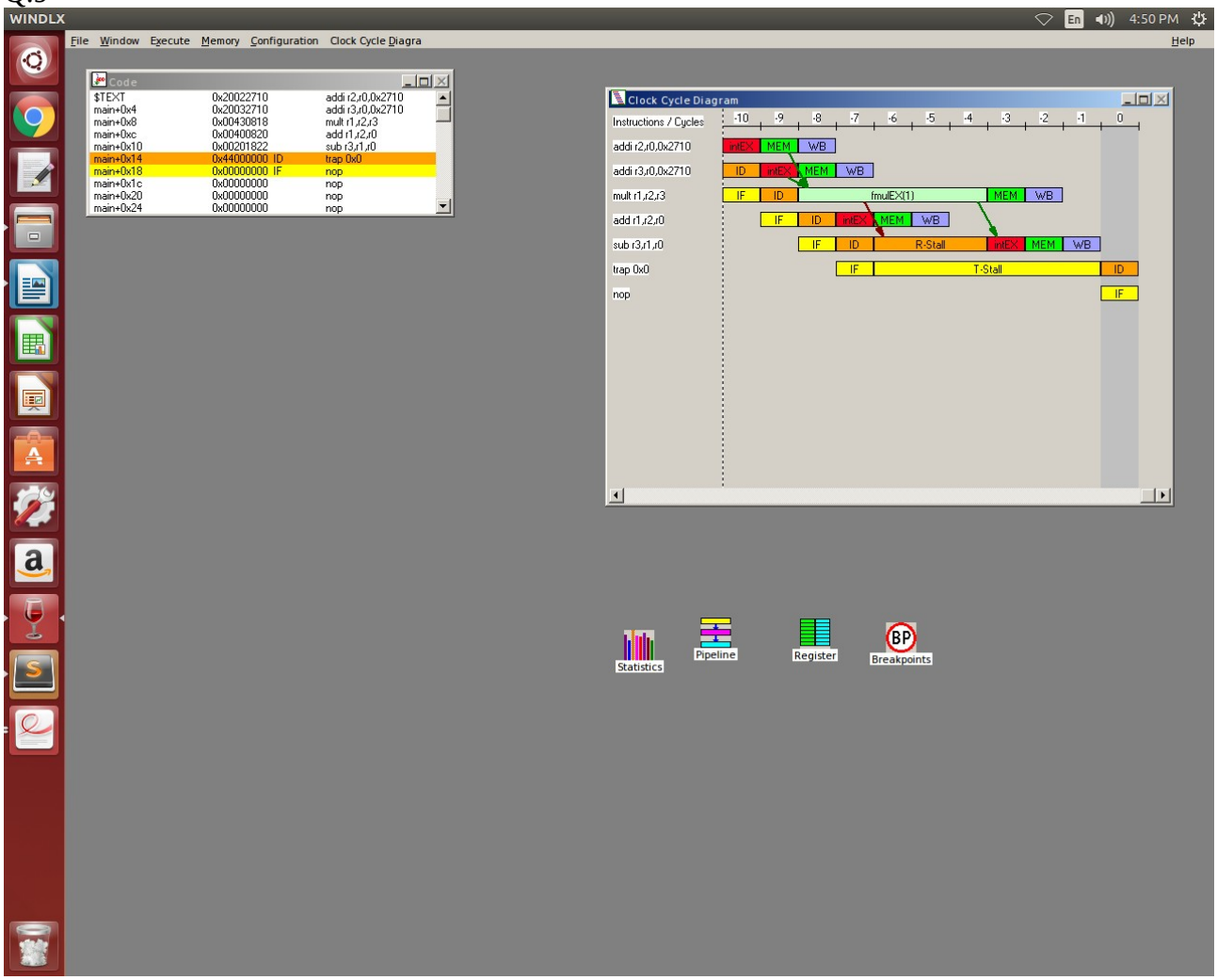

If stall of length 3 between two consecutive instruction were possible, which is only possible if some value depend on value of 3 stages ahead which is not possible since we can always use data forwarding to avoid such situation.

Q.8




If instructions were more than 3 distance apart it must be the case that MEM forwards data to ID which is not possible according to Q.6 or we can use stored data in 5 stage cycle (normal way).

Q.9




Here since multiplication takes large number of cycles and we are writing value in r1 during ADD; there should have been WAW stall but because of some bug it is not present.