# MICROPROCESSOR & EMBEDDED SYSTEMS (Project 1 & Part-4)

Pipeline and Registers & Data Hazard Stall (DHS) and Branch Detection (Br_detect)

Today in the lab, we implemented an Pipeline and Registers, Data Hazard Stall (DHS) and Branch Detection (Br_detect) using Verilog code with predetermined input and output and implementation, tested the module using a testbench, and verified the results using waveform output. as seen in the screenshots that are linked below.
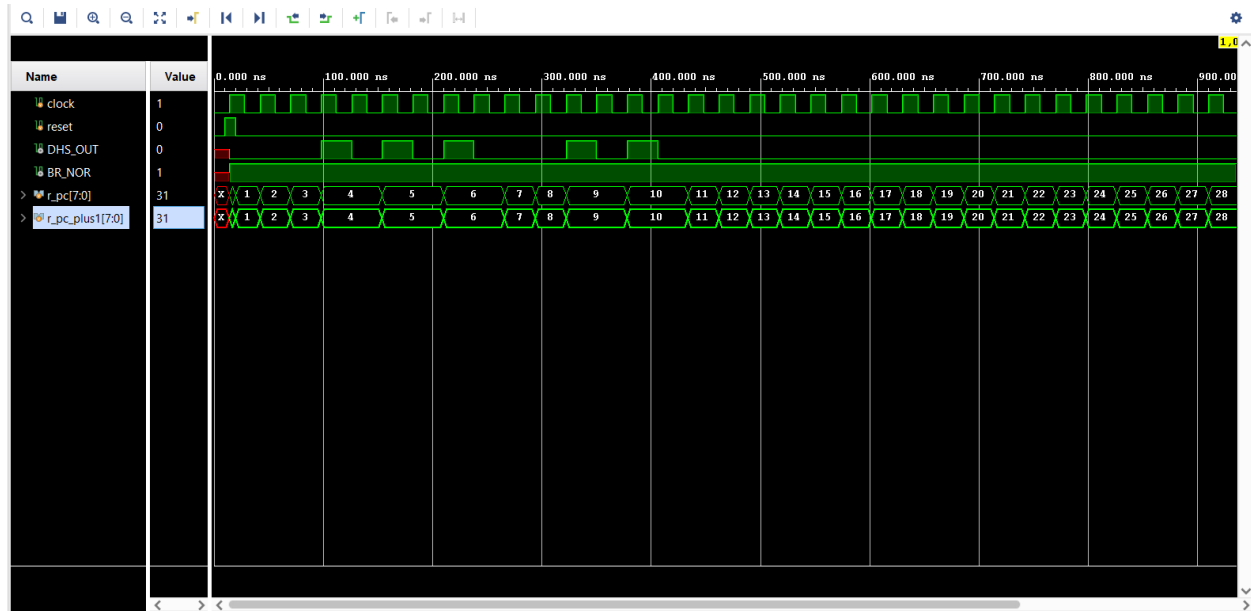
I would design and simulate a synthesizable Top-Level Module as part of my next week's implementation strategy. There are numerous requirements and inputs listed that must be fed to them. Therefore, I am looking forward to working with FPGA Board to check my code in the upcoming lab session on Thursday.