MICROPROCESSOR & EMBEDDED SYSTEMS (Project 1 & Part-3)

Instruction Decoder & Constant Unit

Today in the lab, we implemented an Instruction Decoder & Constant Unit using Verilog code with predetermined input and output and implementation, tested the module using a testbench, and verified the results using waveform output. as seen in the screenshots that are linked below.

In *image 1.1* Here SH is not used till for any operation so that will be Don't care.

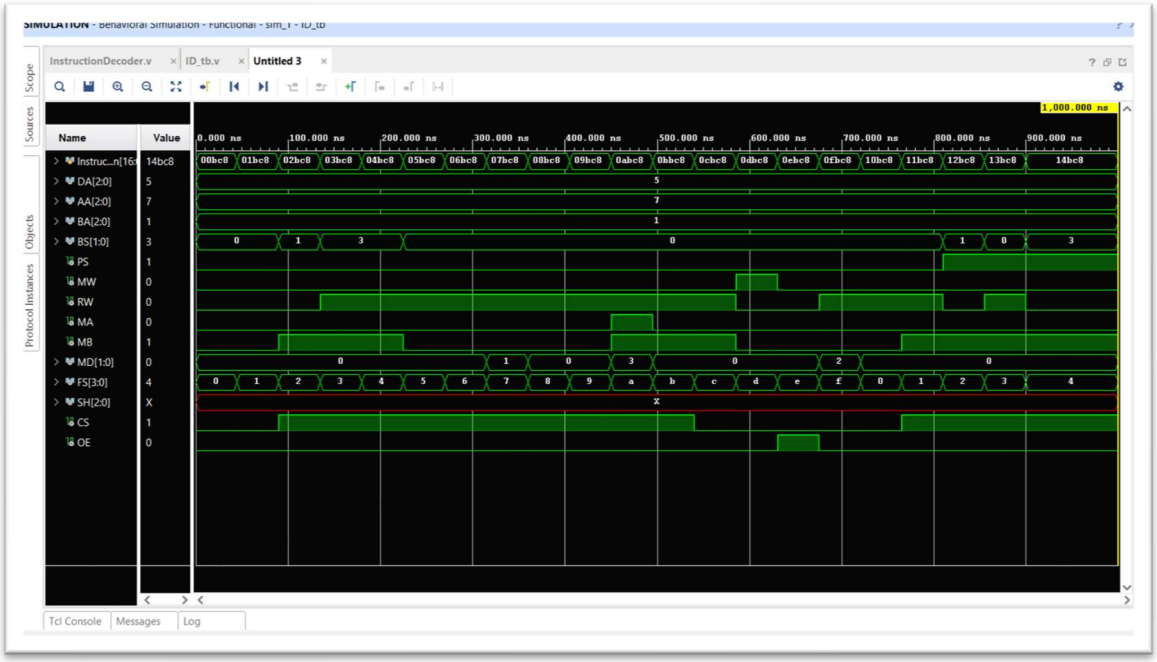

Image 1.1

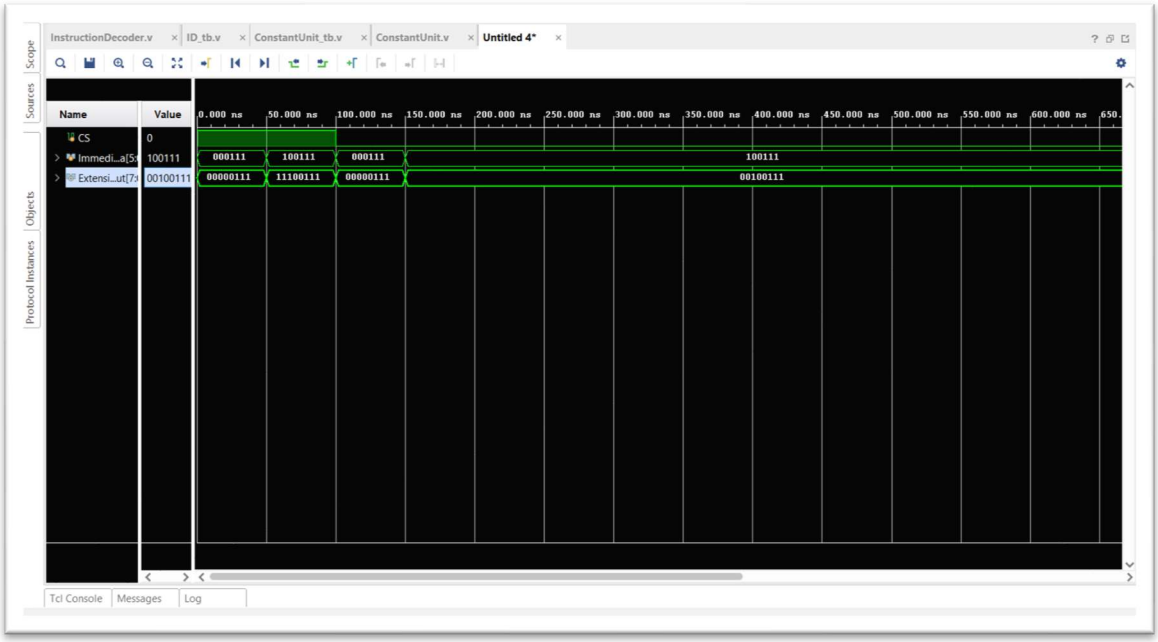

Image 1.2

I would design and simulate a synthesizable Pipeline and Register as part of my next week's implementation strategy. There are numerous requirements and inputs listed that must be fed to them. Therefore, I am looking forward to working with Pipeline and required Register in the upcoming lab session on Thursday.