HW1 Rubric

5+ 5 = 10 marks

Rubric - (10 marks)

Due: 11:55PM 20-Feb-2020

1	**Run AES Cipher on FPGA.**	**5**		
1.1	Making verified synthesizable C code. (Submit synthesis report from Vivado HLS)		1	
1.2	Generate Bit-stream for FPGA. (submit project summary from vivado)		1	
1.3	Check the data for default input and key. (submit screenshot)		1	
1.4	Try two different inputs and two different keys (4 combinations) on FPGA implementation. (submit screenshot of UART input/output)		1	
1.5	Apply your N# as input “N-number, N-number”. (Submit screenshot of UART input/output;) If you N# is N12345678, input is “12 34 56 78 12 34 56 78” (In Hex)		1	
2	**Run AES InvCipher on FPGA.**	**5**		
2.1	Making verified synthesizable C code. (Submit synthesis report from Vivado HLS)		1	
2.2	Generate Bit-stream for FPGA. (submit project summary from vivado)		1	
2.3	Check the data for default input and key. (submit screenshot)		1	
2.4	Try two different inputs and two different keys (4 combinations) on FPGA implementation. (submit screenshot of UART input/output)		1	
2.5	Apply your N# as input “N-number, N-number”. (Submit screenshot of UART input/output;) If you N# is N12345678, input is “12 34 56 78 12 34 56 78” (In Hex)		1	
	Total:	**10**		