HW1 Rubric

5+ 5 = 10 marks

Rubric - (10 marks)

Due: 11:55PM 20-Feb-2020

1	**Run AES Encryption (Cipher) on FPGA.**	**5**		
1.1	Submit RTL and Testbench codes (Verilog/VHDL). (Submit synthesis report from Vivado HLS)		2	
1.2	Generate Bit-stream for FPGA. (submit project summary from vivado)		1	
1.3	Try two different inputs and two different keys (4 combinations) on FPGA implementation. (submit screenshot of UART input/output)		1	
1.4	Apply your N# as input plaintext “N-number, N-number and key = “00..0”. (Submit screenshot of UART input/output;) If you N# is N12345678, input is “12 34 56 78 12 34 56 78” (In Hex)		1	
2	**Run AES Decryption (InvCipher) on FPGA.**	**5**		
2.1	Submit RTL and Testbench codes (Verilog/VHDL). (Submit synthesis report from Vivado HLS)		2	
2.2	Generate Bit-stream for FPGA. (submit project summary from vivado)		1	
2.3	Try two different inputs and two different keys (4 combinations) on FPGA implementation. (submit screenshot of UART input/output)		1	
2.4	Apply your N# as input plaintext “N-number, N-number and key = “00..0”. (Submit screenshot of UART input/output;) If you N# is N12345678, input is “12 34 56 78 12 34 56 78” (In Hex)		1	
3	**Prepare a video demonstrating your module operating on the FPGA within input/output using UART … load a new plaintext and key and then trigger encryption --- 2 minutes max.**	**5**		
	Total:	**15**		