

TakuNet: an Energy-Efficient CNN for Real-Time Inference on Embedded UAV systems in Emergency Response Scenarios

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Abstract

Designing efficient neural networks for embedded devices is a critical challenge, particularly in applications requiring real-time performance, such as aerial imaging with drones and UAVs for emergency responses. In this work, we introduce TakuNet, a novel light-weight architecture which employs techniques such as depth-wise convolutions and an early downsampling stem to reduce computational complexity while maintaining high accuracy. It leverages dense connections for fast convergence during training and uses 16-bit floating-point precision for optimization on embedded hardware accelerators. Experimental evaluation on two public datasets shows that TakuNet achieves near-state-of-the-art accuracy in classifying aerial images of emergency situations, despite its minimal parameter count. Real-world tests on embedded devices, namely Jetson Orin Nano and Raspberry Pi, confirm TakuNet's efficiency, achieving more than 650 fps on the 15W Jetson board, making it suitable for real-time AI processing on resource-constrained platforms and advancing the applicability of drones in emergency scenarios. The code and implementation details are publicly released.

1. Introduction

Images captured at high altitudes are very important data that, especially if processed by artificial intelligent systems, can provide crucial information in many areas, ranging from precision agriculture [4], environmental and urban monitoring [10], energy resource planning [5], to search and rescue operations [7] and risk prevention [9].

Usually, high-altitude images are acquired by satellites, aircraft, or even drones and unmanned aerial vehicles (UAVs), where the latter has begun to gain increasing interest since they combine affordability and the acquisition of high-quality and stabilized images. In addition, in emergency response scenarios, drones and UAVs play a key and crucial role, such as entering remote or difficult-to-access areas, providing a comprehensive view of the hazard, and enabling safer conditions for the personnel engaged in rescue operations.

Unfortunately, the adoption of modern artificial intelligence systems in this kind of device is still critical and poses specific and significant challenges, mainly related to the limitation imposed by embedded hardware [32]. Specifically, the power consumption of drone and UAV hardware is constrained by the use of lightweight batteries, which limits the feasibility of employing high-frequency processors. Therefore, in the context of embedded systems, an efficient design is a key feature, especially for deep neural networks [36], such as CNNs and Transformers.

In this context, a possible solution is to run neural network architectures in the cloud. Images or videos can be sent to a remote server that takes care of processing them. We observe that this approach is not always feasible due to, for instance, damages to telecommunication infrastructure or lack of signal in remote areas. Another solution is represented by the recent introduction on the market of new ARM-based silicon architectures that combine increasingly high efficiency with ever-growing computational power [38]. Finally, a complementary approach is represented by the development of efficient neural network architectures, *i.e.* networks that require a limited amount of computing capabilities and memory, possibly maintaining a good level of accuracy [34] with respect to standard models.

Following the latter approach, in this paper, we introduce TakuNet, an extremely lightweight architecture explicitly designed to limit the number of parameters and, in general, the computational load and then foster its use on embedded boards. Indeed, the number of parameters in a model is a crucial value to consider when designing the architecture: a deficiency of parameters leads to a network that is unable to properly model and learn information from the data; on the other hand, too many parameters means wasting resources. Consequently, it is important to find the right balance, especially if the target hardware is a battery-powered embedded system with limited resources.

https://github.com/DanielRossil/TakuNet

From a technical point of view, TakuNet is mainly based on depth-wise convolutions [17], and exploits an early downsampling stem to reduce computational complexity in the initial layers. TakuNet consists of four different stages, at the end of each a downsampler block reduces the size of the feature maps while implementing a dense connection which allows for fast convergence of the model during training. TakuNet is trained with a floating-point resolution of 16 bits, enabling lossless optimization on hardware accelerators for embedded systems. Through the utilization of NVIDIA TensorRT², a substantial enhancement in performance is achieved.

The experimental evaluation of model accuracy is conducted on two public datasets, namely AIDER [23] and AIDERv2 [42], both containing aerial images depicting emergency situations, *e.g.* floods, traffic accidents, and fires. The proposed method achieves an accuracy close to the state-of-the-art, despite a very limited number of parameters. Finally, we test TakuNet on embedded devices, *i.e.* Jetson Orin Nano and Raspberry Pi, demonstrating its real-time performance and potential for deployment on drones in emergency response scenarios.

In summary, the contributions of this work are the following ones:

- We introduce TakuNet, a new architecture specifically designed to limit the number of parameters and computational complexity. This promotes the adoption of our architecture on embedded boards, e.g. drones and UAVs, commonly employed in emergency scenarios.
- We assess the performance of our model using the F1score metric on two public datasets, attaining high accuracy despite its constrained computational requirements.
- 3. We evaluate our architecture on four real-world embedded platforms, *i.e.* Jetson Orin Nano and three Raspberry Pi. TakuNet achieves more than 650 fps on the Jetson board when optimized with TensorRT.

2. Related Work

2.1. Performance of Deep Learning architectures

Convolutional architectures for image processing are among the most studied in the field of Computer Vision.

The first notable architecture was AlexNet [22], the first deep model trained on a GPU, which used dropout layers and ReLU activation functions and won the 2012 ILSVRC competition. Unlike the previous method, VGG [43] promoted the use of small kernels in convolutional layers and a uniform architecture that progressively increased the number of channels in the feature maps. As the networks

gradually became deeper, the problem of vanishing gradient began to be noticed, making weights update negligible. ResNet [12] demonstrated the effectiveness of skip connections, in which the output of a layer was added to its input, resulting in extremely deep architectures. Differently, DenseNet [19] exploited dense connections between the input and output of its blocks, promoting feature reuse and improving model efficiency.

Unlike previous approaches, the introduction of Vision Transformers (ViT) [6, 48] for image processing significantly increased both the number of parameters and the overall complexity of the models. ViTs [6] can model global dependencies and consequently extract more relevant features for vision tasks. Unfortunately, the attention mechanism scales its complexity quadratically, limiting performance and easily saturating the memory due to the huge matrices that need to be computed.

In summary, despite being able to model only local relationships between feature maps, CNNs are fundamentally designed to be efficient through the use of shared kernels. Recent developments in CNNs have made it possible to further reduce their complexity while preserving or enhancing their output quality.

2.2. Towards more efficient architectures

One of the pioneering approaches in neural network efficiency is SqueezeNet [20], which reduces the size of the model by more than 500 times compared to AlexNet. It employs "fire modules", which integrate "squeeze" and "expand" convolution layers, lowering the number of parameters while preserving high performance.

Subsequently, ShuffleNet [54] improves efficiency by introducing the "shuffle" operation, which rearranges feature maps to enhance communication between convolution groups. This overcomes the limitations of group-wise convolutions that restrict interaction along the channel axis.

One of the most efficient convolutional blocks was introduced in MobileNetV1 [17], namely depthwise separable convolution. They consist of a depthwise convolution applied independently to each input channel, followed by a 1×1 convolution that combines the resulting feature maps along the channels, leading to a reduction in parameters and computational costs compared to traditional 2D convolutions. MobileNetV2 [39] enhances accuracy through the introduction of the "inverted residual structure", which first expands the channel size using pointwise convolutions before applying depthwise convolutions, in contrast to traditional architectures. Additionally, it incorporates shortcut connections between bottleneck blocks, akin to ResNet networks, facilitating direct information flow, improving gradient propagation, and aiding in network training. Later, MobileNetV3 [16] optimizes its architecture using Neural Architecture Search (NAS) to enhance design efficiency.

²https://developer.nvidia.com/tensorrt

It simplifies the model by removing certain layers and introduces the HardSwish activation function. Additionally, MobileNetV3 incorporates "squeeze-and-excitation" [18] blocks, allowing the network to recalibrate channel activations, emphasizing informative features while suppressing less relevant ones, thereby improving the quality of learned representations.

EfficientNet [45] introduces a novel approach to scaling neural networks through compound scaling, which uniformly adjusts the network's width, depth, and resolution to optimize performance. This method allows for efficient adaptation of larger models to smaller datasets and vice versa, ensuring high output quality while enhancing overall efficiency.

In addition to solutions based on efficient architectural choices, neural networks can also be optimized a posteriori. Pruning and quantization [49] are two of the most wellknown strategies used to optimize neural networks. Pruning works by removing unnecessary weights or connections from a model, which reduces its size and computational demands. This can lead to faster inference times and a smaller memory footprint, while often preserving accuracy if done correctly. However, pruning can be complex to implement and its improper execution may result in a loss of model performance. Quantization, on the other hand, involves converting the model's weights and activations from floatingpoint precision to lower-bit representations, such as 8-bit integers. This approach improves computational efficiency and reduces energy consumption. Despite these benefits, quantization, if not carefully managed, carries the risk of accuracy degradation. Besides, not all hardware supports low-precision computations, limiting its applicability.

2.3. Challenges in aerial images recognition tasks

In the context of image recognition, datasets containing frames captured at high altitudes pose different challenges than scenes captured on the ground. For instance, many aerial data collections [13, 47, 52] contain multispectral imagery, which requires appropriate extraction or fusion layers of the spectral bands of input features. The various spectral feature maps can be composed of images captured in the visible light band, infrared, ultraviolet, and so on. Sensors for multiband acquisition have exorbitant costs and are often mounted on satellites, making updating such datasets an expensive and burdensome operation.

In addition, real-time monitoring through satellite imagery is challenging, as satellites take hours, if not days, to sample specific points on the planet multiple times. However, images acquired from drones or aircraft hardly integrate multispectral images. Nevertheless, these devices allow to perform real-time monitoring of specific and even remote areas, providing access to data at a lower latency.

Regardless of the acquisition system, high-altitude imag-

ing is characterized by the fact that objects are very small and details are quite difficult to capture. Aerial datasets such as [23,42] provide a more extensive overview of the area being monitored and find easy use in the analysis and recognition of, for example, violent weather events, such as forest fires, floods, major vehicle accidents, or collapse of buildings.

2.4. Methods for aerial image recognition

In recent years, aerial image classification has played a crucial role in various scenarios, including agriculture, where the ability to analyze and interpret visual data can significantly improve resource management.

Yang et al. [53] approach combines spatial and spectral information through a hybrid classification technique, achieving high accuracy in classifying damaged rice lodging areas using drone-acquired imagery. Mafania et al. [29] proposes to map the invasive plant Harrisia pomanensis using UAV imagery, comparing different image classifiers to assess their effectiveness in mapping this species. Among the later methods for aerial image classification, APDC-Net proposed by Bi et al. [2] is distinguished by the use of attention-based pooling and a dense connection structure, which preserves multilevel features and improves local semantic representation. To improve object detection in UAV images, Hendria et al. [14] proposed a combined approach that integrates transformer-based models [25] and CNN [37], using ensemble and hybrid techniques. However, the shortcoming of these methods is that they are all designed to run offline and therefore do not allow for realtime processing of aerial images. In this regard, two important contributions are introduced in [24] and [33], who laid the groundwork for architectures capable of running on UAV(s). Kyrkou et al. introduced EmergencyNet [24], a model based on atrous convolution, whose multi-resolution features are later merged. Mogaka et al., derived TinyEmergencyNet [33] from the previous method by using a pruning strategy, removing up to 60% of the least significant weights of the model.

However, despite significant advancements in efficient neural architectures, many models remain too complex for widespread deployment on embedded devices. There is a clear gap in approaches specifically tailored for these systems, particularly regarding micro-components like activation functions, which can exhibit varying latency. Furthermore, existing hardware accelerators for neural networks are often overlooked in architecture design. TakuNet aims to address these challenges by consolidating and harmonizing existing techniques that enhance neural network efficiency, focusing on minimizing parameters and latency specifically for embedded devices. It is specifically designed to leverage available hardware accelerators, ensuring that the weights learned during training remain intact.

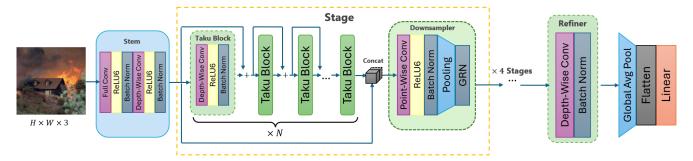


Figure 1. Overview of the TakuNet architecture. The input image is first processed by a convolutional stem block. Four subsequent stages progressively extract spatial features, whose final output is later integrated along the channel axis with dense connection feature maps coming from the stage's input. At the end of each stage, the Downsampler block reduces the spatial size, while expanding the channel dimension. Finally, the Refiner block balances spatial features before the linear classification layer.

3. TakuNet model

The architecture of the proposed TakuNet is depicted in Figure 1. Our choices are driven by the need to develop a model that combines strong performance in image classification with limited computational demands -i.e. a limited number of parameters and floating point operations - enabling real-time execution on embedded hardware.

From a general point of view, we take advantage of several elements introduced in the recent literature. The first is the depth-wise convolutions and grouped point-wise convolutions, inspired by [17, 40] to reduce the number of convolutional layer parameters. We harness the Global Response Normalization layer [50] to promote feature diversity and increase contrast and selectivity along channels, enabling the model to identify and differentiate more effectively between relevant features. In addition, dense connections [19] are used to encourage feature reuse and better gradient propagation. Finally, following [24], we have included a layer of dilated convolution in the stem to capture more distant features without enlarging the number of parameters.

3.1. TakuNet Architecture

From an architectural point of view, TakuNet consists of 6 main macroblocks -i.e. a stem block, 4 stages containing Taku Blocks and a Downsampler block, a Refiner block, and a final linear layer that acts as a classifier.

The first block is the stem, consisting of two stacked convolutional layers according to the following formulation:

$$y = \text{ReLU6}(\text{BN}(\text{Conv}_{3\times3}(x))),$$

$$z = \text{ReLU6}(\text{BN}(\text{DWConv}_{3\times3}(y))) + y,$$
(1)

where in this formula, and in the next sections of the paper, ReLU6 and BN denote Rectified Linear Unit function [17] clamped between $[-\infty, 6]$, and Batch Normalization [21], while DWConv refers to depthwise convolution.

The initial 3×3 full-convolution has a stride of 2, a

padding of 2, and a dilation of 2. An additional 3×3 depthwise convolution layer follows, with stride 2 and padding 2. In these early layers of the network, the size of the initial image is reduced from $H\times W\times 3$ to $\frac{H}{4}\times \frac{W}{4}\times 40$. This plays a crucial role in significantly reducing computational complexity, as each successive convolutional layer will need to be applied fewer times on the feature maps it receives as input.

The architecture subsequently consists of 4 stages. Each stage is composed of multiple Taku Blocks, which can be represented by the following formulation:

$$y = \text{ReLU6}(\text{BN}(\text{DWConv}_{3\times3}(x))) + x,$$
 (2)

in which a depth-wise convolution with stride 1 is applied. The dilation and padding are set to 1 for all Taku Block of each stage. The four stages have a depth of (5, 5, 5, 4), respectively. The number of stages and blocks are empirically set, aiming for the best tradeoff between accuracy on one side and model size and efficiency on the other side. At the end of each stage, a Downsampler block is responsible for reducing the size of the feature maps, while expanding the number of channels. Inspired by [19, 54], the feature maps produced by the last Taku Block are concatenated and mixed with those coming from the dense connection. To further reduce the number of parameters, we apply a grouped point-wise convolutional layer [40] on the new concatenated feature maps, where the number of groups is given by | (in_channels+out_channels)/4 |. Here in_channels refers to the number of channels of the feature maps input to the stage, while out_channels refers to the number of channels of the feature maps output to the last Taku Block.

Next, a Batch Normalization and a ReLU6 activation function are applied. In the first 3 stages of the architecture, the output is then dimensionally scaled by a max-pooling layer, while in the last stage average pooling is applied. Each of these pooling layers is then followed by a Global Response Normalization (GRN) [50] function.











Figure 2. The variety of some of the images in the AIDER [23] dataset grouped by each class. In detail, from the left, collapsed buildings, fire/smoke, floods, traffic incidents and normal classes are shown.

Following the last stage, a Refiner block is applied to the feature maps according to the following formulation:

$$y = \text{AdaptiveAvgPool}(BN(DWConv_{3\times3}(x))),$$
 (3)

where the adaptive average pooling layer reduces the height and width dimensions of the feature maps to a unit value. The probability of each class is derived through a linear layer applied to the latent vector generated by the Refiner.

4. Experiments

4.1. Aerial Image Disaster Event Recognition (AIDER) dataset

The AIDER [23] dataset is a collection of images acquired by aerial vehicles coming from various sources, such as the world-wide-web (YouTube, newspaper web pages, the image section of various search engines, etc.) and via real-world drone acquisitions. The dataset consists of a set of multi-resolution images of complex scenes composed of natural territories, urban environments, large road infrastructure, rural or coastal areas, and so on. It includes scenes acquired in different seasons and at distinct times of the day, trying to offer a truthful overview of the real world, despite its small size. The hand-collected images contain scenes of emergency situations such as floods, collapsed buildings, traffic accidents, and fires. The first version of the dataset features 320 images for fires/smoke, 370 images for floods, 320 images for collapsed buildings/rubble, 335 images for traffic accidents, and 1200 images for the normal class, i.e. aerial images free of the various types of disasters. The dataset has a first limited version in size and was later expanded in [24]. Unfortunately, this latest version has been reduced due to copyright infringement and a rather high number of images have been removed. The image composition of the AIDER dataset is detailed in Table 1, which enumerates the total number of images available along with a breakdown of the distribution between individual classes. For a fair comparison, we split the dataset into training and testing sets, using a proportion of 70/30 for all classes except Normal, split with a proportion of 65/35, keeping the same test proportions as [33] and [24].

Due to the scarcity of data, we did not leave room for a standalone validation set, which we replaced with a k-fold cross-validation method performed on the training set, with k=5.

Class	Train	Test	Total
Collapsed Building	395	146	511
Fire/Smoke	403	148	521
Flood	406	150	526
Traffic Accidents	376	139	485
Normal	3,250	1,540	4,390
Total Per Set	4,830	2,123	6,433

Table 1. Class distribution across training and testing sets of AIDER dataset [23] (latest available version).

4.2. Aerial Image Disaster Event Recognition Version 2 (AIDERv2) Dataset

Similarly to AIDER, AIDERv2 [42] is a collection of aerial images representing multiresolution emergency situations. The dataset collects urban, suburban, rural, coastal or lagoon scenes, and natural parks, taken at different times and seasons. Unlike the previous, the dataset is fully available and official training, validation, and test sets are provided, where the split ratio is set to 80/10/10, respectively, as expressed in Table 2.

Class	Train	Validation	Test	Total
Earthquakes	1,927	239	239	2,405
Flood	4,063	505	502	5,070
Fire	3,509	436	436	4,384
Normal	3,900	487	477	4,864
Total Per Set	13,399	1,670	1,654	16,723

Table 2. AIDERv2 [42]: distribution across training, validation, and testing sets.

Model	Parameters	Model Size (MB)	F1-score	FLOPS
VGG16 [43]	14,840,133	59.36	0.601	17.62G
ResNet50 [12]	23,518,277	94.07	0.917	4.83G
SqueezeNet [20]	737,989	2.95	0.890	845.38M
EfficientNet B0 [45]	4,013,953	16.06	0.950	479.68M
MobileNetV2 [39]	2,230,277	8.92	0.930	371.82M
MobileNetV3 [16]	4,208,437	16.83	0.915	265.02M
ShuffleNet [54]	1,258,729	5.03	0.908	176.82M
EmergencyNet [24]	90,963	0.360	0.936	77.34M
TinyEmergencyNet [33]	39,334	<u>0.160</u>	0.895	<u>36.30M</u>
TakuNet _{FP=16}	37,685	0.15	0.943	35.93M
TakuNet _{FP=32}	37,685	0.15	0.938	35.93M

Table 3. Comparison of model parameters, memory footprint, F1-score, and FLOPs on the latest AIDER [23] version, where images are set to 240×240 pixels. Elements highlighted in **bold** refer to the best results, while those <u>underlined</u> refer to the second-best results.

4.3. Training

In the early stage of the training pipeline, we apply image augmentation as a pre-processing step to enhance pattern generation and increase variance in the limited datasets. These augmentations are the same as those indicated in [24] and include color shifting, blurring, geometric transformations (translations, rotations, mirroring), random image cropping, sharpening, shadowing, illumination variations, and zooming. Each transformation is applied with a randomly selected probability between 0.05 and 0.5, ensuring the model does not interpret random variations as intrinsic dataset properties. Thereafter, all images are scaled to the range [0,1] and resized to a fixed dimension of 240×240 pixels for height and width.

Trainings are conducted on a system equipped with NVIDIA RTX 4070 Ti Super and Intel i7-12700F. TakuNet is trained using the RMSProp [46] optimizer with decay 0.9, momentum 0.9, and an initial learning rate of 1×10^{-3} , along with a L₂-regularization term of 1×10^{-5} . Training is performed over 300 epochs with a batch size of 64, using a step learning rate scheduler to adjust the learning rate at each epoch, as defined by the following formula:

$$\eta_t = \eta_0 \times \gamma^{\lfloor t/\text{step_size} \rfloor} \tag{4}$$

where η_t represents the learning rate at epoch t, γ is the multiplicative factor for the learning rate, and $step_size$ is the period of learning rate decay. We use a γ value of 0.975 with a $step_size$ of 2. Finally, a cross-entropy loss function is used to measure the error in the probability estimates generated by the final linear layer.

4.4. Evaluation and Performance Metrics

Similarly to [24, 33], to validate the accuracy of the method proposed here, we use the F1-score metric. This

type of metric is very effective at measuring the quality of a model in the case where the dataset is unbalanced.

As performance metrics, we use FLOP as the unit of measurement of computational complexity. FLOPs indicate the number of floating-point operations that a system can perform in one second. This measure has been criticized in literature [44, 51] because it often does not reflect networks performance when executed on a real device. In addition, the efficiency of neural network components can vary significantly depending on the computational capabilities of the underlying hardware, particularly the CPU. To address this limitation, we provide a practical understanding of our model's performance, reporting the framerate obtained on real-world embedded boards. This assessment highlights the model's latency, offering a more explicit perspective on its suitability for deployment in real-world scenarios.

5. Results

To comprehensively evaluate our model in terms of key metrics, such as the number of parameters, memory footprint, FLOPs, and F1-score, we conduct a comparative analysis against several well-known convolutional architectures, with particular focus on EmergencyNet [24] and TinyEmergencyNet [33]. These architectures are chosen because of their specific design for the aerial image recognition task.

Both EmergencyNet and TinyEmergencyNet are reimplemented using the PyTorch³ framework, adhering rigorously to the instructions detailed in the respective articles [24, 33]. During this process, we observe minor discrepancies in the publicly available implementation of EmergencyNet, while no official implementation of TinyEmergencyNet is found online. Other architectures included in the comparison are sourced directly from the TorchVision

³https://pytorch.org

Model	Parameters	Model Size (MB)	F1-score	FLOPS
ConvNext Tiny [26]	27,820,000	111.29	0.940	4.46G
GCVit XXtiny [11]	11,480,000	45.93	0.932	1.94G
Vit Tiny [6]	5,530,000	22.1	0.873	1.08G
Convit Tiny [8]	5,520,000	22.07	0.871	1.08G
MobileViT s [30]	4,940,000	19.76	0.855	1.42G
MobileViT V2 0100 [31]	4,390,000	17.56	0.875	1.41G
EfficientNet-B0 [45]	4,010,000	16.05	0.862	0.41G
MnasNet [44]	3,110,000	12.43	0.897	0.34G
MobileNetV2 [39]	2,230,000	8.92	0.893	0.33G
MobileViT xs [30]	1,930,000	7.74	0.837	0.71G
ShuffleNet V2 [27]	1,260,000	5.03	0.852	0.15G
MobileVit V2 050 [31]	1,110,000	4.46	0.834	0.36G
MobileViT xxs [30]	950,000	3.81	0.859	0.26G
MobileNetV3 Small [16]	930,000	3.72	0.868	0.06G
DiRecNetV2 [41]	799,380	3.20	0.964	1.09G
SqueezeNet [20]	730,000	2.90	0.845	0.26G
EmergencyNet [24]	90,704	0.360	0.952	61.96M
TinyEmergencyNet [33]	39,075	<u>0.160</u>	0.928	<u>31.57M</u>
TakuNet _{FP=16}	37,444	0.15	0.958	31.38M
TakuNet _{FP=32}	37,444	0.15	0.954	31.38M

Table 4. Comparison of Model Parameters, Size, F1-score, and FLOPs on AIDERv2 [42], where image height and width are set to 224. Elements highlighted in **bold** refer to the best results, while those <u>underlined</u> refer to the second-best results.

library⁴, ensuring consistency and reproducibility in benchmarking. All methodologies in comparison are trained for 300 epochs with a batch size of 64 on AIDER (Table 3) and AIDERv2 (Table 4) datasets, employing the training settings specified in the respective publications.

5.1. Results on AIDER

We first perform a set of experiments on AIDER [23] to validate the effectiveness of our method against some of the well-known CNNs, along with EmergencyNet and TinyEmergencyNet. Leveraging the stem to reduce the size of the input images by a factor of 4 has significantly enhanced the efficiency of our approach. Although our method employs a sparse integration of features along the channel axis, dense channel features integration enables TakuNet to perform proficiently on AIDER while considerably reducing its parameter count. The results shown in Table 3 highlight that TakuNet is capable of surpassing EmergencyNet in F1-score while using the minimum number of parameters and FLOPs among the various competitors.

These results point out that our method is the best in terms of the trade-off between F1-score/FLOPs, making a significant contribution to high-efficiency aerial image classification methods. Furthermore, when TakuNet is trained using floating point 32 precision, the F1-score obtained on the test set is lower to a minor extent. This result is important for two other reasons. First, the difference in

F1-score between the use of 16-bit floating-point precision (FP=16) and 32-bit floating-point precision (FP=32) is moderated. However, the efficiency gap between the two is substantial, primarily due to hardware acceleration, enabling the optimization of half-precision computation. Secondly, not all processors support hardware acceleration for 16-bit floating-point precision. In such cases, either lossless 32-bit floating-point weight casting or 16-bit floating-point emulation can be employed.

5.2. Results on AIDERv2

To evaluate the robustness of our method, we also trained it on AIDERv2 [42], which consists of a larger number of images to be classified.

As shown in Table 4, TakuNet is able to provide the second-best F1-score with fewer parameters and FLOPs compared to competitors. Therefore, despite having a very small number of parameters, our method demonstrates its ability to compete with much larger architectures on more complex scenarios.

Deeper experiments on AIDERV2 showcase the effectiveness of a few architectural design choices. In fact, by removing dense connections the model does not converge during training, while by omitting GRN the overall F1-score decreases to 0.950. The channel shuffle and the refiner block also are key elements for the high-quality outputs of TakuNet since their exclusion causes the accuracy to drop at 0.956 and 0.955, respectively.

⁴https://pytorch.org/vision/stable

Device	Accelerator	TDP	Model	No. Images	FPS
Raspberry Pi 3	CPU ARM Cortex-A53	5W	EmergencyNet TinyEmergencyNet TakuNet	1000 1000 1000	6.7 10.8 7.0
Raspberry Pi 4	CPU ARM Cortex-A72	10W	EmergencyNet TinyEmergencyNet TakuNet	2500 2500 2500	14.7 22.0 16.7
Raspberry Pi 5	CPU ARM Cortex-A76	10W	EmergencyNet TinyEmergencyNet TakuNet	2500 2500 2500	43.3 59.8 62.1
Jetson Orin Nano	GPU Tegra (Ampere)	15W	EmergencyNet TinyEmergencyNet TakuNet _{TDP=15W} TakuNet _{TDP=7W}	2500 2500 2500 2500	140.0 160.0 657.0 564.0

Table 5. Model performance evaluation on embedded platforms, with fps calculated as the mean latency over multiple runs with batch size equal to 1 and image size of 240 pixels. TakuNet's fps on Jetson Orin are reported after TensorRT optimization.

5.3. Performance on Embedded Platforms

To evaluate the inference efficiency of TakuNet, we performed multiple runs on various embedded platforms to measure latency and later compute related frames per second (fps). The results are summarized in Table 5. Notably, TakuNet exhibits limitations in performance on earlier embedded systems such as Raspberry Pi 3 and Pi 4. One potential bottleneck is the GRN layer, where the computation of norms may not be fully optimized for these specific CPUs. Indeed, as shown in Table 6, activation functions that require complex mathematical computations demonstrate increased latency on the Raspberry Pi 4.

ReLU [35]	ReLU6 [17]	LReLU [28]
30.08s	30.84s	30.87s
ELU [3]	CELU [1]	GELU [15]
168.56s	169.27s	401.49s

Table 6. Latency of common activation functions on a Raspberry Pi 4, measured during execution on a (10000, 100) tensor.

In contrast, on more advanced hardware, such as the Raspberry Pi 5, TakuNet outperforms competing approaches, effectively demonstrating its ability to take advantage of the improved CPU power. The key benefit of our approach becomes evident with hardware acceleration, particularly when utilizing the GPU on Jetson devices. Since our method is trained using half-precision floating-point weights, it can be further optimized via TensorRT without any degradation in weight precision. This enables TakuNet to surpass TinyEmergencyNet by a $4.1\times$ speed increase.

To further demonstrate the efficiency of our method, we restrict the Jetson Orin power consumption to a thermal de-

sign power (TDP) set to 7W, achieving a $3.5\times$ performance improvement compared to TinyEmergencyNet operating at 15W. This significant reduction in power consumption highlights the suitability of TakuNet for resource-constrained environments.

6. Conclusion

This research highlights the importance of designing neural network models with a clear consideration of the target context, particularly the embedded devices intended for inference deployment. As demonstrated, combining existing state-of-the-art solutions in a systematic manner enables the creation of highly efficient architectures.

Our proposed TakuNet achieves significant results, providing high accuracy compared to competing approaches while minimizing the parameter count, FLOPs, and memory usage. This makes it a versatile solution capable of addressing a wide range of requirements in embedded applications, particularly in emergency response scenarios. Additionally, we emphasize the significant impact of hardware-specific characteristics on model performance, such as the varying latencies of embedded devices when processing specific model components. By focusing on hardware-aware design, we demonstrate that impressive performance can be achieved through hardware acceleration, and that models trained with FP16 precision can be highly competitive. Such an approach is advisable for edge device models.

Future directions for this work include exploring pruning and quantization techniques to further reduce model complexity. These advancements could enable real-time execution TakuNet on microcontrollers, facilitating the integration of emergency response systems into miniaturized and ultralow-power devices.

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