

Subject - D.L.D.

Assignment No:-3

Q.1:

Ans.

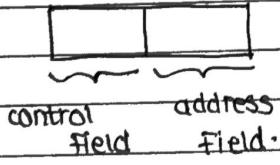
Microprogram control unit:-

With large number of instructions the hard wired control unit becomes complicated moreover the hard wired design is not flexible, because of these limitations micro program control unit is design which is software based and flexible. In these, for every instruction there are microinstructions. These micro-instruction indicates control signals to be activated. Micro-instructions are stored in RAM called as control Memory.

The set of microprogram for all instructions are available in control memory.

Microinstruction format:-

control memory contains various control signal generated based on selection of micro-instruction. Each micro-instruction has two part.



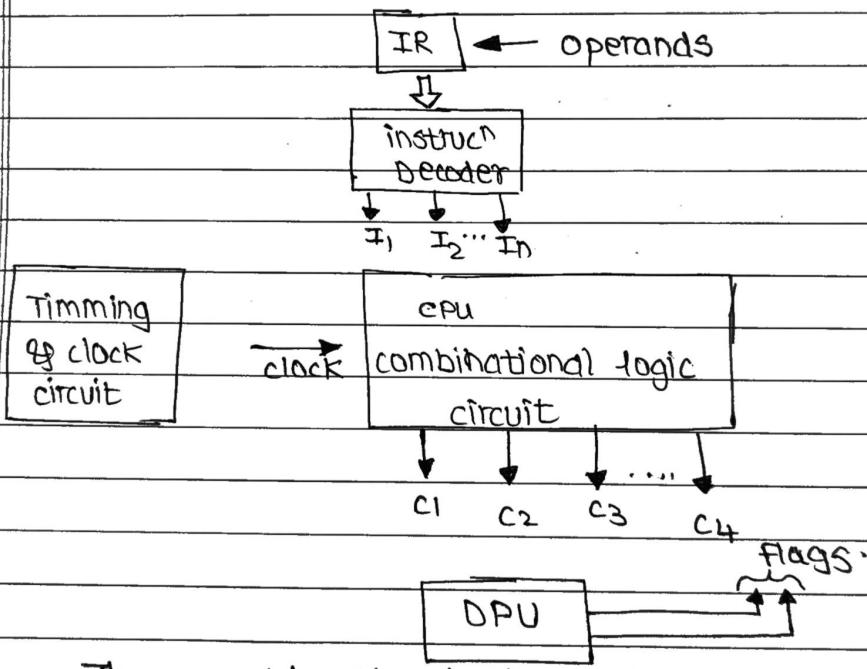
- Control field specifies the control signal to be activated.
- Address field specifies address of next micro-instruction in memory.
- The starting address of microprogram is provided by an external source and stored into CMAR.
- Based on these address the microinstruction is selected.

- The switch(s) is useful for conditional instructions.
- Based on value of switch(s) two possible addresses can be loaded into CMAR and program will proceed according to current condition.

Q.2

Ans. Hardwired control unit :-

In these designs, the combinational logic circuit is used to generate the control signals.



The combinational logic circuit generates control signals based on input code from instruction decoder. The control signals are synchronized w.r.t input clock.

Hardwired control unit faster than micro-program control unit. It is almost impossible to make changes in hardwired control unit.

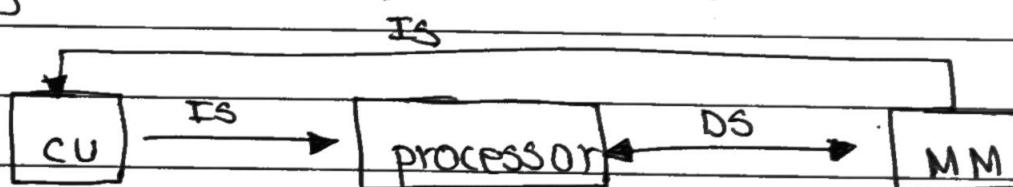
ANS.

Flynn's classification:-

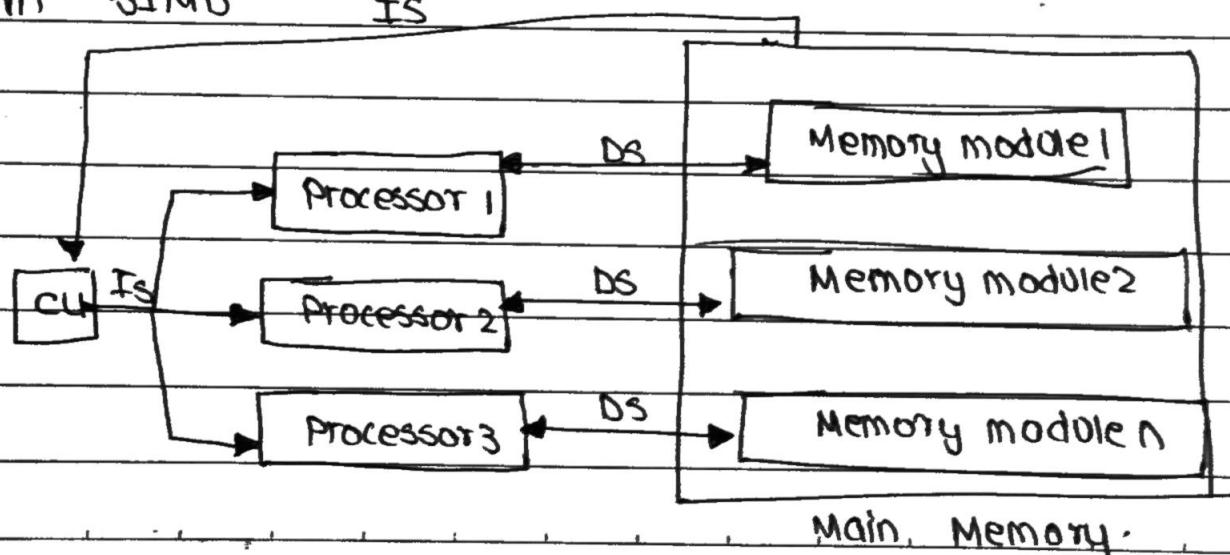


The classification made by M.J Flynn divides computer into 4 major groups based on values of instruction stream and data streams associated with CPU are

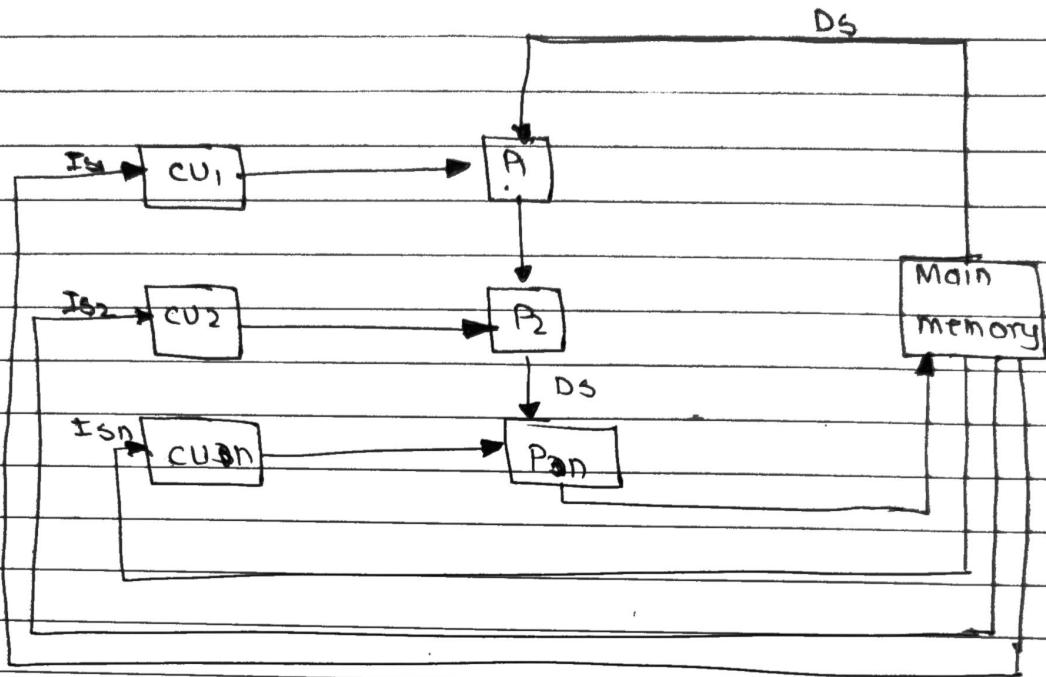
(j) SISD



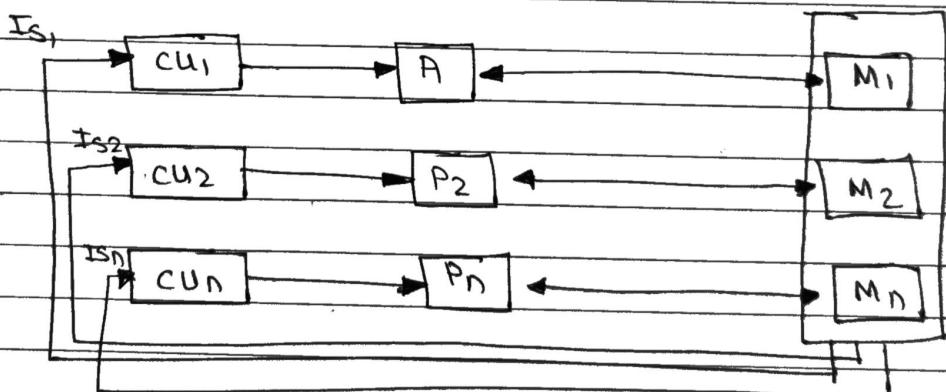
(iii) SIMD



(iii) MISD



(iv) SIMD



Subject - DLCA

Assignment NO : 4

Q.1

Ans.

instruction pipelining:-

- Instruction cycle of the processor or CPU consists of many functions and is operationally divided into its functional units.
- A single instruction in processor life cycle at a time is an inefficient process.
- When a specific instruction completes its work on the specific functional unit and goes to the next functional unit the earlier functional unit is free, and it can process subsequently next instruction in some time frame.
- Therefore, at any given instance, different instructions are in different stages of advancement at the same time allows a greater number of instructions to be executed in same time. This feature is called as instruction Pipelines.
- In non pipelined processor case, it is seen that instructions require two time slots each to complete its fetching and execution.
- This functional overlap allows a greater number of instructions to be executed in same time frame.
- To increase performance of the processor instructions are simultaneously fetched and executed this technique of fetching while executing is called instruction pipeline.

Hazards are :

- structural Hazards
- Data Hazards
- control Hazards.

Q.2.

Ans.

(i) PCI

- Peripheral component interconnect (PCI) was designed by committee of computer scientists set up by IBM and other computer companies as universal international standard for 32-bit interface for 32-bit system architecture.
- It replaced earlier 16-bit standard such as 16-bit ISA and Extended ISA (EISA) buses. It had many unique features and was designed to be green, environment friendly bus standard.
- PCI bus is driven using a special component called as PCI bridge.

(ii) ISA

- Industry standard Architecture is parallel bus standard design by IBM for providing internationality standardised interfacing capabilities to the system boards for its original 1st generation Personal computer (PC's). The bus is based on 8-bit architecture and offers following features:-

- (i) This bus provides 8 data lines and 20 address lines. Thus addressing capability of 1MB.
- (ii) The ISA Bus was originally designed for 8-bit architecture but later on upgraded to house 8 as well as 16-bit Architecture. Therefore, bus is available in 2 versions 8-bit version & 16-bit version.
- Enables to handle 1MB of memory.

(iii) universal serial Bus (USB)

- Universal serial Bus (USB) is international universal bus/port interface standard for connecting peripherals & I/O devices with computer system & works on the synchronous serial data communication protocols & techniques.
- Computer comes with one or more Universal Serial connector on back. All the operating system supports USB so that installation of drivers is quick and easy.
- It is capable of interfacing to slow & high-speed input devices as well as output devices at same time with external mass storage devices & streaming Multi-media devices.

Q. 3.

Ans.

- A conflicts may arise if no. of DMA controllers or any other controllers or processors try to access the common bus at the same time but access can be given to only one of those. If there are multiple bus masters assigned to bus immediately, multiple signals would be mixed on the buses. This would lead to arise to noise and hardware design/damage. This situation is called as Bus contention.
- Bus Arbitration refers to process by which current bus master accesses & then leaves control of the bus & passes it to another bus requesting processor unit controller that has access to bus at an instance is known as Bus master.