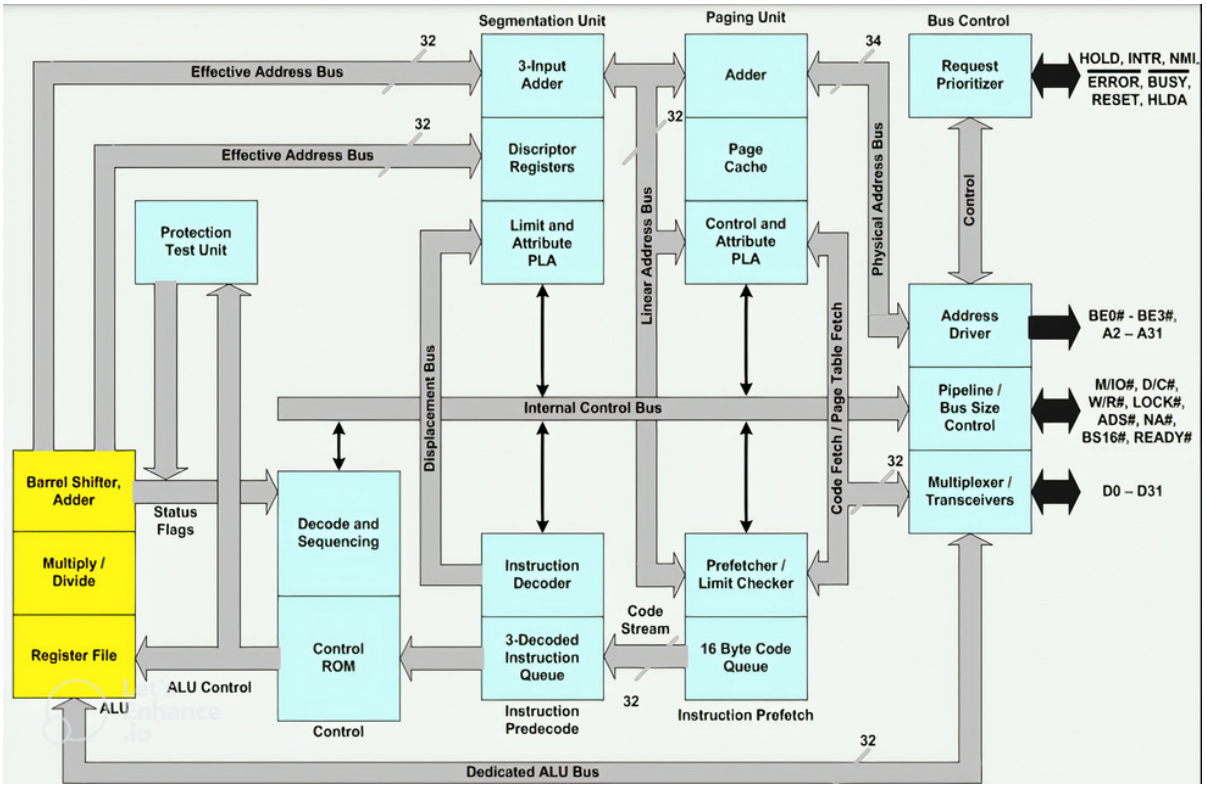
MINUTE PAPER

INTEL 80386 DX MICROPROCESSOR



BUS INTERFACE UNIT

- BIU CONNECTS THE 80386 WITH MEMORY & I/O
- IT HOLDS 32 BIT BIDIRECTIONAL DATABUS & 32 BIT ADDRESS BUS
- IT CONTROLS THE INTERFACE TO EXTERNAL BUS MASTERS AND COPROCESSORS.
- IT ALSO PROVIDES THE ADDRESS RELOCATION FACILITY IT INCLUDE SUPPORTS FOR MULTITASKING OPERATING SYSTEM

CODE PREFETCHQUEUE UNIT

- THIS UNIT FETCHES THE INSTRUCTIONS STORED IN THE MEMORY BY MAKING USE OF SYSTEM BUSES. THE SYSTEM GENERATES A NEED FOR INSTRUCTION THEN THE CODE PREFETCH UNIT FETCHES THAT INSTRUCTION FROM THE MEMORY AND STORES IT IN A 16-BYTE PREFETCH QUEUE.
- THIS UNIT FETCHES ONE DOUBLE WORD (32 BITS) I SINGLE ACCESSS

INSTRUCTION DECODE UNIT

THIS UNIT DECODES THE INSTRUCTIONS STORED IN THE PREFETCH QUEUE.

THE INSTRUCTION DECODE UNIT TAKES THE INSTRUCTION BYTES FROM THE CODE PREFETCH QUEUE AND TRANSLATES THEM INTO MICROCODE.

THE DECODED INSTRUCTION ARE THEN STORED IN THE INSTRUCTION QUEUE. THEY ARE PASSED TO CONTROL SECTION FOR DERIVING THE NECESSARY CONTROL SIGNALS

EXECUTION UNIT

THESE INSTRUCTIONS ARE PROVIDED TO THE EXECUTION UNIT IN ORDER TO EXECUTE INSTRUCTIONS. THE CONTROL UNIT CONTAINS MICROCODE AND PARALLEL HARDWARE FOR FAST MULTIPLY, DIVIDE, AND EFFECTIVE ADDRESS CALCULATION.

THIS UNIT HAS A 32-BIT ALU, THAT PERFORMS THE OPERATION OVER 32-BIT DATA IN ONE CYCLE. ALSO, IT CONSISTS OF 8 GENERAL PURPOSE AS WELL AS 8 SPECIAL PURPOSE REGISTERS. THESE ARE USED FOR DATA HANDLING AND CALCULATION OF OFFSET ADDRESS.

MEMEORY MANAGEMENT UNIT

Segmentation Unit

- THE SEGMENTATION UNIT OFFERS A PROTECTION MECHANISM IN ORDER TO PROTECT THE CODE OR DATA PRESENT IN THE MEMORY FROM APPLICATION PROGRAMS.
- IT GIVES 4 LEVEL PROTECTION TO THE DATA OR CODE PRESENT IN THE MEMORY.
- EVERY INFORMATION IN THE MEMORY IS ASSIGNED A PRIVILEGE LEVEL FROM PL0 TO PL3. HERE, PL0 HOLDS THE HIGHEST PRIORITY AND PL3 HOLDS THE LOWEST PRIORITY.

Paging Unit

PAGING IS A FUNCTION OF MEMORY MANAGEMENT WHERE A COMPUTER WILL STORE AND RETRIEVE DATA FROM A DEVICE'S SECONDARY STORAGE TO THE PRIMARY STORAGE..

General purpose Register

- The 80386 contains 32-bit general purpose register called EAX, EBX, ECX, EDX, ESP,EBP, ESI, and EDI.
- The lower 16-bits of each of the general purpose register can be accessed individually.
- These 16-bit registers are accessed as AX, BX, CX, DX, SP, BP, SI, and, DI respectively.
- The AX, BX, CX and DX registers can be further divided into two separate bytes: Higher byte and lower byte.

EFLAGS

- ❖ STATUS FLAG
  - CF (Carry Flag)
  - PF (Parity Flag)
  - AF (Auxiliary Carry Flag) ZF (Zero Flag)
  - SF (Sign Flag)
  - OF (Overflow Flag)
- ❖ CONROL FLAG
  - DF (Direction flag)
- ❖ SYSTEM FLAG
  - VM (Virtual Memory) flag R (Resume) flag
  - NT (Nested flag)
  - IOPL (1/0 Privilege level) IF (Interrupt Flag) TF (Trap Flag)

Control Register

The 80386 contains 32-bit general purpose register called EAX, EBX, ECX, EDX, ESP,EBP, ESI, and EDI. The lower 16-bits of each of the general purpose register can be accessed individually.
These 16-bit registers are accessed as AX, BX, CX, DX, SP, BP, SI, and, DI respectively.
The AX, BX, CX and DX registers can be further divided into two separate bytes: Higher byte and lower byte.
1.CR0 (Control Register 0): This register controls various system operations such as memory management, task switching, and protected mode. It has several bits that control these operations, including the PE (Protected Mode Enable) bit, which enables or disables protected mode operation, and the PG (Paging) bit, which enables or disables memory paging.
2.CR1 (Control Register 1): This register is reserved and not used by the processor.
3.CR2 (Control Register 2): This register is used for debugging purposes. It contains the linear address of the last page fault that occurred.
CR3 (Control Register 3): This register is used to specify the base address of the page directory. The page directory is used for memory paging and contains the page tables for the currently executing process

VIRTUAL MODE

- ❑ VM can only be enabled in protected mode by VM flag bit set to 1.
- ❑ VM86 mode uses a segmentation scheme identical to that of real mode (for compatibility reasons), which creates 20-bit linear addresses in the same manner as 20-bit physical addresses are created in real mode, but are subject to protected mode's memory paging mechanism

PROTECTION MODE

- ❑ All features of 80386 is enabled here.
- ❑ 32 bits of operations & 32 bits of extended GPRs.
- ❑ 32 bit of Flag register is available
- ❑ PA is calculated by paging , segmentation.
- ❑ All 4 control register available.
- ❑ Max seg size= 4GB as per 32 bit offset register

REAL MODE

- ❑ 80386 works similar to 8086.
- ❑ 16 bit of operations and 16 bit GPRs
- ❑ Only 8086 flags are available.
- ❑ PA=Segment Register*10H+Offset Reg
- ❑ No Paging , Protection & Multitasking
- ❑ No control register available.
- ❑ Max seg size=64 KB as per 16 bits of offset register.

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