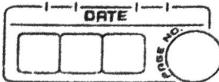


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Assignment No:- 1

Q.1:

ANS.

$$(43)_{10} = (?)_{16} \quad \text{and} \quad (43)_{10} = (?)_{BCD}$$

$$\therefore (i) \quad (43)_{10} = (?)_{16}$$

$$\begin{array}{r} = 16 \mid 43 \\ 16 \quad 11 \quad 2 \\ \hline \end{array} \quad \begin{matrix} \uparrow \\ \downarrow \end{matrix} \quad 11$$

$$(43)_{10} = (B2)_{16}$$

$$\text{ii) } (43)_{10} = (?)_{BCD}$$

$$4 \Rightarrow 0100 \quad \text{and} \quad 3 \Rightarrow 0011$$

$$= 01000011$$

Q.2:

ANS.

$$(8899)_{10} \quad \text{and} \quad (7766)_{10}$$

$$\Rightarrow 8899 = 1000100010011001$$

$$\Rightarrow 7766 = 0111011101010010$$

Now, Adding $(8899)_{10} + (7766)_{10}$

$$\begin{array}{r} 8899 \\ + 7766 \\ \hline \end{array} \quad \begin{array}{r} 1000100010011001 \\ + 0111011101010010 \\ \hline \end{array}$$

$$1111111111111111 \Rightarrow BCD$$

Q.3.

Ans.

computer Architecture

computer Organization.

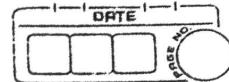
- (i) computer Architecture deals with the way hardware components are connected together to form a computer system.
- (ii) It acts as interaction between hardware & software.
- (iii) It provides the understanding of functionalities at system level.
- (iv) Architecture expresses in terms of instructions, addressing modes and registers.
- (v) While designing a computer system architecture is considered first time.
- (i) computer organisation deals with the structure and behaviour of computer system as seen by user.
- (ii) It deals with the components level of a connection in a system.
- (iii) computer organization explains the exact arrangement of units in the system and their interconnection.
- (iv) whereas organization expresses realization of architecture.
- (v) An organisation is done on basis of architecture.



FOR EDUCATIONAL USE

Subject :- DLCA

Assignment NO:- 2



Q.1

Ans.

$$A = 00000$$

$$Q = 01001$$

$$M = 01000$$

$$-M = 11000$$

$$Q_{-1} = 0$$

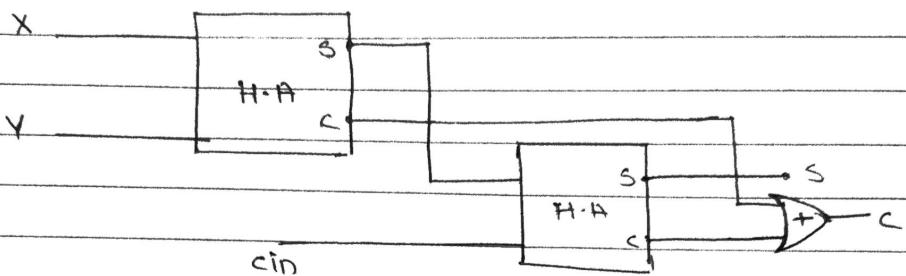
	A	Q	Q ₋₁	M	-M	Action
5	00000	01001	0	01000	11000	Initially $Q \cdot Q_{-1} = 10$
	11000					$A = A - M$
	11000	01001	0			ARS AQQ ₋₁
	01100	00100	1			
4	01100	00100	1			$Q_0 \cdot Q_1 = 01$
	01000					$A = A + M$
	10100	00100	1			ARS AQQ ₋₁
	11010	00010	0			
3	11010	00010	0			$Q_0 \cdot Q_{-1} = 00$
	01101	00001	0			ARS AQQ ₋₁
2	01101	00001	0			$Q_0 \cdot Q_1 = 10$
	11000					$A = A - M$
	00101	00001	0			ARS AQQ ₋₁
	00010	10000	1			
1	00010	10000	1			$Q_0 \cdot Q_{-1} = 01$
	01000					$A = A + M$
	00100	10000	1			ARS AQQ ₀ Q ₁
	00010	01000	0			

Product Available is $(000100000)_2 = 72$

FOR EDUCATIONAL USE

Q.2.

Ans. Fuller Adder using two Half adder and OR Gate:



Expression is given as,

$$S = \bar{x}\bar{y} \text{cin} + \bar{x}y \bar{\text{cin}} + x\bar{y} \bar{\text{cin}} + xy \text{cin}$$

$$C_{out} = \bar{x}y \text{cin} + x\bar{y} \text{cin} + xy \otimes \bar{\text{cin}} + xy \text{cin}$$

Q.3.

Ans. Instruction format:

Every instructions consisting of two field,

- (i) opcode (specifies operation to be performed).
- (ii) operand (it is data on which operation is to be performed).

Depending upon no: of operands in instruction.

we have following instruction format:

(a) zero operand instruction:-

These instructions have implicit operations. Therefore, these instructions does not need to specify the operands.

For ex:- \rightarrow ADD

$\rightarrow ST(0) \leftarrow ST(0) + ST(1)$

5	ST(6)
7	ST(1)
8	ST(2)

(b) one operand instructions:-

Some instructions needs to specify only second operand & first operand is implicit such instruction are one operand instructions.

For ex:- general register.

$\text{ADD } B$ $B = 05$
 $(A) \leftarrow (A) + (B)$ $A = 04$

Accumulator
register.

Above example of 8085 instruction

B, C, D, E, H, L 8 bits.
A

(c) Two operand instruction:-

There are some instruction which needs to specify both operands such instruction are two operand instruction.

Given example is of 8086 instructions.

for example :-

$\text{ADD } AL, BL$ 8-bit :- $\underbrace{AL, AH}_{AX}, \underbrace{BL, BH}_{BX}, \underbrace{CL, CH}_{CX}$
 $(AL) \leftarrow (AL) + (BL)$

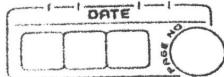
$\text{ADD } AX, BX$ 16-bit :- $\underbrace{AH}_{AX}, \underbrace{AL}_{BX}$
 $(AX) \leftarrow (AX) + (BX)$

(d) Three operation instruction:-

opcode Address 1, Address 2, Address 3

$\text{ADD } A_1, A_2, A_3$

$\text{ADD } [2021], [2023]$	2021	
$[2021] \leftarrow [2021] + [2023]$	2022	05
	2023	04



Above instructions uses three addresses

First two addresses are for two operands on which operation is to be performed. And third address is for next instruction to be executed.

This format of instruction is used for instruction sequencing.

Instruction cycle:-

It is the time required by microprocessor to execute the instruction, it consists of two cycles
Fetch cycle.

Execute cycle:-

This time is used to decode & execute the instruction.

Fetch cycle:-

This is time required to fetch the opcode and operations operands of a instruction.

