VIT Vidyalankar Institute of Technology
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Version 0120-7

Consolidated Academic Administration Plan for the Course

Microprocessor (Core) Sem. IV – Program- Computer Engineering 2021-2022 – Even Semester

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The academic resources available in VIT –

VMIS (ERP)	V-Refer and V-Live	VIT Library	VAC & MOOC Courses
Institute & Department Vision and Mission	Former IA question papers and solutions (prepared by faculty)	Former IA question papers solutions - hardcopy	Value Added Courses (VAC) are conducted throughout the semester & in the semester break - Enrol for the VACs
Program Educational Objectives (PEO)	MU end semester examination question papers and solutions (prepared by faculty)	MU end semester exam question paper & solutions - by faculty, hardcopy	
Program Specific Outcome (PSO)	Class notes and Digital Content for the subject (scanned / typed by faculty)	All text books, reference books, e -books mentioned in the syllabus & AAP	Online courses from NPTEL, Coursera etc. are pursued throughout the semester - Register for the course & get certified
Program Outcome (PO)	Comprehensive question bank, EQ, GQ, PPT, Class Test papers	Technical journals and magazines for reference	
Departmental Knowledge Map	Academic Administration Plan & Beyond Syllabus Activity report	VIT library is member of IIT Bombay Library	Watch former lectures captured in LMS at VIT

1.a Course Objectives (Write in detail – as per NBA guidelines)

Cognitive	What do you want students to know?	- Basics of Microprocessor - Basics of Peripheral chips - Advanced features like multitasking, protection mechanism, superscalar architecture - Instruction set of microprocessor, Assembler	
Affective	What do you want students to think / care about?	- Effective utilization of system resources - Memory efficient code	
Behavioural	What do you want students to be able to do?	- Develop application by using assembly language and mixed language - Designing microprocessor based system as per requirements	

Advice to Students:

Attend every class!!! Missing even one class can have a substantial effect on your ability to understand the course. Be prepared to think and concentrate, in the class and outside. I will try to make the class very interactive. Participate in the class discussions. Ask questions when you don't understand something. Keep up with the class readings. Start assignments and homework early. Meet me in office hour to discuss ideas, solutions or to check if what you understand is correct. The

v-Refer Link for this course -

http://vidyalankarlive.com/vrefer/index.php/apps/files/?dir=/vRefer/CMPN/SEM%20IV/2021-22/MP&fileid=579563

Collaboration Policy:

We encourage discussion between students regarding the course material. However, no discussion of any sort is allowed with anyone on the assignment and homework for the class. If you find solution to some problems in a book or on the internet, you may use their idea for the solution; provided you acknowledge the source (name and page in the book or the website, if the idea is found on the internet). Even though you are allowed to use ideas from another source, you must write the solution in your own words. If you are unsure whether or not certain kinds of collaboration is possible please ask the teacher.

1.b Course Outcome (CO) Statements and Module-Wise Mapping (follow NBA guideline)

CO No.	Statements	Related Module/s
CO1	Describe architecture of x86 processors.	1
CO2	Interpret the instructions of 8086 and write assembly and Mixed language programs.	2
CO3	Explain the concept of interrupts	3
CO4	Identify the specifications of peripheral chip	4
CO5	Design 8086 based system using memory and peripheral chips	5
CO6	Appraise the architecture of advanced processors	6

1.c Mapping of COs with POs (mark S: Strong, M: Moderate, W: Weak, Dash '–': not mapped)

(List of POs is available in V-refer)

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12
CO 1	S	M	-	M	M	W	-	-	-	-	-	-
CO 2	S	S	S	M	M	-	M	W	-	M	-	-
CO 3	S	W	-	-	-	-	-	-	-	-	-	-
CO 4	S	M	-	-	-	-	-	-	-	-	-	-
CO 5	S	M	S	S	M	M	-	-	-	M	-	-
CO 6	M	M	-	-	M	-	-	-	-	-	-	M

1.d Mapping of COs with PSOs (mark S: Strong, M: Moderate, W: Weak, Dash '–':not mapped)

	PSO 1	PSO 2	PSO 3	PSO 4
CO 1	S	M	M	NA
CO 2	S	M	W	NA
CO 3	S	-	-	NA
CO 4	S	-	-	NA
CO 5	S	M	W	NA
CO 6	M	M	W	NA

1.e Teaching and Examination Scheme (As specified by the University) for the Course

Categories	Mathematics	Basic Science & General Engg.	Humanities & Soft Skill	Core Engg./ Technology - Design & Analysis	Multidisciplinary
Tick suitable category	-	-	-	√	-

Subject Code	Subject Name	**Teaching Scheme**			Credits Assigned			
		Theory	Practical	Tutorial	Theory	TW/Practical	Tutorial	Total
CSC405	Microprocessor	03	02	-	03	01	-	04
		-			-			

Subject Code	Subject Name	**Examination Scheme**							
		Theory Marks IA Test			End Sem. Exam Marks	TW	Practical	Oral	Total
		IA 1	IA 2	Average of IA1 and IA2					
CSC405	Microprocessor	20	20	20	80	25	-	-	125
(For Lab Only)									

1.f Faculty-Wise Distribution of all Lecture-Practical-Tutorial Hours for the Course

Divisions	Lecture (Hrs.)	Practical (Hrs.)				Tutorial (Hrs.)			
		Batch 1	Batch 2	Batch 3	Batch 4	Batch 1	Batch 2	Batch 3	Batch 4
A & B	3 SB	2 SB			-	-	-	-	-

A & B	3 ARK	2 ARK	-	-	-	-	-

1.g **Office Hours (Faculty will be available in office in this duration for solving students' query)**

Division	Day	Time (at least 1 Hr. / Division)	Venue (Office Room No.)
A & B	Friday	3:00 pm to 4:00 pm	Faculty cabin

2.a **Syllabus : Module Wise Teaching Hours and % Weightage in University Question Paper**

Module No.	Module Title and Brief Details	Teaching Hrs. for each module	% Weightage in University Question Papers
1	The Intel Microprocessors 8086 Architecture 1.1 8086CPU Architecture, 1.2 Programmer's Model 1.3 Functional Pin Diagram 1.4 Memory Segmentation 1.5 Banking in 8086 1.6 Demultiplexing of Address/Data bus 1.7 Functioning of 8086 in Minimum mode and Maximum mode 1.8 Timing diagrams for Read and Write operations in minimum and maximum mode 1.9 Interrupt structure and its servicing	08	21%
2	Instruction Set and Programming 2.1 Addressing Modes 2.2 Instruction set-Data Transfer Instructions, String Instructions, Logical Instructions, Arithmetic Instructions, Transfer of Control Instructions, Processor Control Instructions 2.3 Assembler Directives and Assembly Language Programming, Macros, Procedures	06	15%-
3	Memory and Peripherals interfacing 3.1 Memory Interfacing - RAM and ROM Decoding Techniques – Partial and Absolute 3.2 8255-PPI-Block diagram, CWR, operating modes, interfacing with 8086 3.3 8257-DMAC-Block diagram, DMA operations and transfer modes. 3.4 Programmable Interrupt Controller 8259-Block Diagram, Interfacing the 8259 in single and cascaded mode.	08	21%
4	Intel 80386DX Processor 4.1 Architecture of 80386 microprocessor 4.2 80386 registers–General purpose Registers, EFLAGS and Control registers 4.3 Real mode, Protected mode, virtual 8086 mode 4.4 80386 memory management in Protected Mode – Descriptors and selectors, descriptor tables, the memory	07	18%

	paging mechanism		
5	Pentium Processor 5.1 Pentium Architecture 5.2 Superscalar Operation, 5.3 Integer &Floating-Point Pipeline Stages, 5.4 Branch Prediction Logic, 5.5 Cache Organization and 5.6 MESI protocol	06	15%
6	Pentium 4 6.1 Comparative study of 8086, 80386, Pentium I, Pentium II and Pentium III 6.2 Pentium 4: Net burst micro architecture. 6.3 Instruction translation look aside buffer and branch prediction 6.4 Hyper threading technology and its use in Pentium 4	04	10%
	Total	**39**	**100%**

2.b Prerequisite Courses

No.	Semester	Name of the Course	Topic/s
1	3	Digital Logic and Computer Architecture	Logic gates, Multiplexers, Demultiplexes, Encoder, Decoder, Latches, Flip-flops , Registers ,control unit, memory, ALU etc.
2	2	Structured Programming Approach	C Programming

2.c Relevance to Future Courses

No.	Semester	Name of the Course
1	VI	System Programming & Complier Construction
2	VIII	High Performance Computing
3	VII, VIII	Project based on Microprocessor/ Microcontroller

2.d Identify real life scenarios / examples which use the knowledge of the subject

Real Life Scenario	Concept Used
Industrial Automation	Interfacing of sensors and actuators
Office Automation	Communication Protocols
Robotics in Healthcare	Precision control, Motors: DC, Servo, Stepper
Automobile Controls & Automation Systems – Engine firing control, Dashboard, Navigation and lighting control, Climate control, GPS, EBD/ABS Systems, Electronic Suspensions, CAN bus systems.	Interfacing of sensors, actuators with standard bus protocols(CAN,I2C,SPI)

Consumer Electronics Systems – Mobile Phones, TV, Fridge, Microwave Oven, Washing Machine, Audio Music Systems, Digital Camera and Camcorder etc.	Advance processors are used

3. Past Results – Division-Wise

Details	Target – May 2022	May 2021	May 2020	May 2019
Course Passing % – Average of 3 Divisions	100%	100%	100%	100%
Marks Obtained by Course Topper (mark/100)	95	90	--	80

	Division A		Division B	
Year	Initials of Teacher	% Result	Initials of Teacher	% Result
Dec 2019	AC	98.5	MS	98.1
Dec 2020	AC	100	AC	100
Dec 2021	MS	100	MS	100

4 All the Learning Resources – Books and E-Resources

4.a List of Text Books (T – Symbol for Text Books) to be Referred by Students

Sr. No	Text Book Titles	Author/s	Publisher	Edition	Module Nos.
1	Microprocessor and Interfacing	Douglas Hall	Tata McGraw Hill	Third Ed	1,2,3,4
2	Microcomputer Systems: 8086/8088 family Architecture, Programming and Design (T)	Liu & Gibson	PHI Publication	NA	1,2,3,4
3	Pentium Processor System Architecture (T)	Tom Shanley & Don Anderson	Addison Wesley	NA	6
4	Advanced Microprocessor	Daniel Tabak	Tata McGraw Hill	Fifth Edition	6
5	The 80386DX Microprocessor: Hardware, Software and Interfacing	Walter A Triebel	Prentice Hall	NA	5

4.b List of Reference Books (R – Symbol for Reference Books) to be Referred by Students

Sr. No	Reference Book Titles	Author/s	Publisher	Edition	Module Nos.
1	8086/8088 family: Design Programming and Interfacing	John Uffenbeck	PHI	Third Edition	1,2,3,4
2	Intel Microprocessors (R)	Barry B. Brey	Pearson Education India	Eighth Edition	1,2,3,4,5,6
3	Processor Architecture and Interfacing (R)	Swati Joshi, Atul Joshi, Hemlata Jadhav	Wiley	--	5,6
4	The X86 Microprocessors: Architecture and Programming (8086 to Pentium)	Das Lyla B	Pearson Education India	--	1,2,3,4,5,6
5	Intel Manuals			--	1,2,3,4,5,6
6	Programmer's Reference Manual for IBM Personal Computers	Steven Armbrust, Ted Forgeron	McGraw Hill	--	2
7	IBM PC Assembly Language and Programming	Peter Abel	Prentice Hall of India	Eighth Edition	2

4.c List of E - Books (E – Symbol for E-Books) to be Referred by Students

Sr. No	E- Book Titles	Author/s	Publisher	Edition	Module Nos.
1	8086_family_Users_Manual_1_.pdf https://edge.edx.org/c4x/BITSPilani/EEE231/asset/8086_family_Users_Manual_1_.pdf	Intel	Intel	--	1,2,3,4
2	INTEL 80386 PROGRAMMER'S REFERENCE MANUAL https://pdos.csail.mit.edu/6.828/2012/readings/i386.pdf	Intel	Intel	--	5
3	Pentium® Processor Family Developer's Manual http://datasheets.chipdb.org/Intel/x86/Pentium/241428_4.PDF	Intel	Intel	--	6

4.d Reading latest / top rated research papers (at least 5 papers)

Name of Paper	Authors with Background	Published in		Problem Statement
		Date	Journal	
Demonstration of a Single-Flux-Quantum Microprocessor Operating With Josephson-CMOS Hybrid Memory	Yuki Hironaka Affiliation Department of Electrical and Computer Engineering Yokohama National University Yokohama, Japan	2020	IEEE Transactions on Applied Superconductivity	A single-instruction SFQ microprocessor whose data memory is implemented using Josephson-CMOS hybrid memory with a 16 × 4-b accessible address space.
Design of an 8-bit Bit-Parallel RSFQ Microprocessor	Pei-Yao Qu Affiliation State Key Laboratory of Computer Architecture Institute of Computing Technology Chinese Academy of Sciences, Beijing, China	2020	IEEE Transactions on Applied Superconductivity	The proposed microprocessor processes 8-bit data each clock cycle. Ten different instructions are executed. The microprocessor mainly consists of an on-chip instruction memory, two data registers, an instruction decoder, an 8-bit bit-parallel arithmetic logic unit, and a program counter.
Runtime Performance Optimization of 3-D Microprocessors in Dark Silicon	Hai Wang Affiliation State Key Laboratory of	2021	IEEE Transactions on Computers	The new method determines many runtime settings of the 3-D system on the fly, including the active core and cache bank positions, active

	Electronic Thin Films and Integrated Devices University of Electronic Science and Technology of China Chengdu, Sichuan, China			cache bank number, and the voltage/frequency (V/f) level of each active core, which optimizes the performance of the 3-D microprocessor under thermal constraint.
Updates on Testing Microprocessors Effectively	Heather Quinn Also published under: Heather M. Quinn, H. Quinn Affiliation Los Alamos National Laboratory, USA	2021	IEEE Transactions on Nuclear Science	a discussion of the changes to both the input vectors and the checkers are presented with test results showing the effect of both on the previous and new algorithms.

4.e **Based on research paper an identify the current Problem statement**

Problem Statement	Used in					
	Quiz	Assignment	Lab	Mini Project	Poster Presentation	Test
Overview of modern computers and modern technologies used to build microprocessors	√	√	√		-	-

4.f **Identify Companies / Industries which use the knowledge of the subject and thus may provide Internships and final Placements**

Name of the Company	To be / Contacted for		
	Student Internship	Student Final Placement	Faculty Internship
IBM India Pvt Ltd, Bengaluru	√	√	-
TCS	√	√	
Wipro	√	√	
Cognizant	√	√	
Accenture	√	√	
Infosys	√	√	

4.g **Identify suitable relevant TOP Guest Speakers from Industry (CS50 Lecture by Mark Zuckerberg - 7 December 2005 - YouTube)**

Name of the Identified Guest Speaker	Designation	Name of the Company
Mr. Mubeen Abbas	Marketing Manager	NXP Semiconductors N.V.
Mr. Rangarajan Anand	Product Manager	Microchip Technology Inc.

4.h **Identify relevant Technical competitions to participate [Competitions -Paper Presentations, Projects, Hackathons, IVs etc..]**

Name of the Relevant Technical Competition Identified to participate	Organized by	Date of the Event
Texas Instruments Innovation Challenge	Texas Instruments, India	March-April Every Year
The Freescale Cup	Freescale Community, india	November-December Every Year
Hardware Hackathon	Centre for Electronics Design and Technology, NSIT, Delhi	June-July Every Year
Intel IoT Roadshow	Intel	August-September Every Year
Intel India Embedded Challenge	Intel	November-December Every Year
National Instruments NIYANTRA	National Instruments	March-April Every Year

4.i **Identify faculty in TOP schools / Universities who are teaching same / similar subject and develop rapport e.g. Exchange Lecture Material (Assignments / Tests / Project etc..), Joint Paper Publication**

University	Name of the Course	Name of Faculty	Type of Collaboration		
			Exchange of Lecture Material	Joint Publication/ Research	Other
IIT, Mumbai	Microprocessors	Dr. Rajbabu Velmurugan (rajbabu[AT]ee.iitb.ac.in)	-	-	√

4.j **Web Links and Names of Magazines, Journals, E-journals – [VIT is member of IIT Bombay Library]**

Refer online journals subscribed in VIT library. You can also access IIT Bombay online library for journals from IITB campus.

Sr. No.	Web-Links and Names of Journals and E-Journals Recommended to Students for this Course	Web-Links and Names of Magazines Recommended to Students for this Course	Module Nos.
1	IEEE-xplore Journals of Electronics & Communications Society	Electronics for you	All
2	IEEE-xplore Control and computations Society	Elector India Magazine	All
3		IEEE Electronics online e-magazine	All

4.k **Module Best Available in - Tick ONE best resource [from *4.a* to *4.d* in this AAP] & give details**

Module No.	Category (Please Tick Mark) - √						Available In VIT Library ?		Details of the Resource (i.e. Name, Chapter no.etc.)
	Book			Magazine	Journals				
	Text	Reference	E-Book		Regular	E-Journal	Y	N	
1			√					√	8086_family_Users_Manual_1_.pdf https://edge.edx.org/c4x/BITSPilani/EEE231/asset/8086_family_Users_Manual_1_.pdf 1. Chapter -1 Page 1-1 to 1-14 2. Chapter -2 Page 2-1 to 2-14
2			√					√	8086_family_Users_Manual_1_.pdf https://edge.edx.org/c4x/BITSPilani/EEE231/asset/8086_family_Users_Manual_1_.pdf 1. Chapter – 2 Page 2-29 to 2-92
3			√					√	8086_family_Users_Manual_1_.pdf https://edge.edx.org/c4x/BITSPilani/EEE231/asset/8086_family_Users_Manual_1_.pdf 1. Chapter – 2 Page 2-22 to 2-29
4			√					√	R1 Chapter 7 # Pages 328 – 394 R1 Chapter 8 # Pages 423 – 469 R1 Chapter 9 # Pages 475 – 517
5			√					√	INTEL 80386 PROGRAMMER'S REFERENCE MANUAL https://pdos.csail.mit.edu/6.828/2012/readings/i386.pdf 1. Chapter 2 Page 22 to 44 2. Chapter 4 Page 85 to 90 3. Chapter 5 Page 91 to 105 4. Chapter 6 Page 105 to 129 5. Chapter 7 Page 130 to 144 6. Chapter 15 Page 217 to 222
6			√					√	Pentium® Processor Family Developer's Manual http://datasheets.chipdb.org/Intel/x86/Pentium/241428_4.PDF 1. Chapter 2 Page 2-1 to 2-4 2. Chapter 3 Page 3-1 to 3-27
7	-	-	-	-	-	-	-	-	-

4.l **Referred to any top-rated university in that subject for content**

University	Name of the Course	Name of Faculty	Date of Delivery of the Course	Remarks
California State University, Long Beach	Microprocessors	DR. I-HUNG KHOO	--	--

4.m **Faculty received any certification related to their subject. List of Certifications Identified / Done**

Course	Certifying Agency	Certification		Remarks
		Done on	Proposed to be on	
Switching circuits and logic design	NPTEL	June 2018	November 2018	Successfully completed
Computer organization and architecture : A pedagogical aspect	NPTEL	January 2019	April 2019	Successfully completed

4.n **Completed subject wise/cluster wise training with cluster mentor. List of relevant Refresher Course Identified / Done**

Course	Certifying Agency (As suggested by DAB/Cluster Mentor/Industry/University other than MU)	Certification		Remarks
		Done on	Proposed to be on	
Pedagogy	Learning to Teach Online - Coursera	30/04/2020	April 2020	Successfully completed
PBL	'Design Thinking' by ATAL Academy	7/12/2020	11/12/2020	Successfully completed
Sub. Content Training	'Gurucool program on emerging trend in technology by IBM – Build-a Thon	September 2020	October 2020	Successfully completed

4.o **Best Practices Identified and adopted**

No.	Item	Best Practices Identified		
		Univ. 1	Univ. 2	Univ. 3

1	Microsite	California State University, Long Beach		
2	Video Lectures	IIT, Mumbai	IIT, Madras	IIT, Kharagpur
3	Assignments	California State University, Long Beach		
4	Mini Project			
5	Assessment Metric			
6	Quizzes	IIT, Mumbai	IIT, Madras	IIT, Kharagpur
7	Labs/ Practical (PBL)	IIT, Mumbai California State University, Long Beach	IIT, Madras	IIT, Kharagpur
8	Tests			
9	Etc			
10	Peer Assessment etc.	IIT, Mumbai	IIT, Madras	IIT, Kharagpur

4.p Web Links for Online Notes/YouTube/VIT Digital Content/VIT Lecture Capture/NPTEL Videos

Students can view lectures by VIT professors, captured through LMS 'Lecture Capture' in VIT campus for previous years.

No.	Websites / Links	Module Nos.
1	http://www.ques10.com/p/10876/explain-the-interrupt-structure-of-8086-processor/ http://www.bime.ntu.edu.tw/~ttlin/Course15/lecture_notes/C15_LECTURE_NOTE_11(2%20in%201).pdf	Module 3 Interrupts

2	http://nptel.ac.in/courses/108107029/module9/lecture1/lecture1.pdf http://aturing.umcs.maine.edu/~meadow/courses/cos335/Intel8255A.pdf	Module 48255
3	http://nptel.ac.in/courses/108107029/module10/lecture1/lecture1.pdf https://technicalpublications.org/media/freedownloads/8253_54-1.pdf	Module 48253
4	https://pdos.csail.mit.edu/6.828/2014/readings/hardware/8237A.pdf http://nptel.ac.in/courses/Webcourse-contents/IIT%20Kharagpur/Embedded%20systems/Pdf/Lesson-16.pdf	Module 48237
5	http://nptel.ac.in/courses/108107029/module11/lecture2/lecture2.pdf http://www.cs.put.poznan.pl/rklaus/AK/katalogi%20pdf/drKlaus%208259a.pdf http://gradestack.com/Microprocessors-and/8259-Interfacing-with/8259-Interfacing-With/19322-3912-38212-study-wtw	Module 38259
6	https://pdos.csail.mit.edu/6.828/2008/readings/i386.pdf	Modul

		e 5 8 0 3 8 6

4.q Recommended MOOC Courses like Coursera / NPTEL / MIT-OCW / edX/VAC etc.

Sr. No.	MOOC Course Link	Course conducted by – Person / University / Institute / Industry	Course Duration	Certificate (Y / N)
1	https://swayam.gov.in/nd1_noc20_ee11/preview	Prof. Shaik Rafi Ahamed IIT Guwahati (NPTEL)	12 weeks	Y
2	https://nptel.ac.in/courses/108/105/108105102/	Prof. Shantanu Chattopadhyay (NPTEL)	12 Weeks	Y
3	https://www.classcentral.com/course/swayam-microprocessors-and-microcontrollers-9894 4 https://www.mooc-list.com/tags/microprocessors	Chester Rebeiro IIT Madras	8 Week	Y

5 Consolidated Course Lesson Plan

	From (date/month/year)	To (date/month/year)	Total Number of Weeks
Semester Duration	10/01/2022	30/04/2022	15

Week	Lecture no.	Module No.	Lecture Topics / IA 1 and IA 2 / BSA planned to be covered	Actual date of Completion	COs	Recommended Prior Viewing / Reading	
						Lecture No. (on LMS)	Chapter No. / Page Nos./ Books/ Web Site
1	1	1	8086/8088 CPU Architecture, Programmer's Model		CO1		**R1 Page 99-106** **E2** 1. Chapter – 2 Page 2-29 to 2-92
2	2	2	Data Transfer Instructions Arithmetic Instructions		CO2		**E2** 1. Chapter – 2 Page 2-29 to 2-92
			Transfer of control Instructions Processor Control Instructions		CO2		**E2** 1. Chapter – 2 Page 2-29 to 2-92
3	3	2	Logical Instructions String Instructions		CO2		**E2**

							1. Chapter – 2 Page 2-29 to 2-92
			Assembler Directives and Assembly Language Programming, Macros, Procedures Programming based on DOS and BIOS Interrupts (INT 21H, INT 10H)		CO2		**E2** 1. Chapter – 2 Page 2-29 to 2-92
4	4	2	Mixed Language Programming with C Language and Assembly Language.		CO2		**E2** 1. Chapter – 2 Page 2-29 to 2-92 T1 Page 2.7-2.9 R1 Page 106 – 114
5	5	1	8086 pin configuration, Banking in 808 Demultiplexing of Address/Data bus		CO1		E1 1. Chapter -1 Page 1-1 to 1-14 2. Chapter -2 Page 2-1 to 2-14
		1	Study of 8284 Clock Generator Study of 8288 Bus Controller		CO1	Lect 4	T2 Page 310 – 324
6			IA TEST 1		CO1, CO2		
7	6	1 & 3	Functioning of 8086 in Minimum mode and Maximum mode Timing diagrams for Read and Write operations in minimum and maximum mode Types of interrupts Interrupt Service Routine Interrupt Vector Table Servicing of Interrupts by 8086 microprocessor		CO1		T2 Page 314 – 329 8086_family_Users_Manual_1_.pdf https://edge.edx.org/c4x/BITSPilani/EEE231/asset/8086_family_Users_Manual_1_.pdf 1. Chapter -1 Page 1-1 to 1-14 2. Chapter -2 Page 2-1 to 2-14
8	7	3	Programmable Interrupt Controller 8259 – Block Diagram, Interfacing the 8259 in single and cascaded mode, Operating modes, programs for 8259 using ICWs and OCWs		CO3 CO3		R1 Chapter 7 # Pages 483 – 512
9	8	4			CO4		

			Memory Interfacing - RAM and ROM Decoding Techniques – Partial and Absolute		CO4		R1 Chapter 7 # Pages 328 – 394
10	9	4	8255-PPI – Block diagram, Functional PIN Diagram, CWR, operating modes, interfacing with 8086.		CO4 CO4		R1 Chapter 8 # Pages 423 – 469
11	10	4	8253 PIT - Block diagram, Functional PIN Diagram, CWR, operating modes, interfacing with 8086		CO4		R1 Chapter 8 # Pages 423 – 469
			8257-DMAC – Block diagram, Functional PIN Diagram, Register organization, DMA operations and transfer modes		CO4		R1 Chapter 9 # Pages 475 – 517
12	11	5	Architecture of 80386 microprocessor 80386 registers, General purpose Registers, EFLAGS and Control registers		CO5		E2 1. Chapter 2 Page 22 to 44 2. Chapter 4 Page 85 to 90 3. Chapter 5 Page 91 to 105 4. Chapter 6 Page 105 to 129 5. Chapter 7 Page 130 to 144 6. Chapter 15 Page 217 to 222
			Real mode, Protected mode, virtual 8086 mode		CO5		E2 1. Chapter 2 Page 22 to 44 2. Chapter 4 Page 85 to 90 3. Chapter 5 Page 91 to 105 4. Chapter 6 Page 105 to 129 5. Chapter 7 Page 130 to 144 6. Chapter 15 Page 217 to 222
13	12	5 & 6	80386 memory management in Protected Mode – Descriptors and		CO5		E2 1. Chapter 2 Page 22 to 44

			selectors, descriptor tables, the memory paging mechanism				2. Chapter 4 Page 85 to 90 3. Chapter 5 Page 91 to 105 4. Chapter 6 Page 105 to 129 5. Chapter 7 Page 130 to 144 6. Chapter 15 Page 217 to 222
			Pentium Architecture Superscalar Operation,		CO6		E3 1. Chapter 2 Page 2-1 to 2-4 2. Chapter 3 Page 3-1 to 3-27
14	13	6	Integer & Floating Point Pipeline Stages, Branch Prediction Logic,		CO6		E3 1. Chapter 2 Page 2-1 to 2-4 2. Chapter 3 Page 3-1 to 3-27
			Cache Organisation and MESI Model		CO6		E3 1. Chapter 2 Page 2-1 to 2-4 2. Chapter 3 Page 3-1 to 3-27

6 Rubric for Grading and Marking of Term Work (inform students at the beginning of semester)

Lecture + Practical (% Attendance) & Marks	Assign-ments	Tutorial	Lab / Practical Performance	Lab Journal Assessment	Class Tests (Other than IA)	Pop Quiz	Take Home Test	Total
05	05	--	05	05	05	--	--	25

7 Assignments / Tutorials Details

Assignment/ Tutorial No.	Title of the Assignments / Tutorials	CO Map	Assignment/ Tutorials given to Students on	Week of Submission
1	Fundamentals of 8086 Processor	CO1	4th Week July 2020	1st Week August 2020
2	Addressing modes and Instructions	CO2	3rd week August 2020	4th Week August 2020
3	Interrupts	CO3	2nd Week September	3rd Week September
4	80386 Processor	CO5	1st Week October	2nd Week October

Analysis of Assignment / Tutorial Questions and Related Resources

Assignment / Tutorial No.	Week No.	Type* (√)			Module No.	Based on #			Question Type (√)	
		R	PQ	OBT		Text Book	Reference Book	Other Learning Resource	MU EQ	Thought Provoking
1	3	√			1	T1	R1		√	
2	6	√			2			E1	√	
3	9	√			3		R1		√	
4	11	√			5			E2	√	

* Tick (√) the Type of the Assignment: Regular (R); Pop Quiz (PQ) ; Open Book Test for TE/BE/ME (OBT)
# Write number for text book, reference book, other learning resource from this AAP – *from Points 4.a to 4.d*

8 Internal Assessment / Other Class Test / Open Book Test (OBT)/Take Home Test (THT) Details

Tests	Test Dates	Module No.	CO Map	IA Question Paper Pattern	Policy
1st IA Test		1,2	CO1, CO2	Q1 – MCQ - 10 Marks Q2 – 1 numerical 5 Marks Q3 – 1 numerical 5 Marks 20 marks each for IA 1 & 2	No IA Re-test IA is a Head of passing *
2nd IA Test		3,4,5,6	CO3, CO4, CO5, CO6		
Pop Quiz	Every Lecture	2	CO2	MCQ	--
Take Home Test-1	5th Week	1,2	CO1, CO2	Q1 – MCQ - 10 Marks Q2 – 1 numerical 5 Marks Q3 – 1 numerical 5 Marks	--

Take Home Test-2	11th Week	3,4,5,6	CO3, CO4, CO5, CO6		--

*** Failures of IA test (IA1+IA2) shall appear for IA test in the next semester. There is no provision for re-test in the same semester.**

9.a Practical Activities – Regular Experiments

Practical No.	Module No.	Title of the **Regular Experiments**	Topics to be highlighted	CO Map
1	2	Study of tools used for programming of microprocessors (TASM)	Turbo Assembler	CO2
2	2	Develop assembly language code to add, subtract two, 8-bit numbers which will occupy minimum program memory space	Instruction set & Addressing modes	CO2
3	2	Develop assembly language code to multiply, divide, two, 8-bit numbers which will occupy minimum program memory space	Instruction set & Addressing modes	CO2
4	2	Develop assembly language code to convert the input from key board to the format which can be used for processing internally	Instruction set & Addressing modes	CO2
5	2	Develop Assembly language program using 8086 microprocessor for block copy, block exchange with and without string instructions	Data Transfer Instructions	CO2
6		Develop a 8086 program for block exchange operation	Data Transfer Instructions	CO2
7	2	Given a bucket of ten, 8-bit numbers, develop assembly language code to find out smallest and largest element out of the bucket	Instruction set & Addressing modes	CO2
8	2	Develop a 8086 program to count no of odd and even numbers in given array	Instruction set & Addressing modes	CO2
9	2	Develop 8086 Assembly Language Program to implement bubble sort technique to arrange the Numbers in given bucket of 8 bit numbers in (a) Ascending Order (b) Descending Order.	Sorting logics such as bubble-sort.	CO2
10	2	Develop 8086 Assembly Language Program to – Find whether user entered string is Palindrome or not.	Palindrome Logic	CO2

9.b Practical Activities – Newly Added Experiments

Practical No.	Module No.	Title of the **Newly Added Experiments**	Concepts to be highlighted	CO Map

1	2	Develop 8086 Assembly Language Program to implement bubble sort technique to arrange the Numbers in given bucket of 8 bit numbers in (a) Ascending Order (b) Descending Order.	Sorting logics such as bubble-sort.	CO2
2	2	Develop 8086 Assembly Language Program to – Find whether user entered string is Palindrome or not.	Palindrome Logic	CO2

9.c Practical Activities – PBL Experiments

Practical No.	Module No.	Title of the **PBL Experiments**	Concepts to be highlighted	CO Map
1	2	Develop assembly language code to convert the input from key board to the format which can be used for processing internally	Instruction set & Addressing modes	CO2
2	2	Develop assembly language code to add, subtract two, 8-bit numbers which will occupy minimum program memory space	Instruction set & Addressing modes	CO2

10 Beyond Syllabus Activities for Gap Mitigation

No.	Type of the Activity	Activities	Details – no of attendees, guest, feedback, mark sheet, report
1	**Experiential learning/Interaction with Outside World**	1- Guest Lectures by Industry Expert	Planned in the 7th Week
		2- Workshops	-
		3- Mini Project	-
		4- Industrial Visit	-
		5- Any other activity	-
2	**Collaborative & Group Activity**	1- Poster Presentation	-
		2- Minute Papers	-
		3- Students Seminars	Planned in the 8th Week
		4- Students Debates	-
		5- Panel Discussion / Mock GD	-

		6- Mock Interview	-
		7- Any other activity	-
3	**Co-Curricular Activity**	1- Informative videos (NPTEL/Youtube /TEDx/ MIT OW/edX)	Planned in the 2nd Week
		2- Lecture Capture Usage	-
		3- Any other activity	-
4	**Tests & Assessments**	1- Class Tests/ Weekly Tests	-
		2- Pop Quiz	Planned in 10th week
		3- Mobile App Based Quiz	-
		4- Open Book	-
		5- Take Home Test	-
		6- Any other activity	-

11.1 One-on-One Academic Mentoring Meetings done

No.	Name of Mentee	Date of One-On-One Meeting		
		Beginning of Sem.	After Mid Term Results	Before End Sem.

11.2 Identify Financial Concerns and refer appropriately

No.	Name of Mentee			
		Individual Goals Identified	Any Financial Concern which needs to be referred to	Any Emotional Concern to be referred to

*** Do not delete any activity. Give details for planned events. Write 'NA' for activity Not Planned.**

Consolidated Academic Administration Plan Prepared by (mention all theory teaching faculty names with signature)

Please write below your name and sign with date of the external cluster mentor meeting

Ajitkumar Khachane	 Suvarna Bhat	---- Faculty 3

---- External Industry Mentor	External Academic Mentor	 VIT Cluster Mentor	Program HOD