

## Setting up ASAP7 PDK

Copy the folder **asap7** into your home directory, this will be your work directory for 7nm:

```
cp -r /home/eng/v/vks160030/asap7/ ~
```

```
cd asap7
```

## Running Virtuoso

Every time you quit, before starting Virtuoso or Innovus, type in the following commands.

```
. /home/eng/v/vks160030/profile.ic-adv_asap7
```

```
virtuoso
```



```
File Tools Options Help

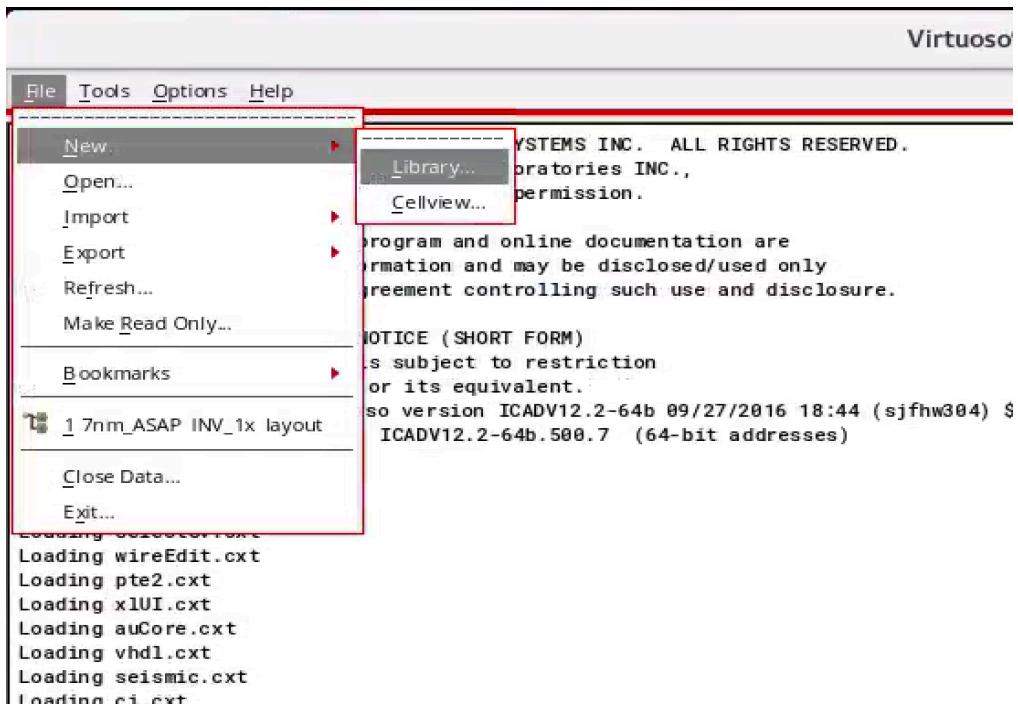
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set forth at FAR 1252.227-19 or its equivalent.
Program: @(#)SCDS: virtuoso version ICADV12.2-64b 09/27/2016 18:44 (sjfhw304) $
Sub version: sub-version ICADV12.2-64b.500.7 (64-bit addresses)
Loading geView.cxt
Loading menuBuilder.cxt
Loading schView.cxt
Loading selectSv.cxt
Loading wireEdit.cxt
Loading pte2.cxt
Loading xUI.cxt
Loading auCore.cxt
Loading vhdl.cxt
Loading seismic.cxt
Loading ci.cxt
Loading ams.cxt
Virtuoso Framework License (111) was checked out successfully. Total checkout time was 0.03s.
// 
// Calibre Skill Interface * (v2017.3_18.12) *
// 
// Copyright Mentor Graphics Corporation 2005 .
// All Rights Reserved.
// THIS WORK CONTAINS TRADE SECRET AND PROPRIETARY INFORMATION
// WHICH IS THE PROPERTY OF MENTOR GRAPHICS CORPORATION
// OR ITS LICENSORS AND IS SUBJECT TO LICENSE TERMS.
// 
// 
*WARNING* Unable to open file /home/eng/v/vks160030/Desktop/ASAP7_PDKandLIB_v1p5/cdslib/setup/cdsenv for env load
### ##### #### ##### ###### ###### ## ##
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```

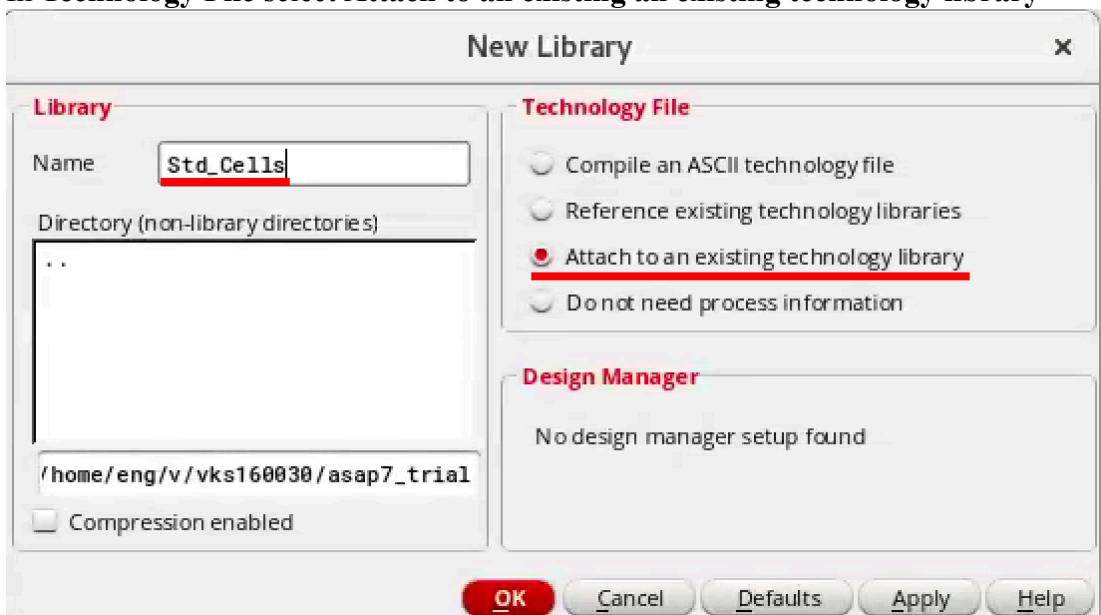
## Create New Library

File -> New -> Library



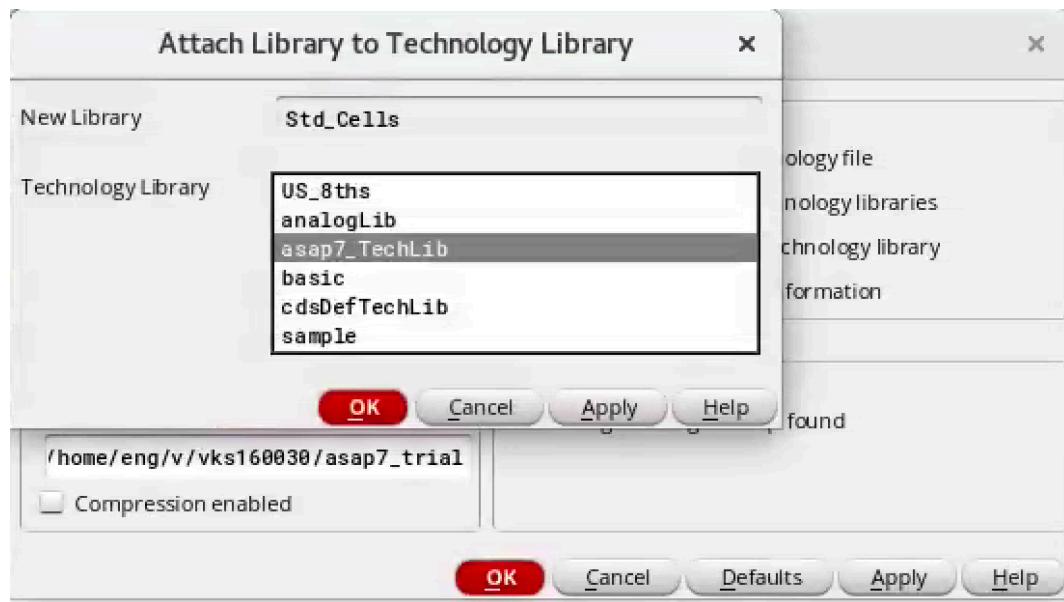
In **Library** give the name of the library (can be any other name too)

In **Technology File** select **Attach to an existing an existing technology library**



Click **OK**

Select **asap7\_TechLib**

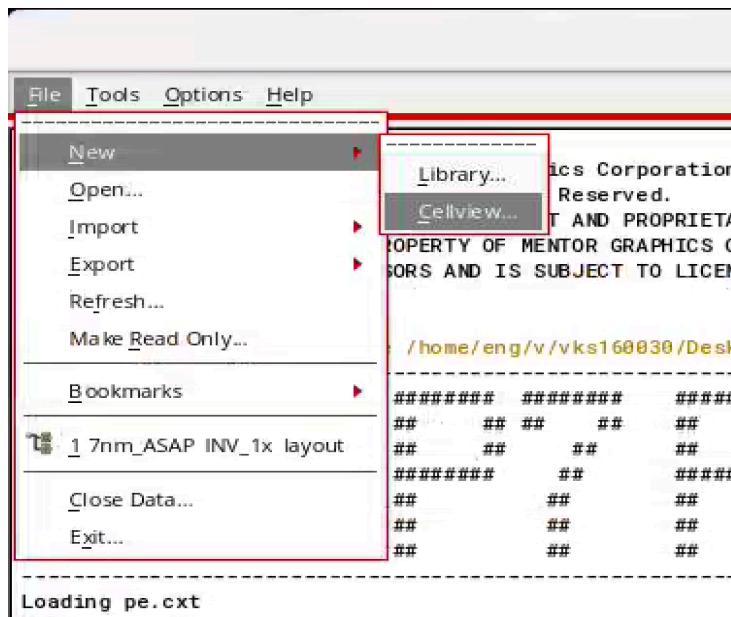


Click **OK**

**Create New Cell View**

**For Layout**

File -> New -> Cellview

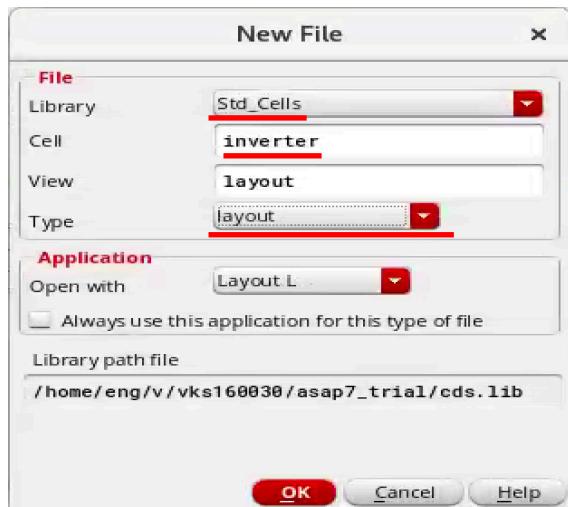


In **File**,

**Library:** Select the name of the library which you created in the previous step

**Cell:** Give the name of the standard cell you will be designing

**Type:** select **layout**

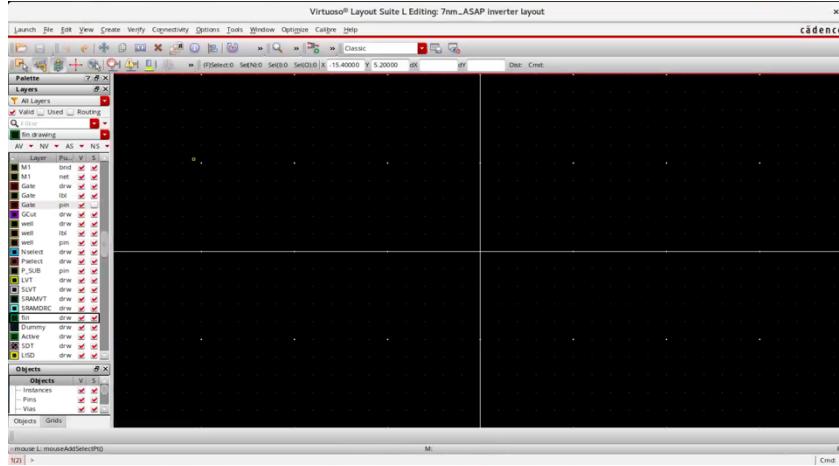


Click **OK**

If you get this warning, click **Yes** and proceed

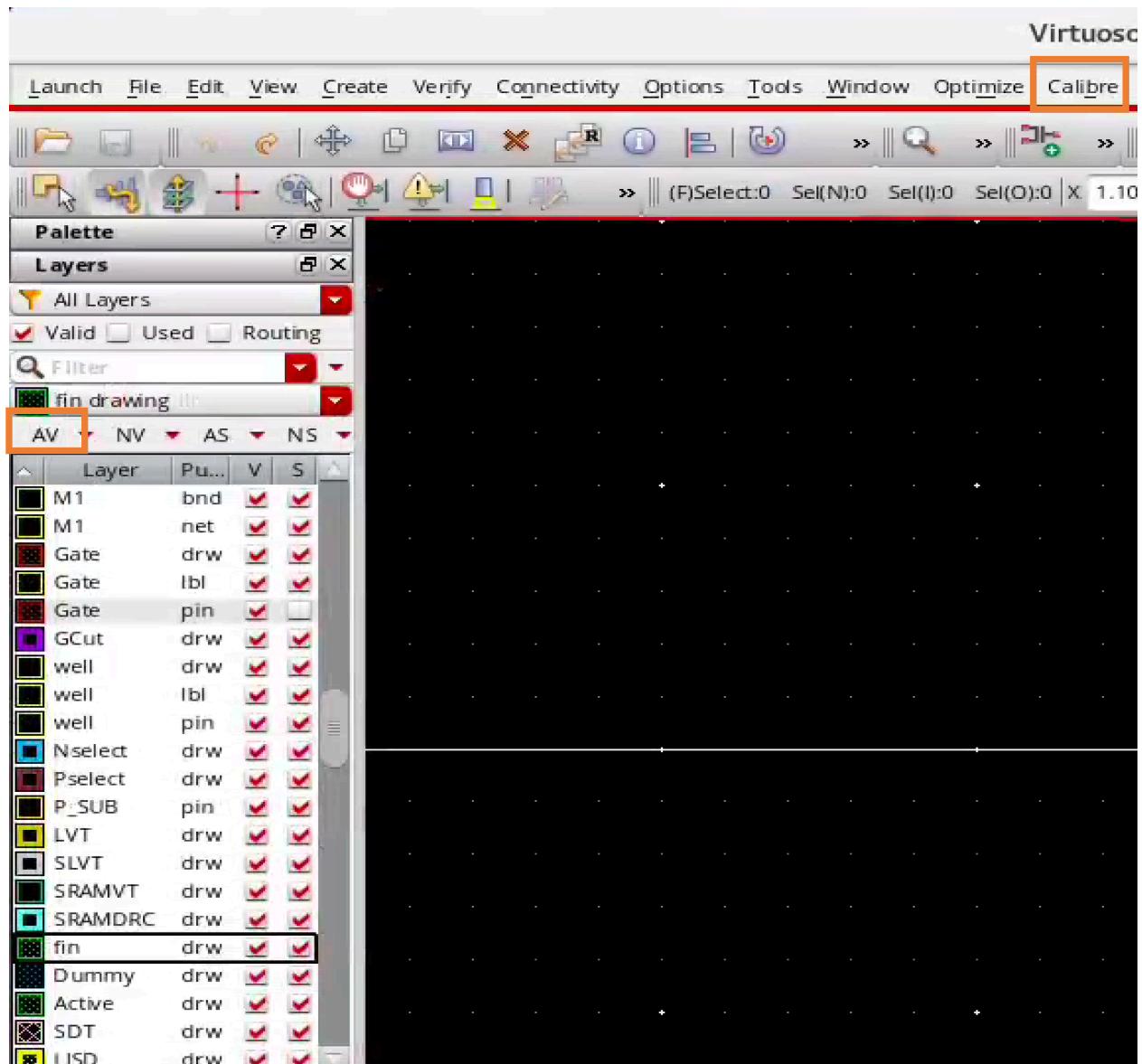


An empty layout view should open

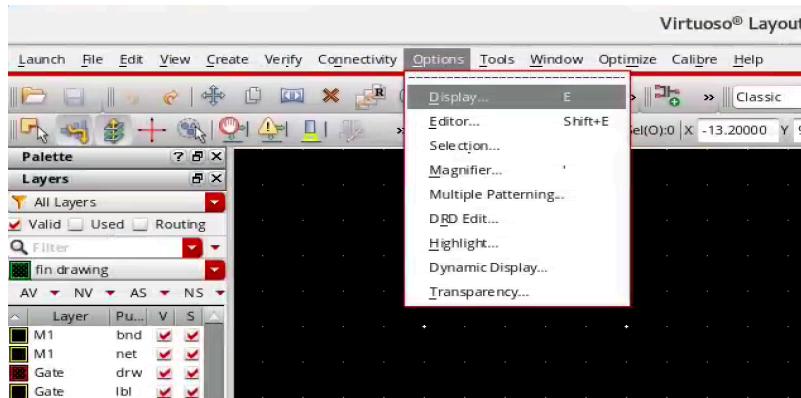


Before starting inverter layout, 3 things should be done:

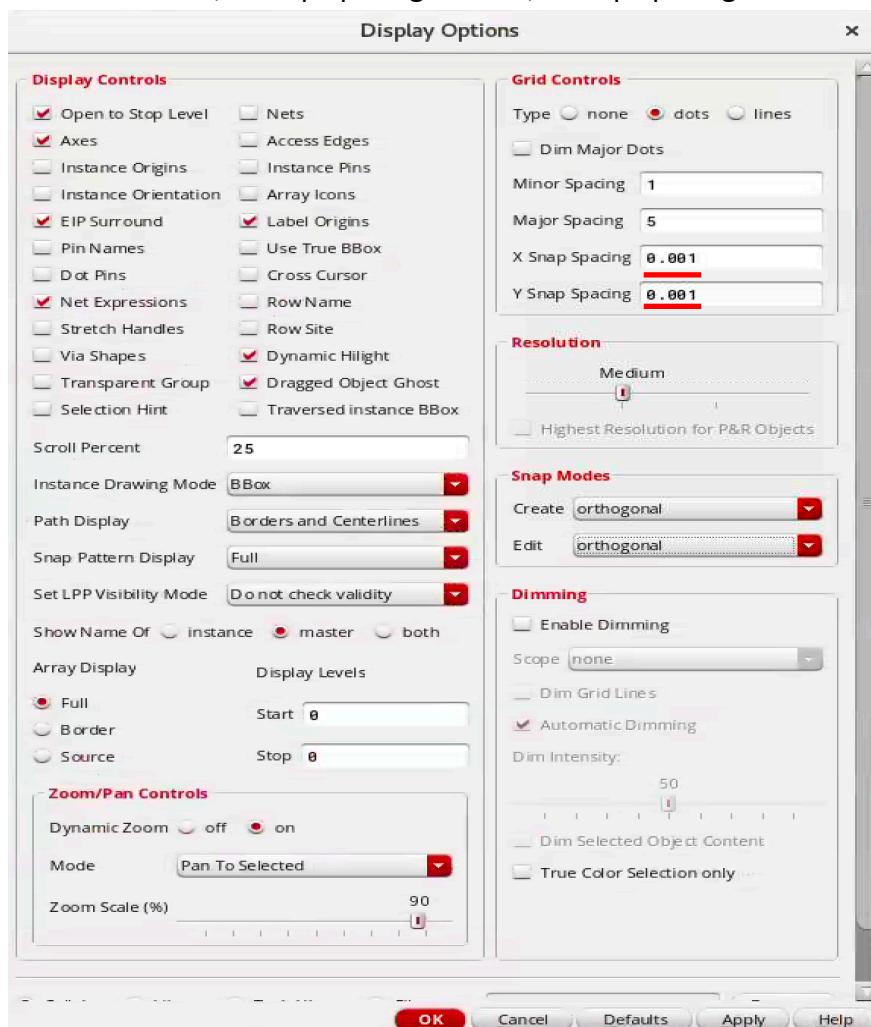
- 1) On the left side of the screen, in **layers** click on **AV** and check if you have layers such as fin drw, Gate drw, LISD drw.
- 2) On top of the screen, in the tool bar look for **Calibre**. If you do not find Calibre, it means that you haven't setup environment properly. Go back to **Setting up ASAP7 PDK** and repeat.



3) Go to Options -> Display



In Grid Controls, X Snap Spacing = 0.001, Y Snap Spacing = 0.001



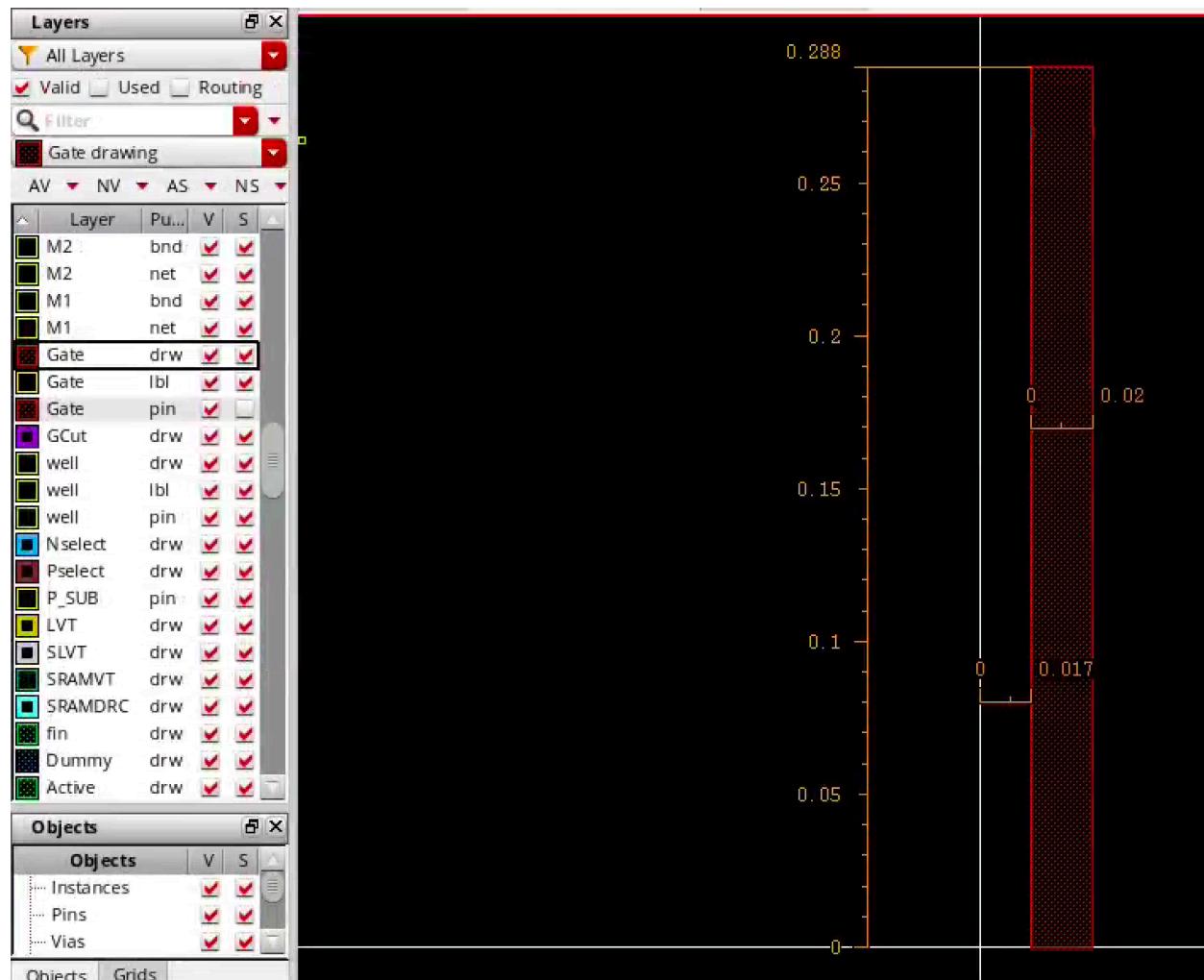
Now you can proceed to layout drawing

### Inverter Layout Tutorial

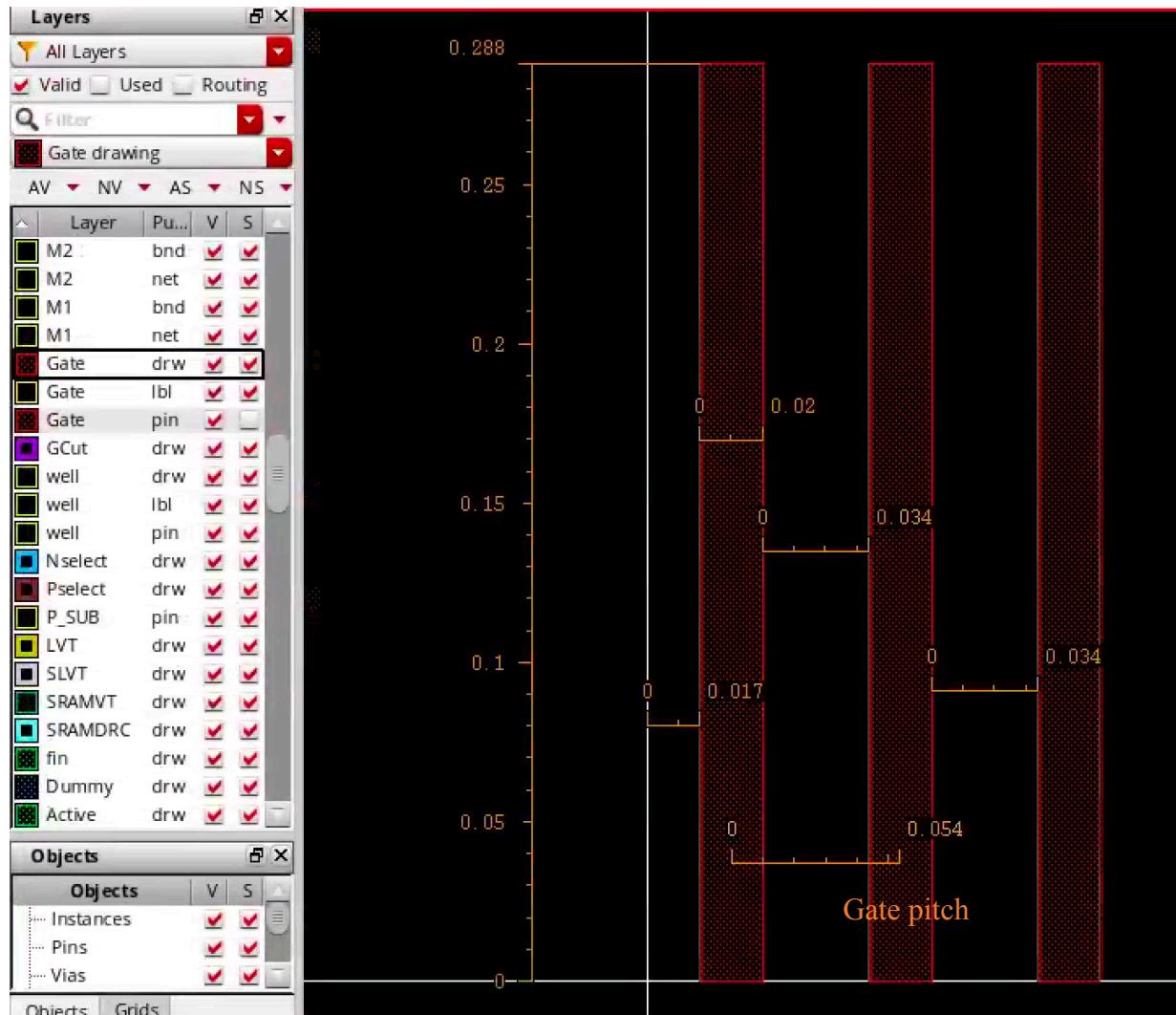
### Layout Rules:

- Gate width = 0.02um
- Gate pitch = 0.054um
- Fin width = 0.007um
- Fin pitch = 0.027um
- Cell height = 0.288um
- SDT width = 0.024um
- Minimum width M1, M2, M3 = 0.018um
- V0, V1, V2 = 0.018um x 0.018um

- i) Select **Gate drawing** layer and Press **R** to draw the layer. Draw the layer with a width of 0.02u and a height of 0.288u. Place the Gate at a distance of 0.17u from the reference y-axis as shown in the picture below.

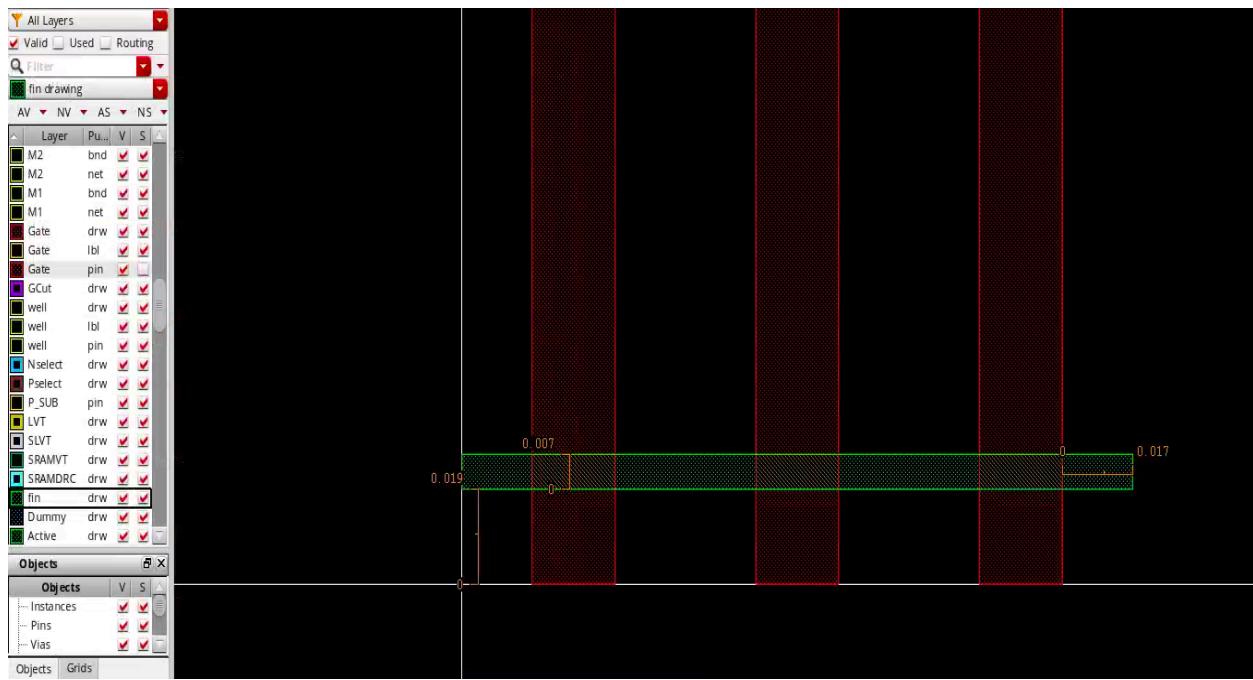


Place 2 more gates beside this gate, the distance between each gate should be 0.034um and gate pitch = 0.054um

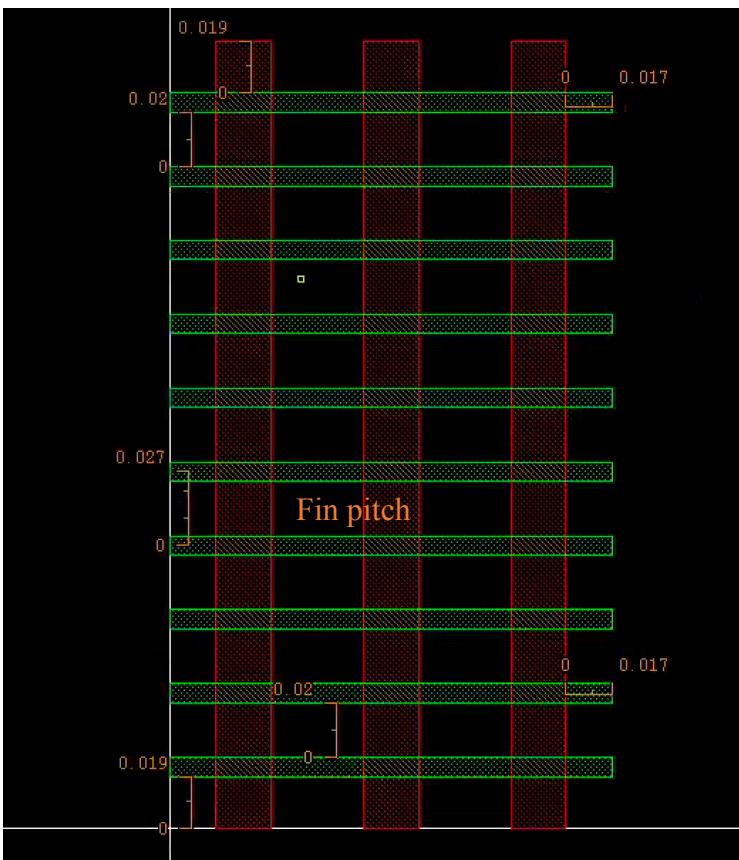


The outer two gates are dummy gates.

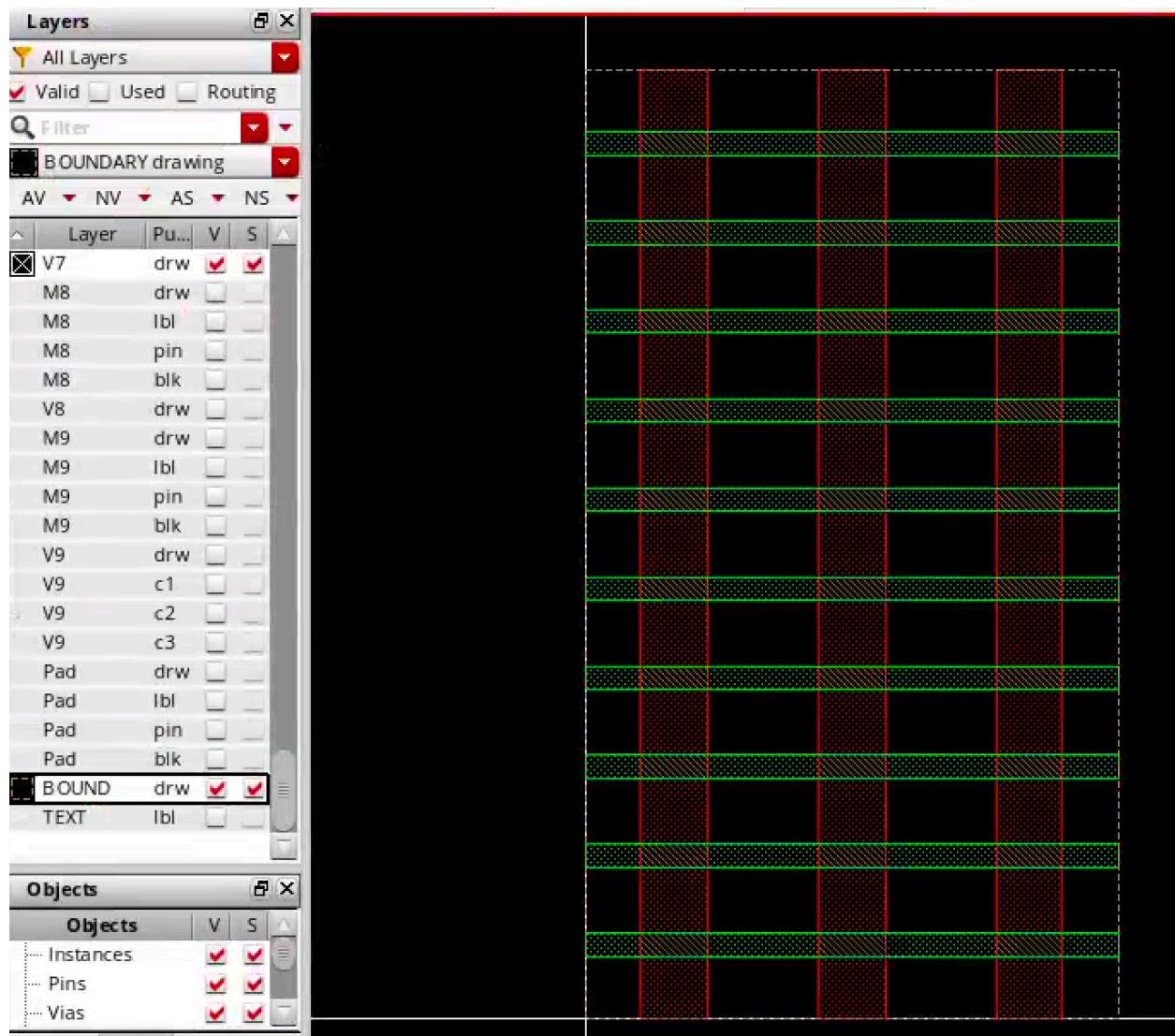
- ii) Select **fin drawing** layer. Draw the first fin as shown in the picture below, it should be touching the y-axis and distance from the x-axis is 0.019um. The width of fin must be 0.007um.



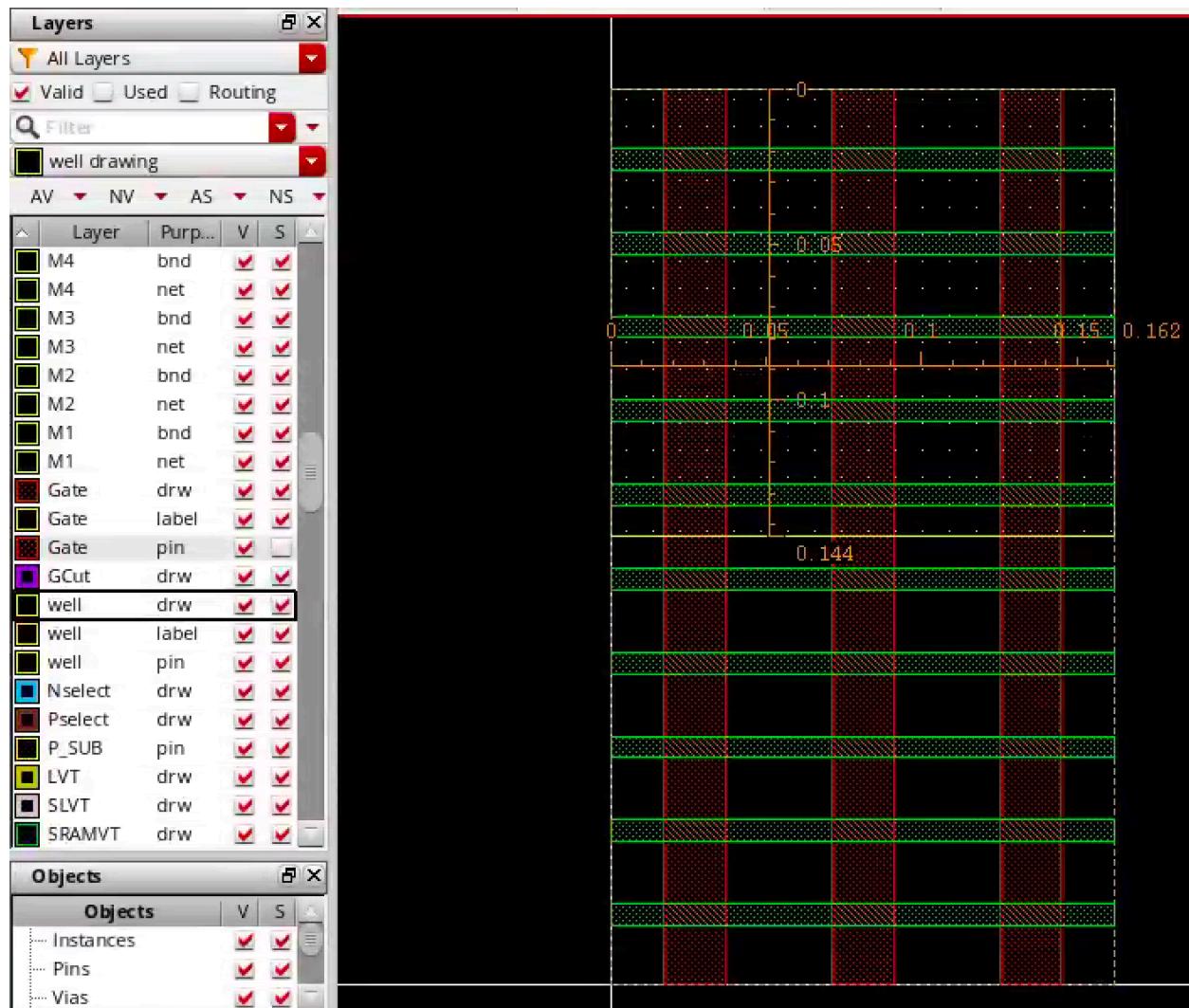
Similarly place 9 fins above this fin, the distance between each fin should be 0.02um and fin pitch = 0.027um



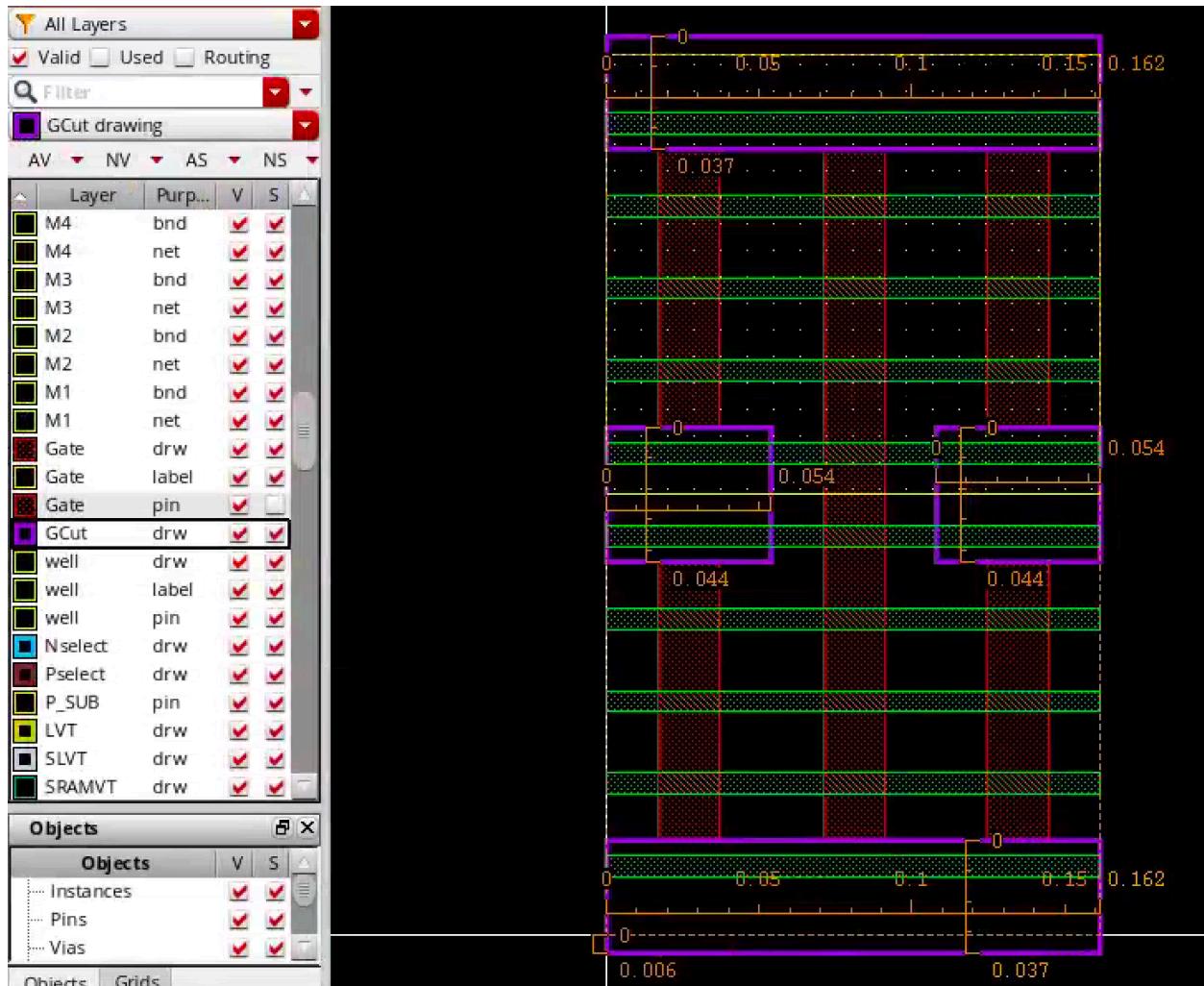
- iii) Draw the **BOUNDARY** drawing layer as shown in picture, it should cover all gates and fins.



iv) Draw well drawing (0.162um x 0.144um)

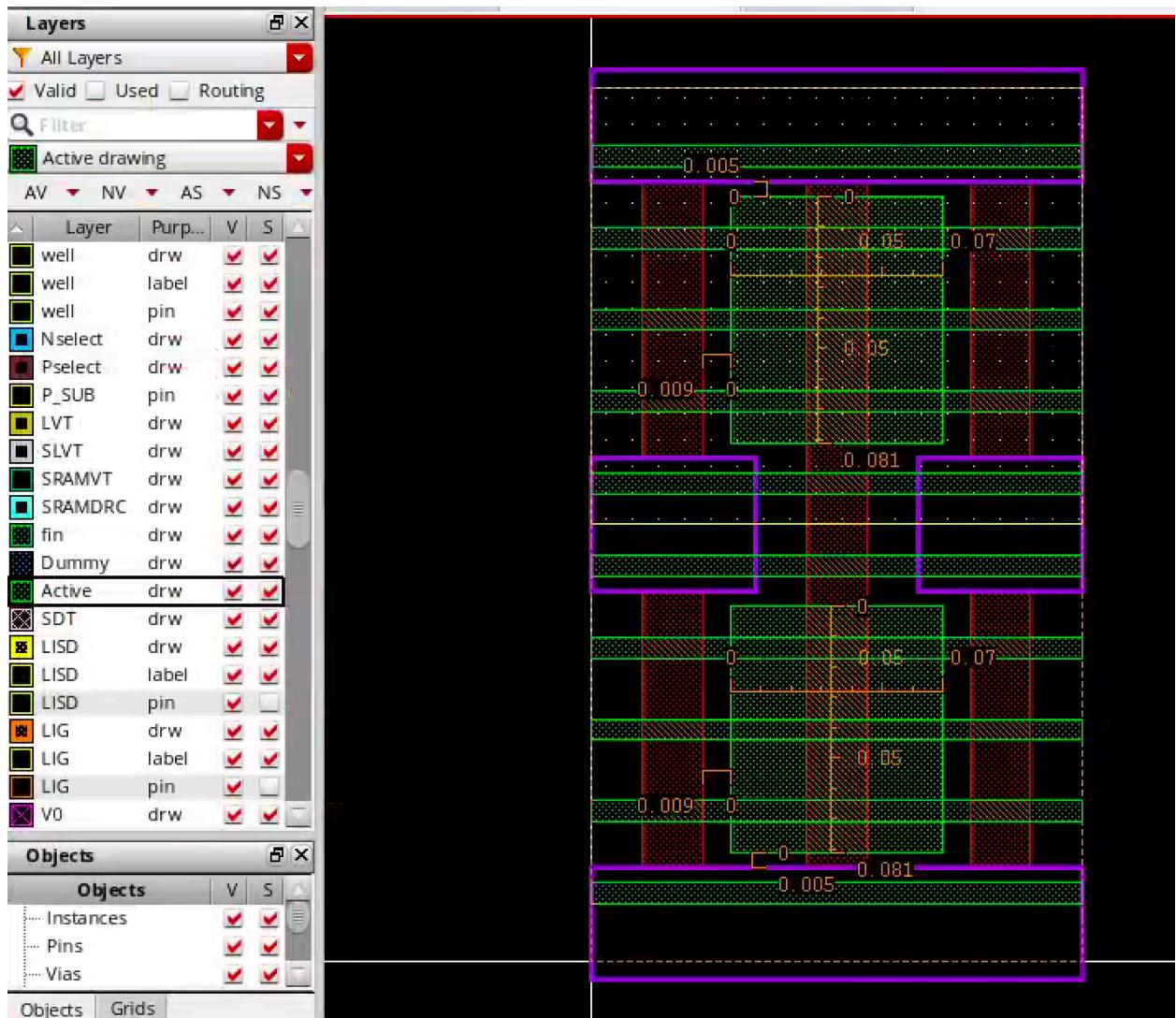


- v) Draw **GCut drawing**. It is drawn at the center of dummy gates ( $0.054\text{um} \times 0.044\text{um}$ ) and also at the top and bottom ( $0.162\text{um} \times 0.037\text{um}$ ). Please refer the below image. At the bottom GCut layer is  $0.006\text{um}$  below the x-axis and at the top its  $0.006$  above the **BOUNDARY** layer.

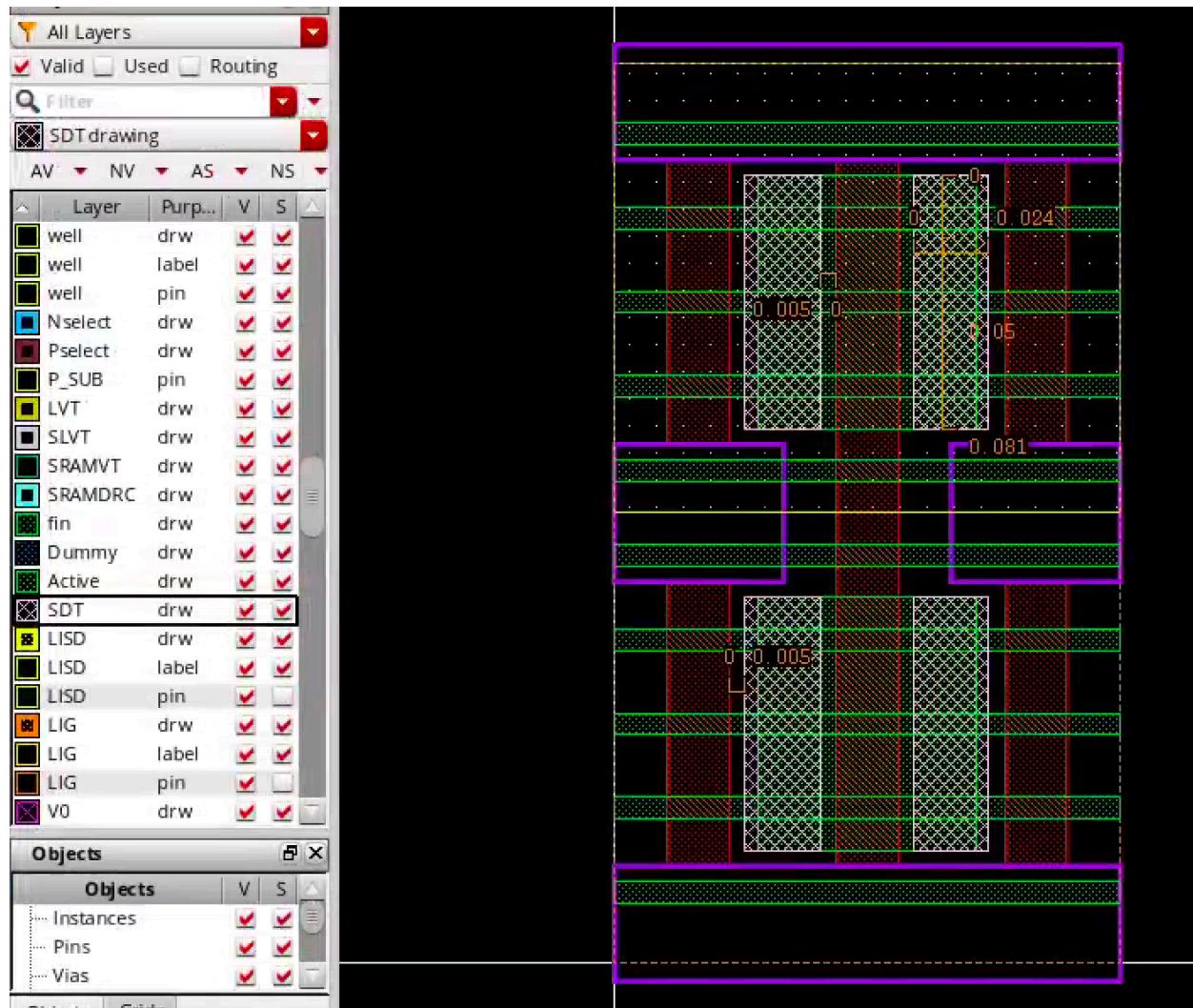


vi) Draw Active drawing for pfet and nfet ( $0.07\text{um} \times 0.081\text{um}$ )

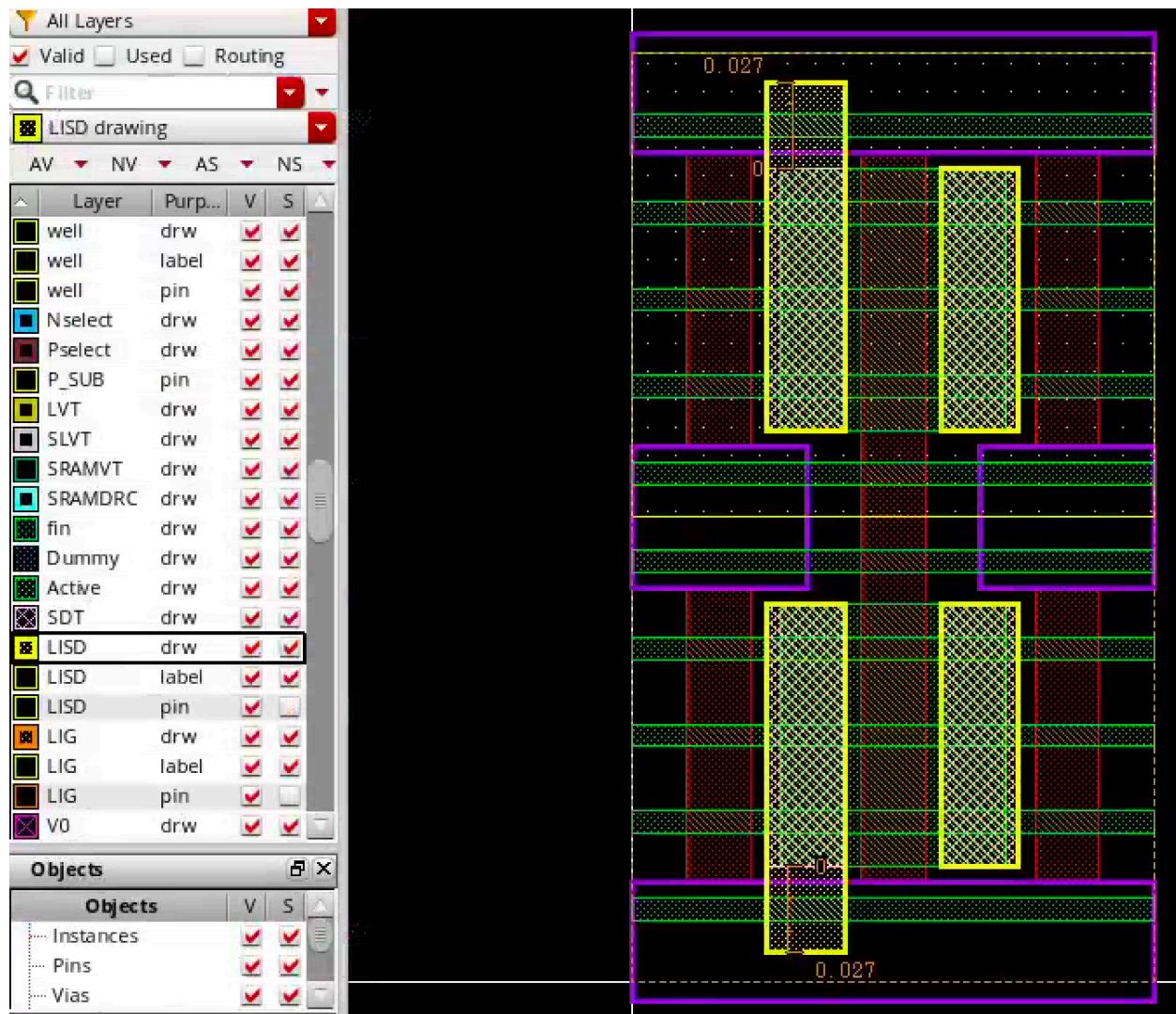
$W_p = W_n = 0.081\text{um}$ . On left and right, distance between the dummy gate and Active layer is  $0.009\text{um}$ . On top and bottom, distance between the GCut layer and Active layer is  $0.005\text{um}$ .



- vii) Draw **SDT drawing** on Active ( $0.024 \text{ um} \times 0.081 \text{ um}$ ). The distance between Gate and SDT is  $0.005\text{um}$ . SDT is drawn on Active layer wherever connections are to be made. If a source or drain has no connections, then SDT layer should not be drawn.

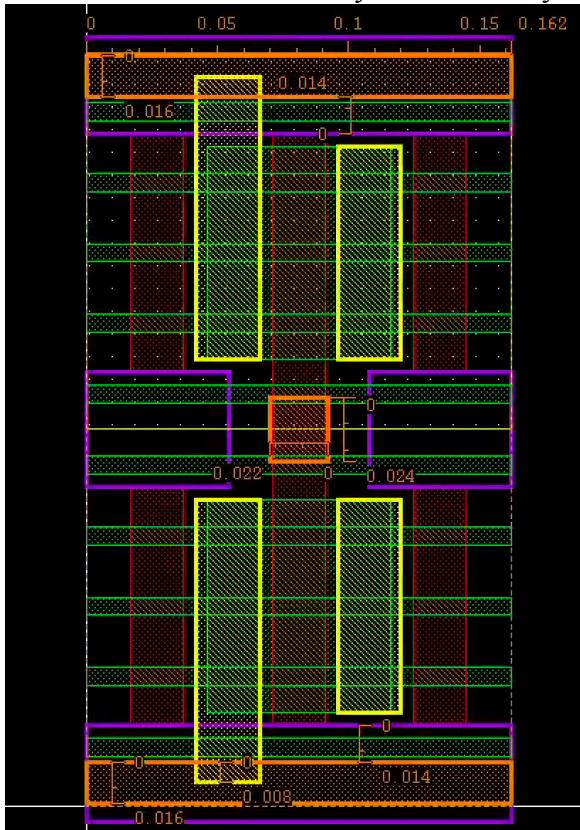


- viii) Draw **LISD drawing** on top on SDT drawing, wherever VDD and GND connections are to be made, extend the LISD layer above the Active layer by 0.027um as shown in the below picture.



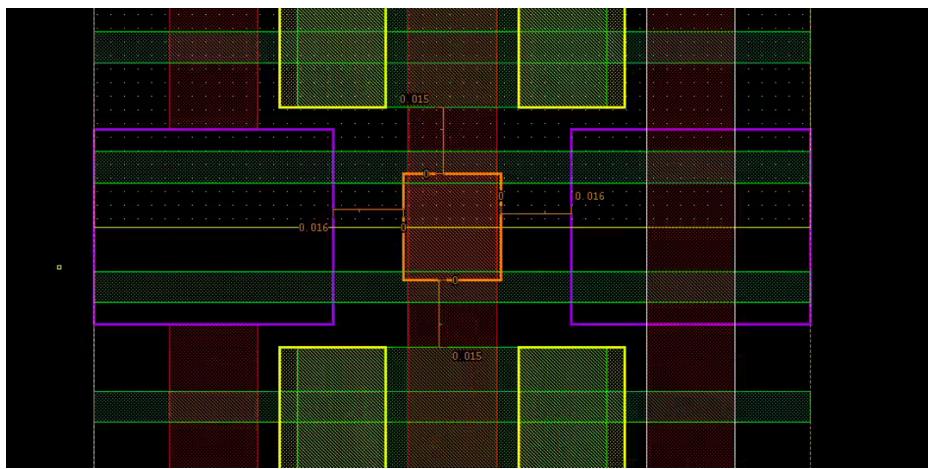
- ix) Draw **LIG** drawing. **Change** On top and bottom for connecting the LISD layer to VDD and GND ( $0.162\text{um} \times 0.016\text{um}$ ). One for gate connection ( $0.022\text{um} \times 0.024\text{um}$ ).

Note: The distance GCut layer and LIG layer is  $0.014\text{um}$

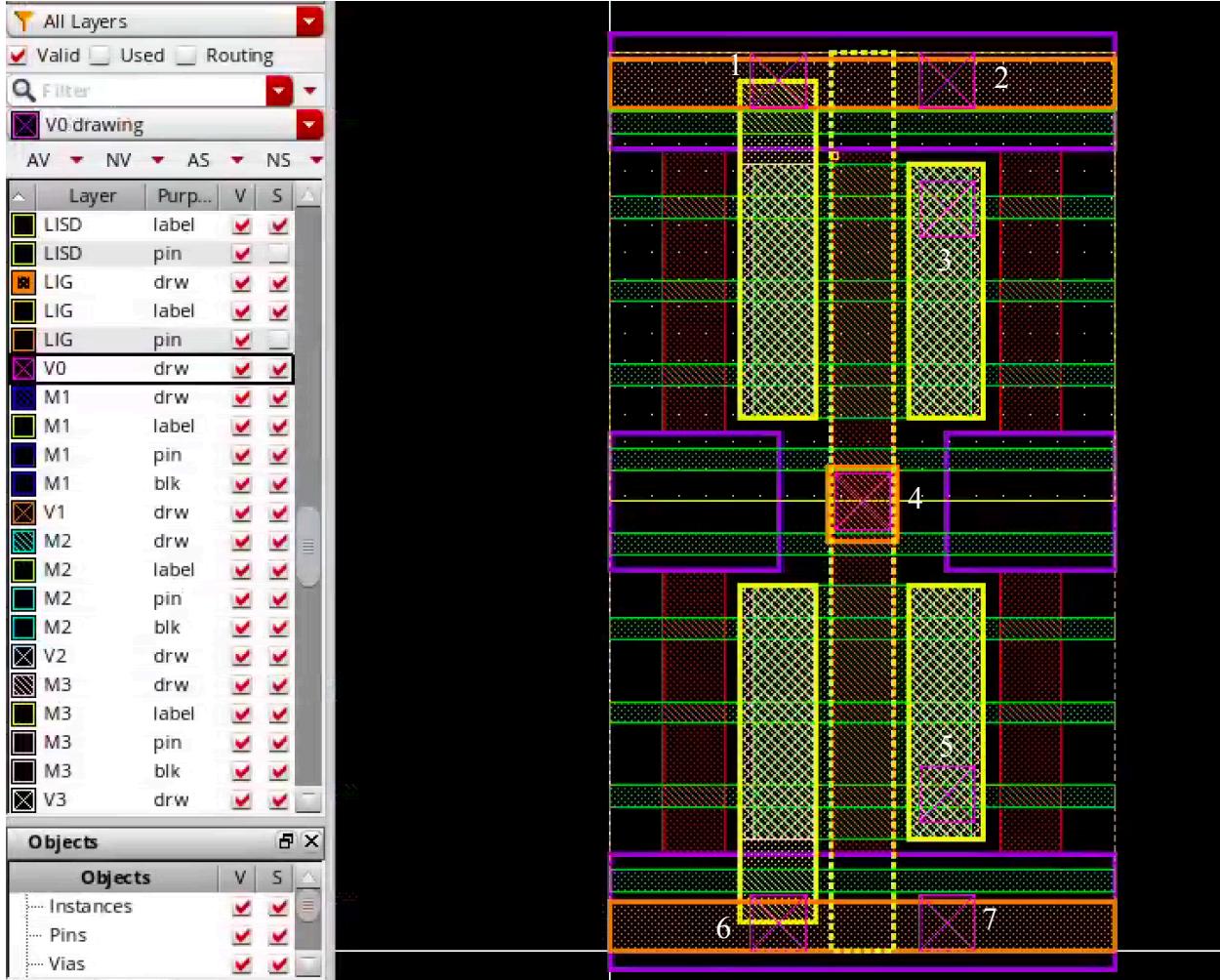


LIG for gate connection: ( $0.022\text{um} \times 0.024\text{um}$ )

Refer the below shown picture. Distance from GCut (left and right):  $0.016\text{um}$ , Distance from Active (top and bottom):  $0.015\text{um}$

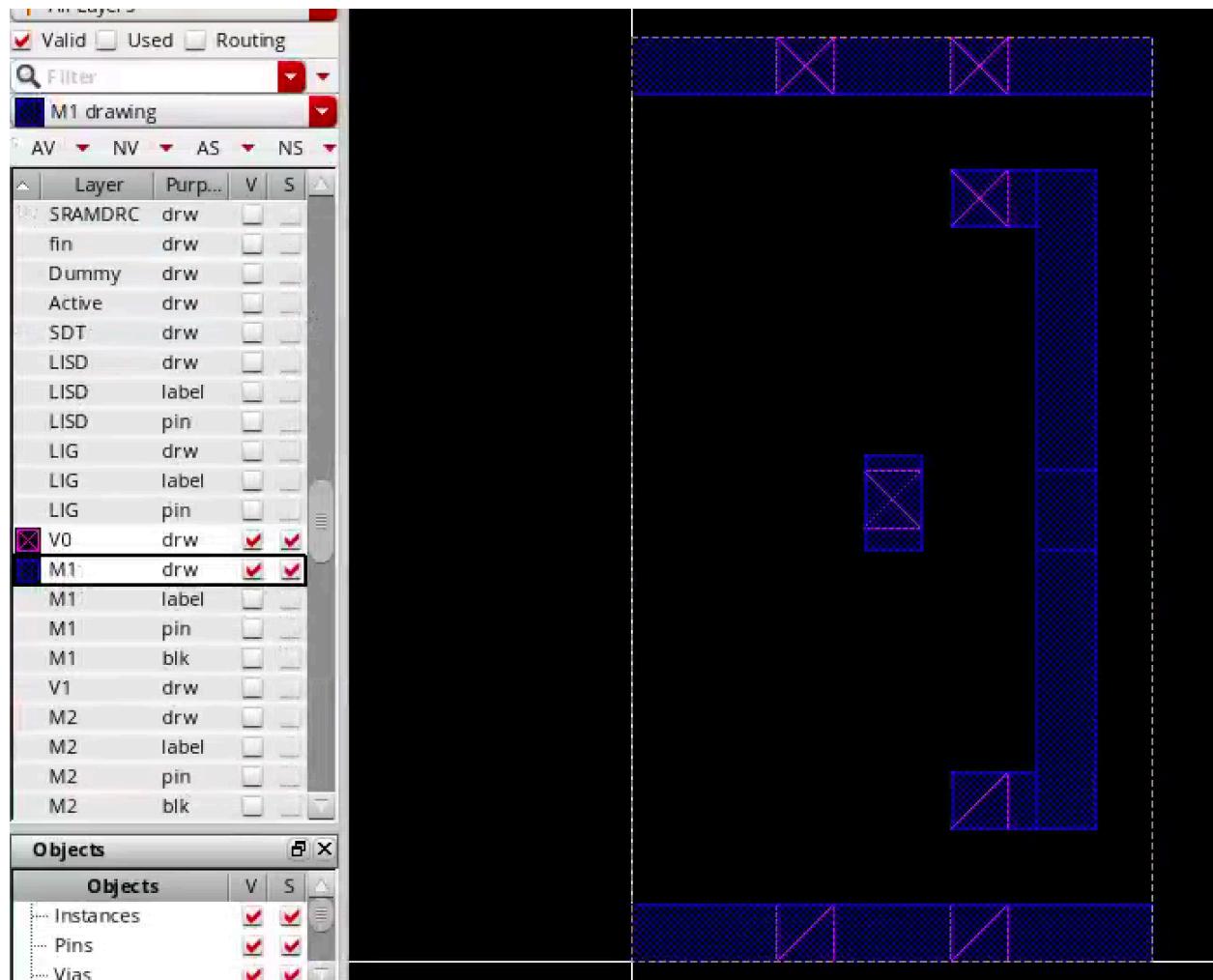


- x) Draw **V0 drawing** (via0: similar to contact in 65nm) for the all gates, nets and VDD, GND (place V0 on LIG layer).
- V0: 0.018um x 0.018um.  
7 V0s drawn are marked in the layout

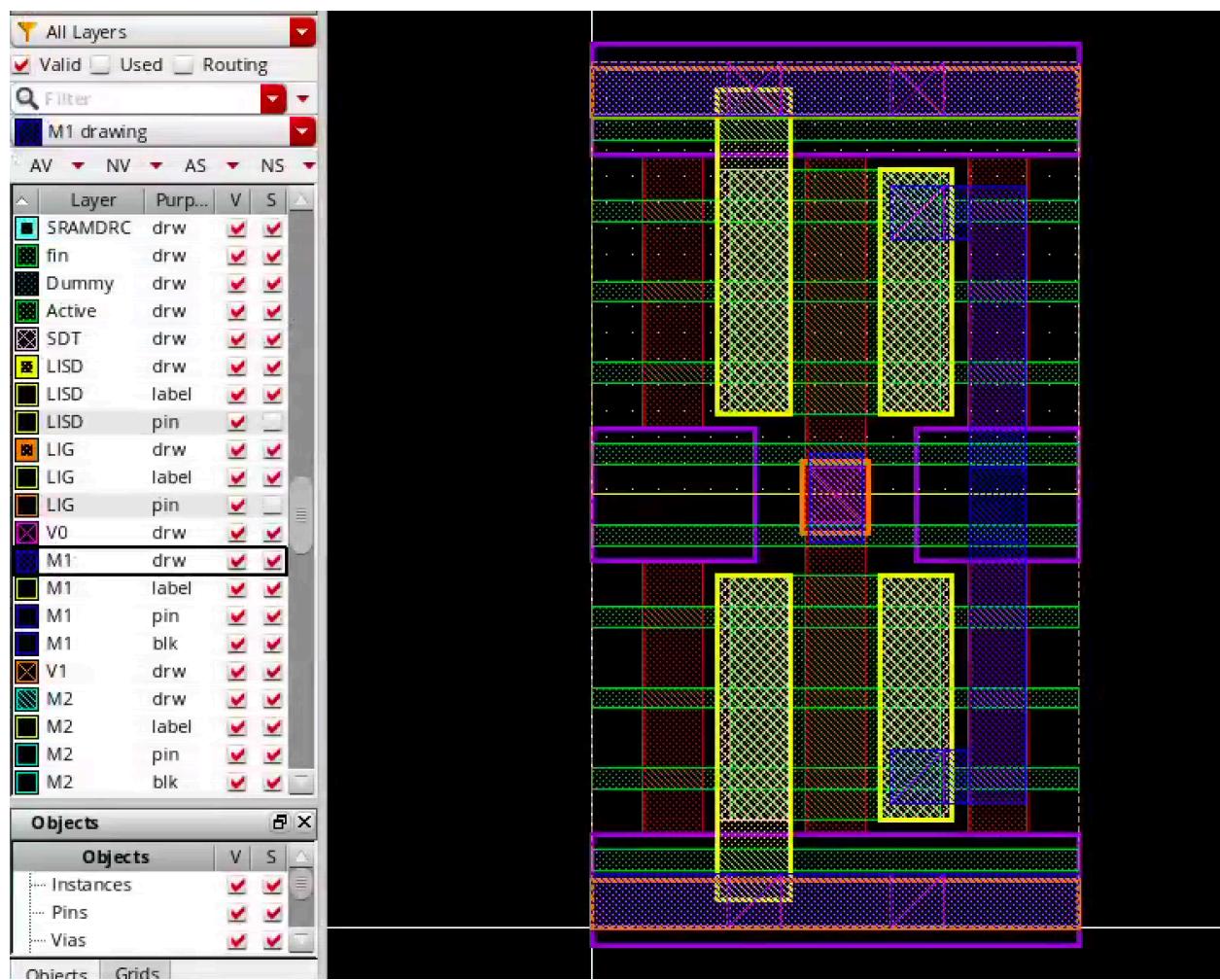


xi) Draw M1 to connect the nets and for VDD and GND

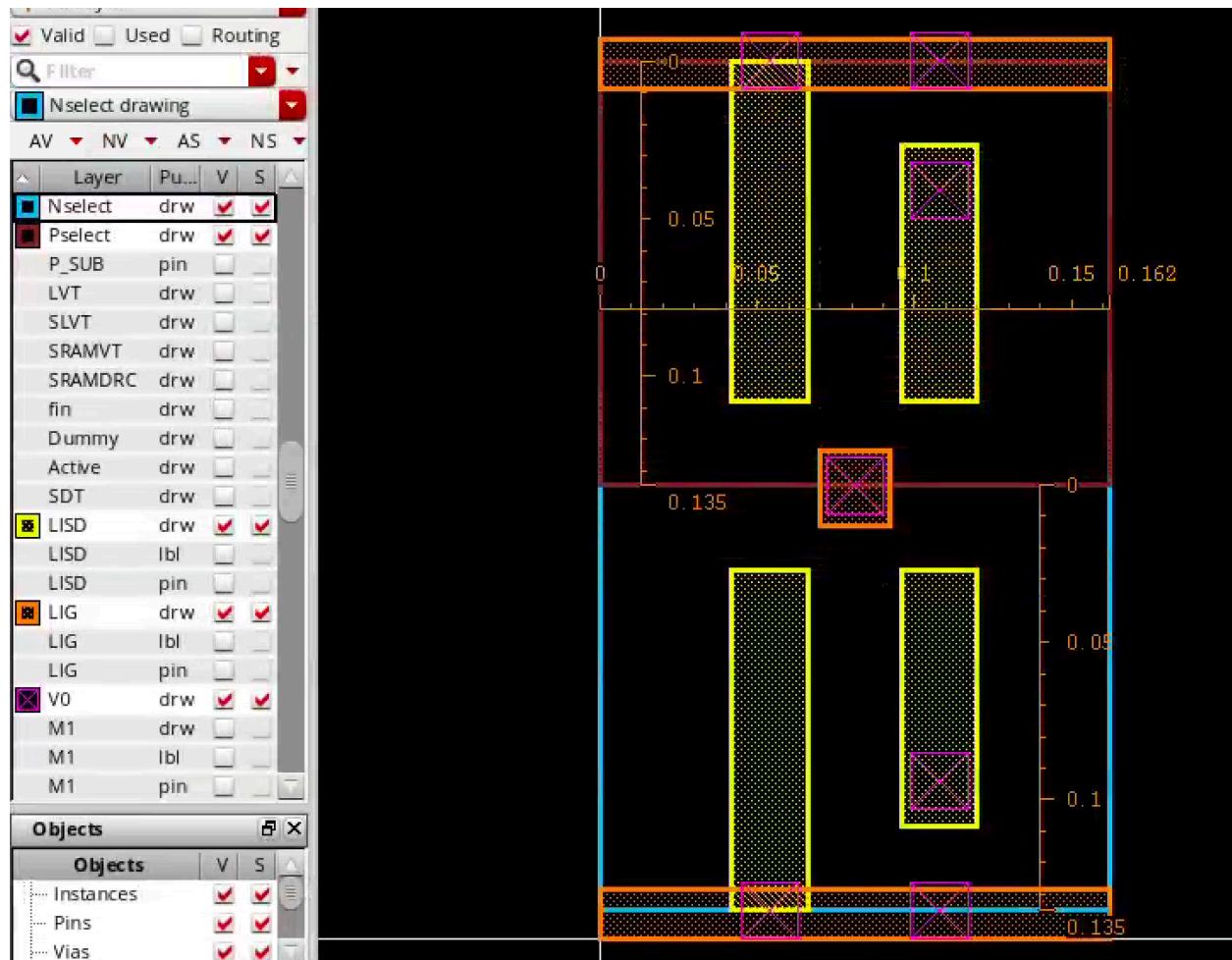
In the below figure, all other layers are disabled so that only M1 and V0 are visible



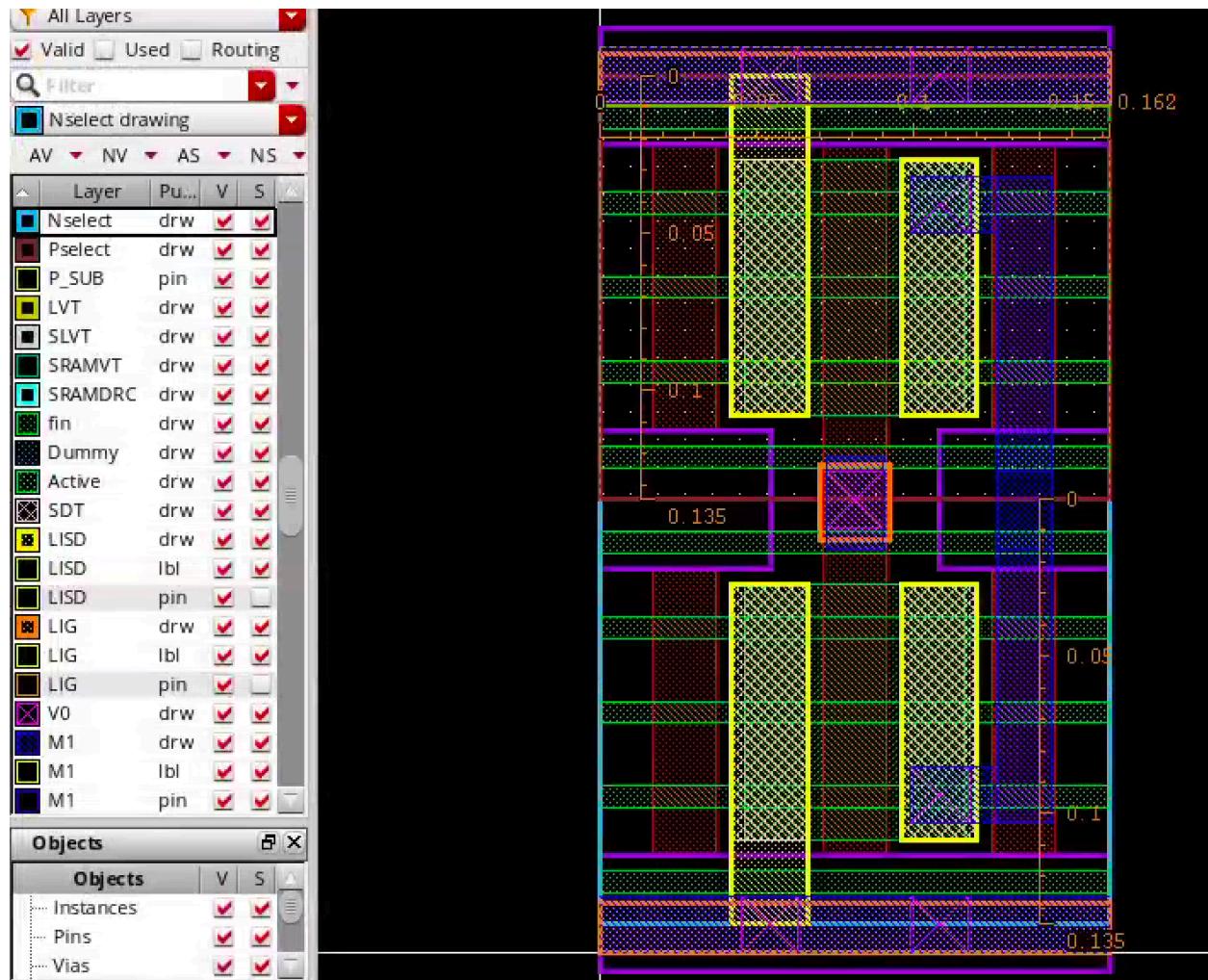
In the picture below all drawn layers are visible



- xii) Draw Pselect on top on pfet and Nselect on top of nfet (0.162um x 0.135um).  
Only V0, LISD, LIG, Pselect, Nselect



The picture below has all drawn layers are visible

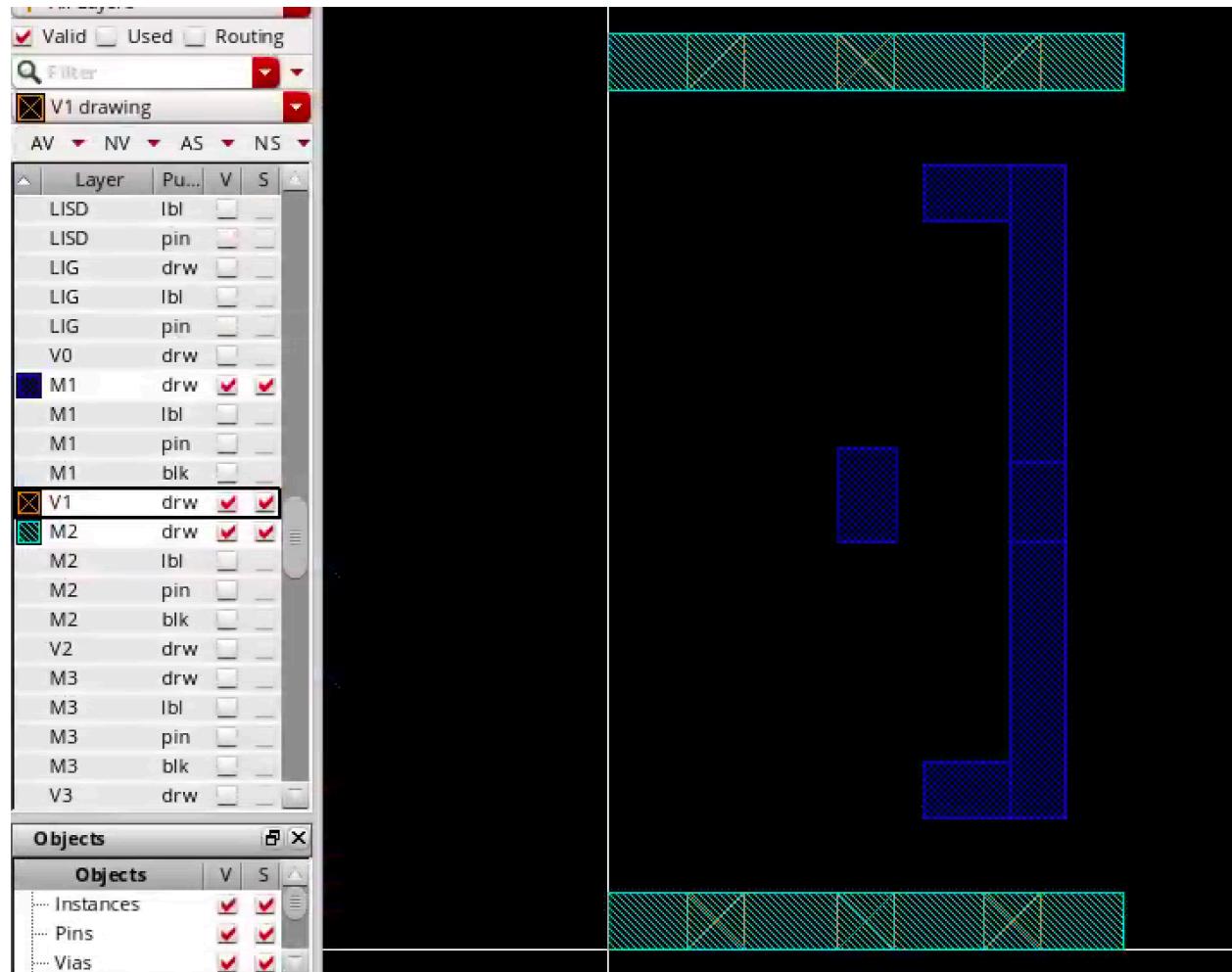


xiii) VDD and GND are brought to M2.

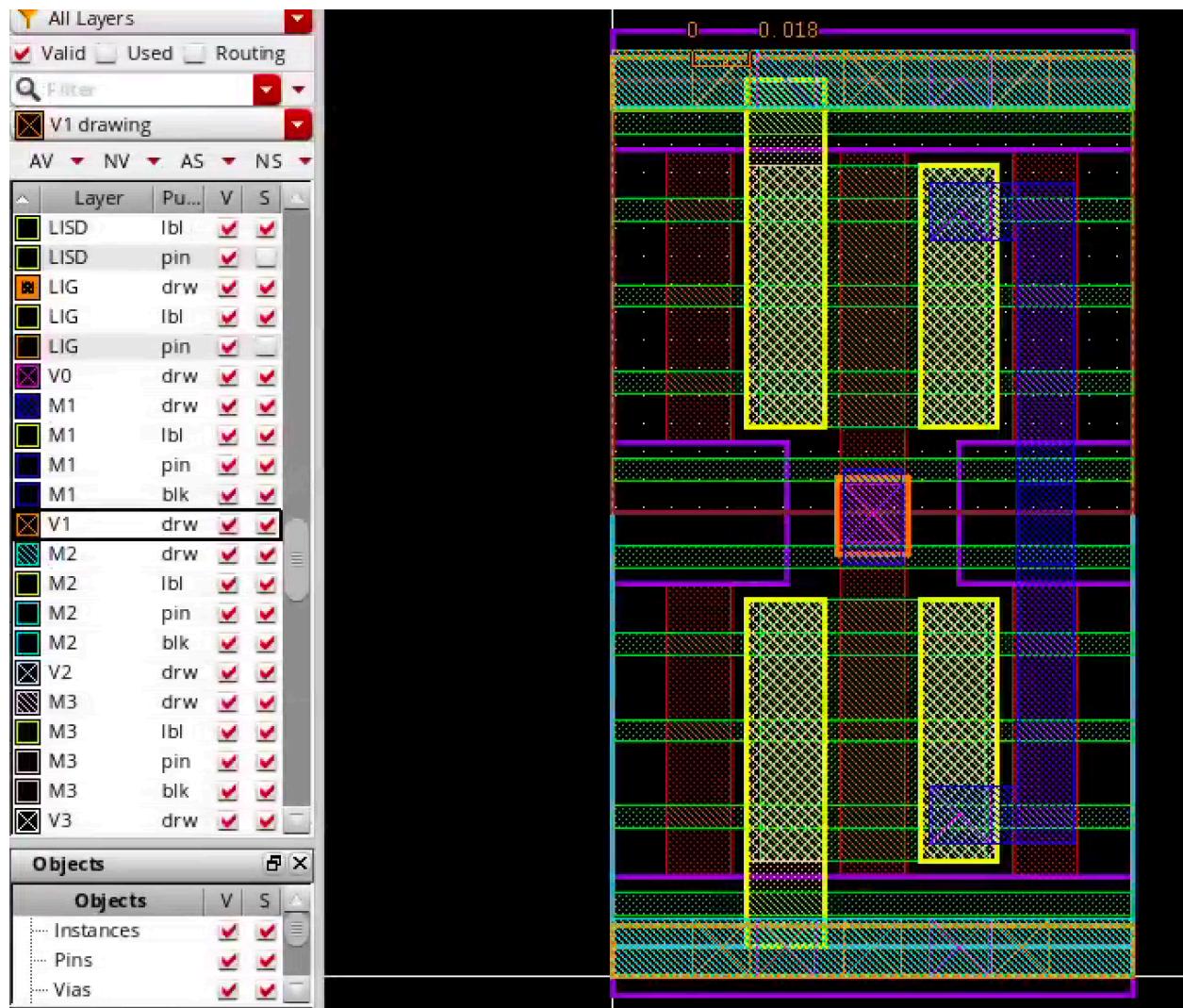
Input and output pins are brought up to M3.

For VDD and GND, draw M2 on top of M1, place V1 (0.018um x 0.018um) to connect M1 to M2

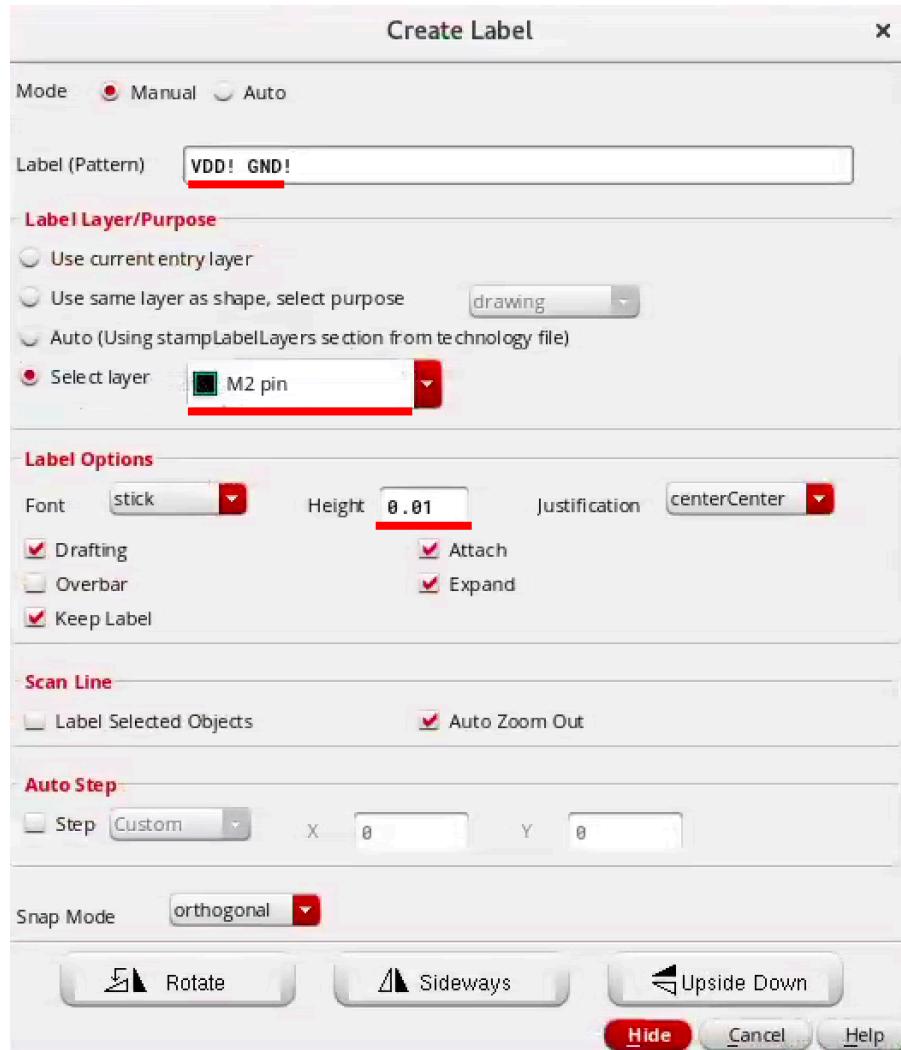
In the below picture only M1, M2, V1 are made visible



All drawn layers are visible below



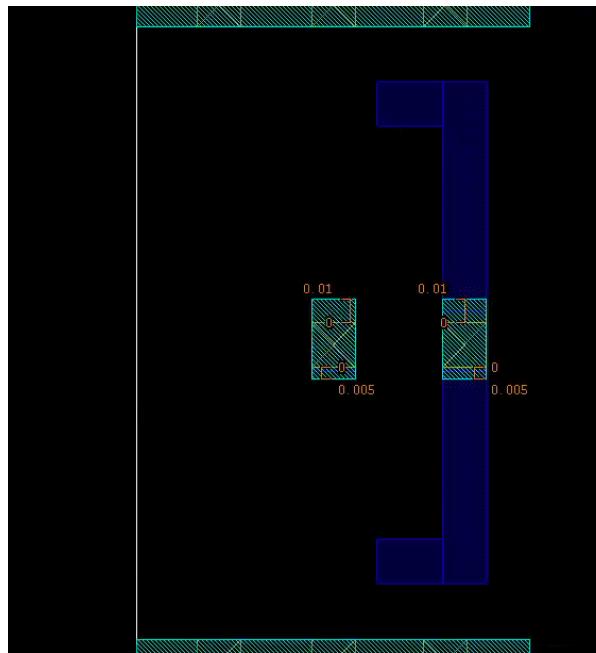
Now create labels for VDD and GND as **VDD!** and **GND!** using **M2 pin** layer  
On the top tool bar, Create -> Label



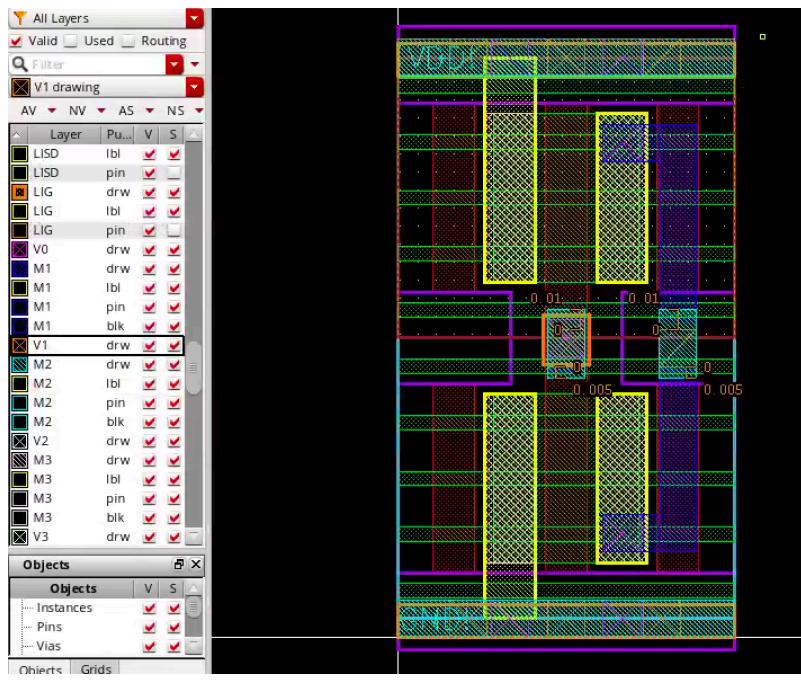
Place the labels on **M2 drawing** layer

Input and output pins should be brought up to M3,  
Place M2 and V1 (0.018um x 0.018um) on top of M1.

Only M1, M2, V1 are enabled in the below picture

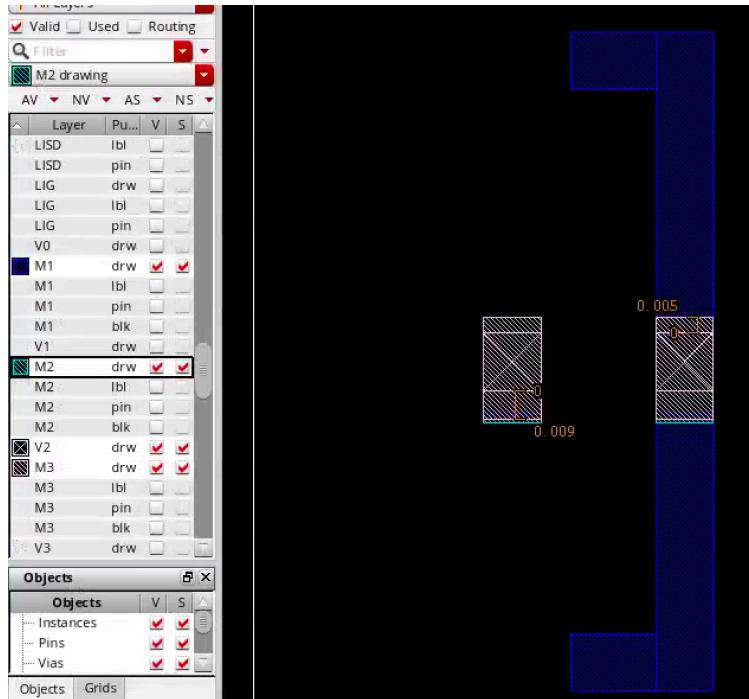


Below is the picture with all drawn layers

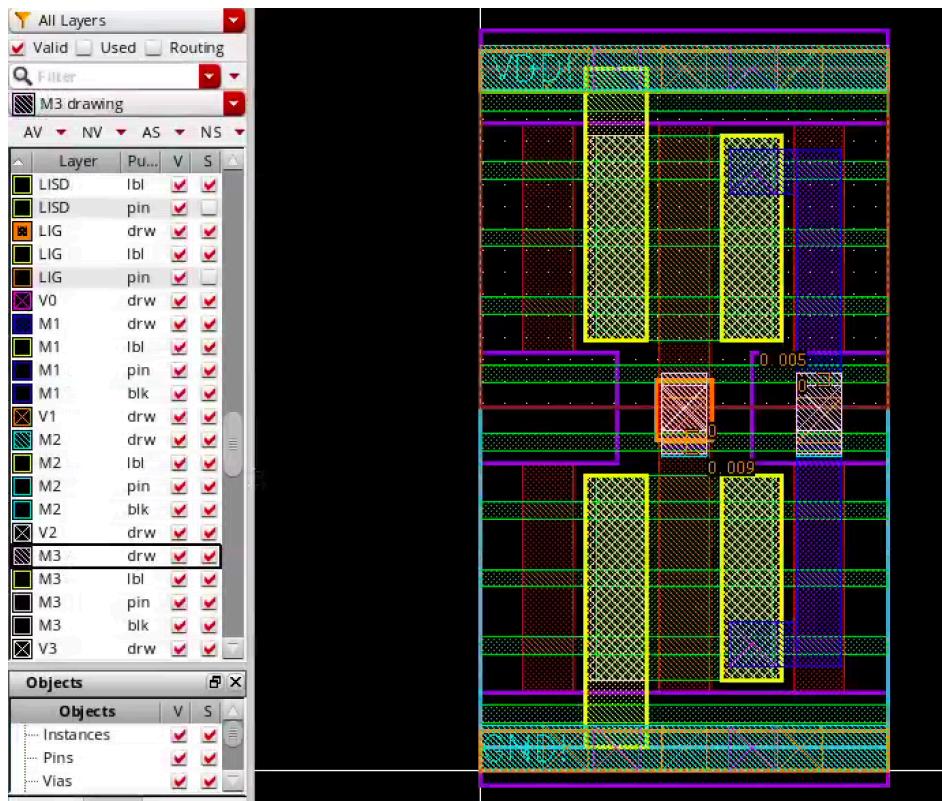


Now place M3 and V2 ( $0.018\mu m \times 0.018\mu m$ ) on top of M2.

Only M1, M2, M3, V2 are enabled in the picture below

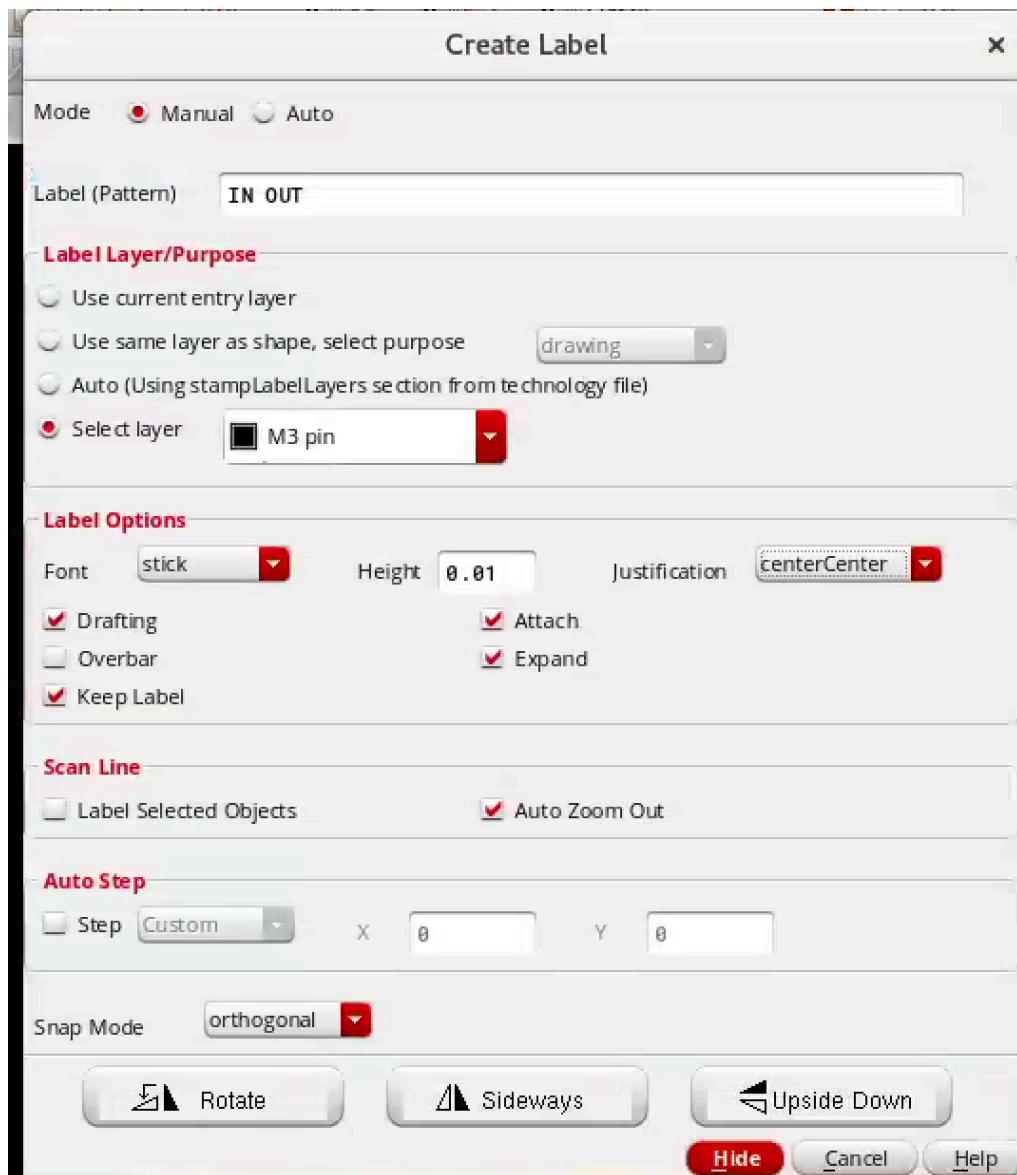


All drawn layers are visible in the next picture

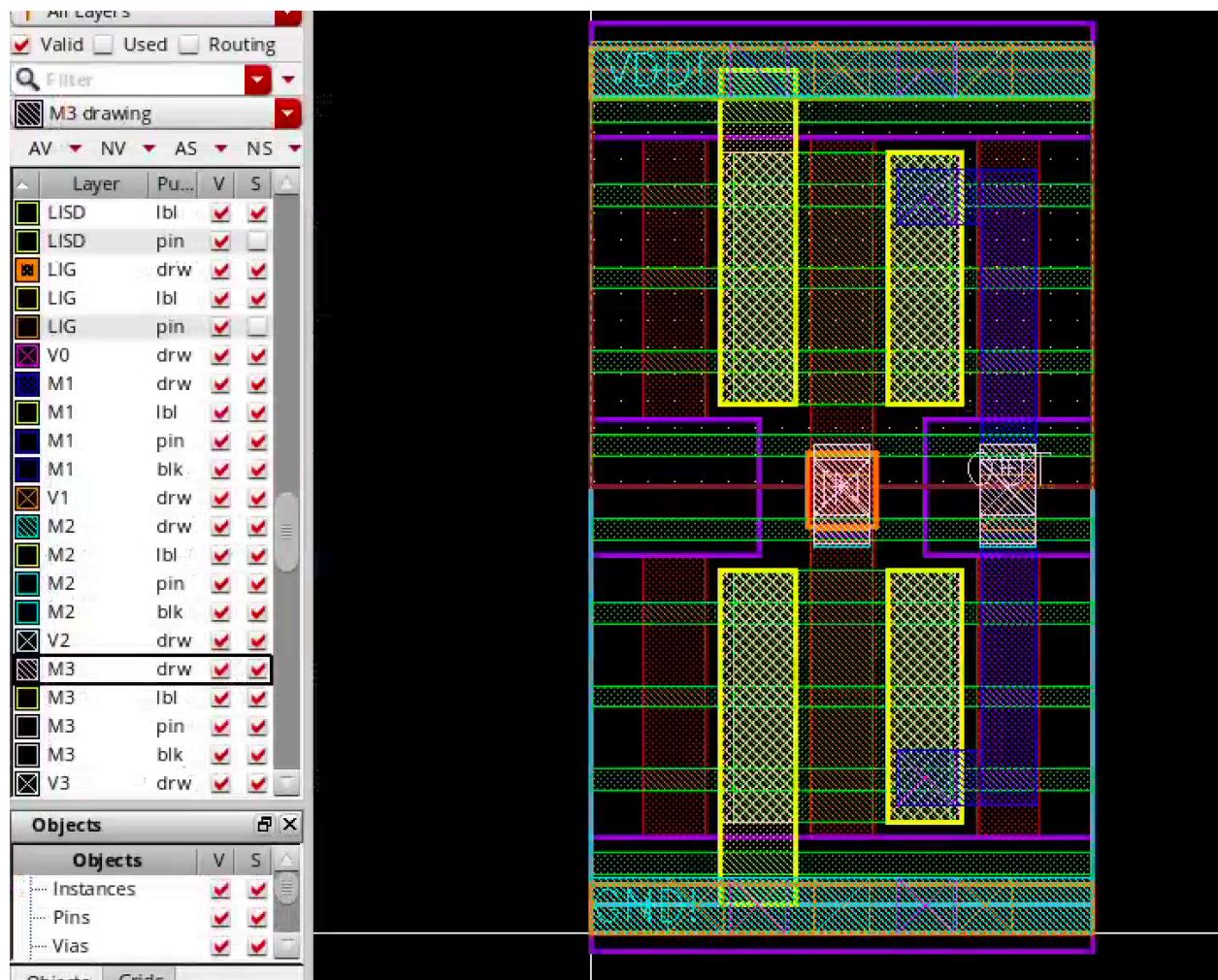


Now create label for Input and Output pins

Create -> Label



Place them on M3 pins.

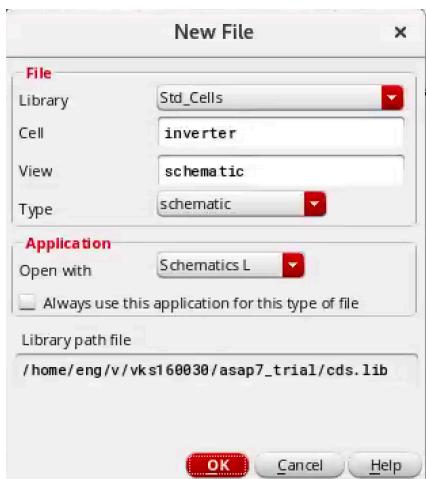


Inverter layout is now completed.

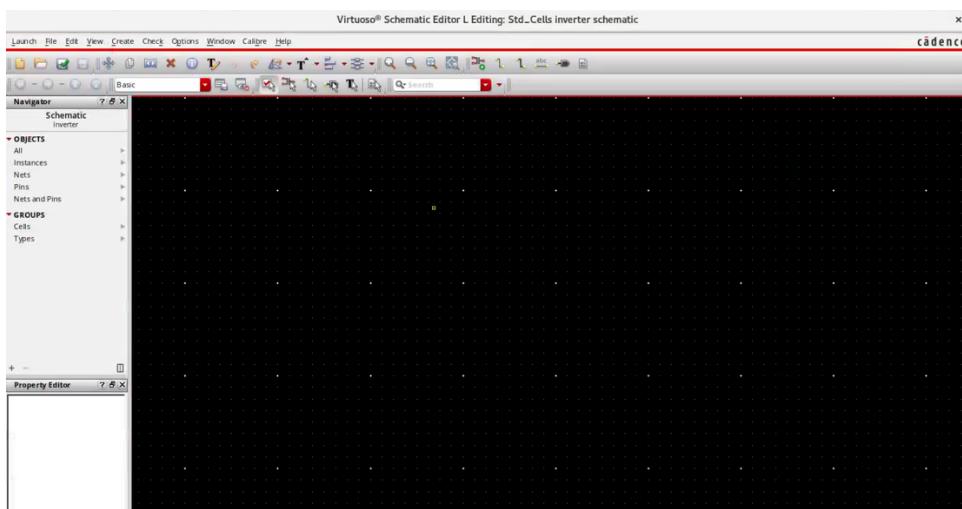
## Schematic

Go to Virtuoso main window

File -> New -> Cellview

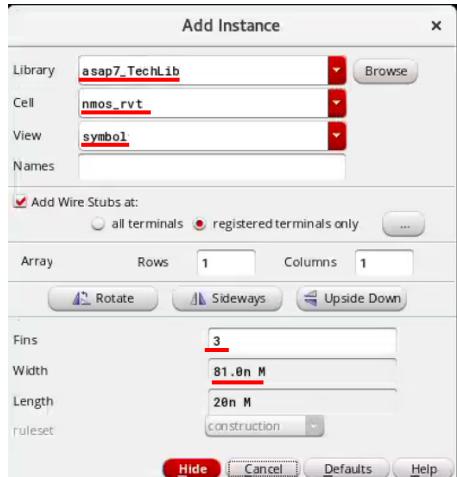


Click **OK**



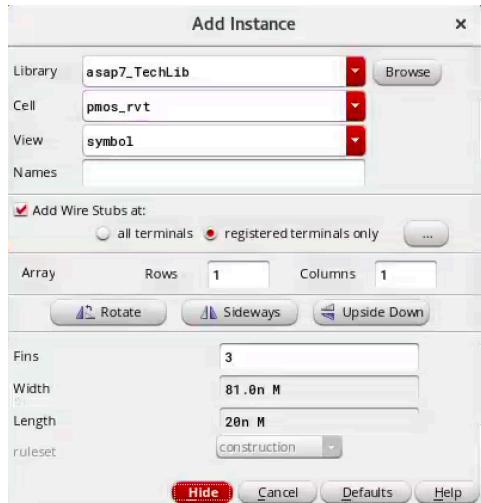
- i) In the tool bar on topTo create nfet: Create -> Instance

**Library:** **asap7\_TechLib**  
**Cell:** **nmos\_rvt**  
**View:** **symbol**  
**Fins:** 3 (Width sets to 81nm)

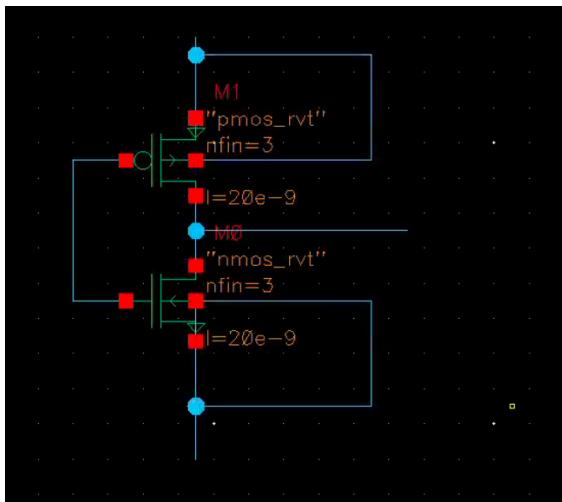


- ii) Similarly, to create pfet: Create -> Instance

**Library:** **asap7\_TechLib**  
**Cell:** **pmos\_rvt**  
**View:** **symbol**  
**Fins:** 3 (Width sets to 81nm)



iii) Press W and draw wires.

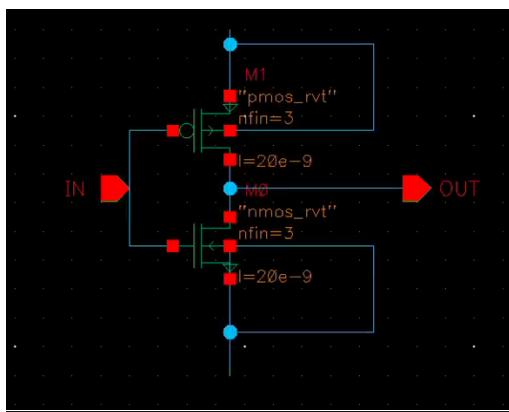
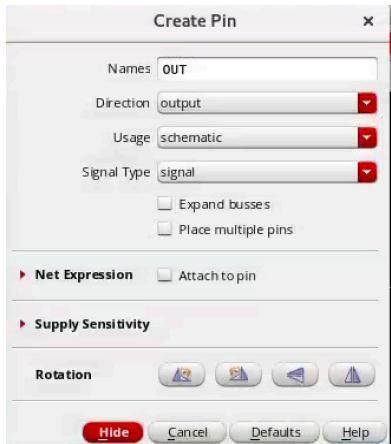


iv) Create Input and Output Pins

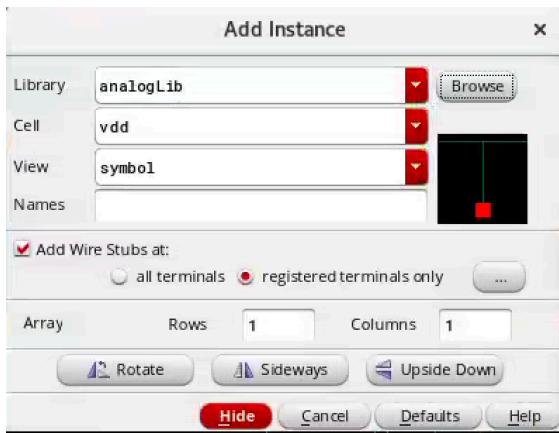
Create -> Pin



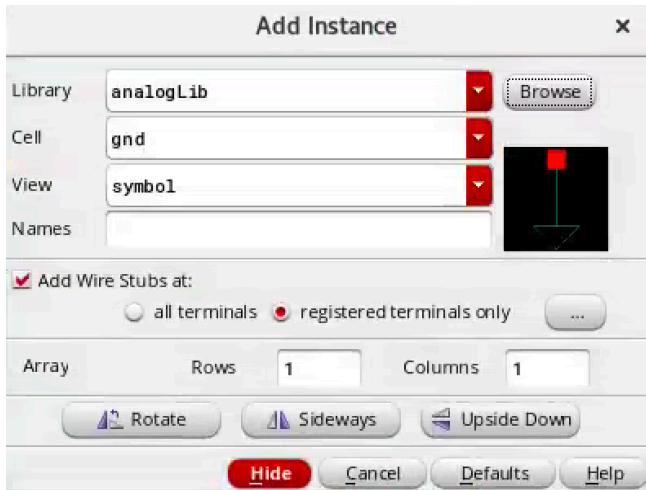
Create -> Pin



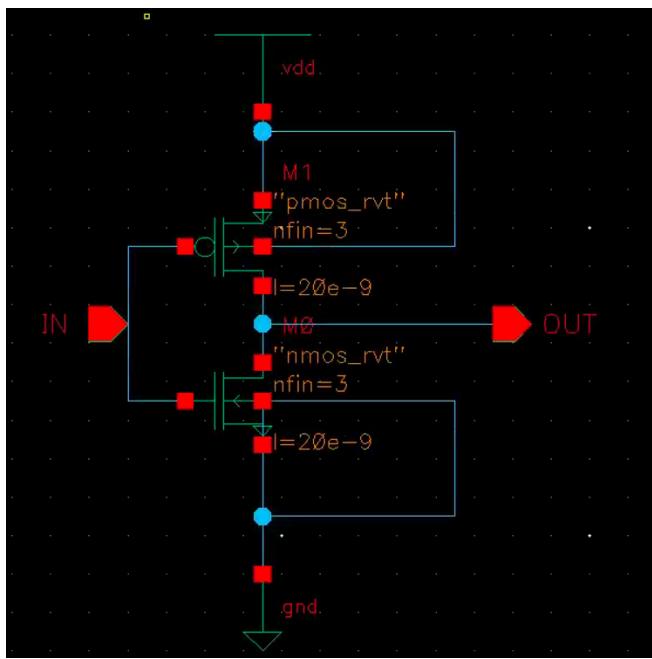
v) Add VDD and GND  
Create -> Instance



Create -> Instance



Final Schematic should like this:



### Check and Save the design

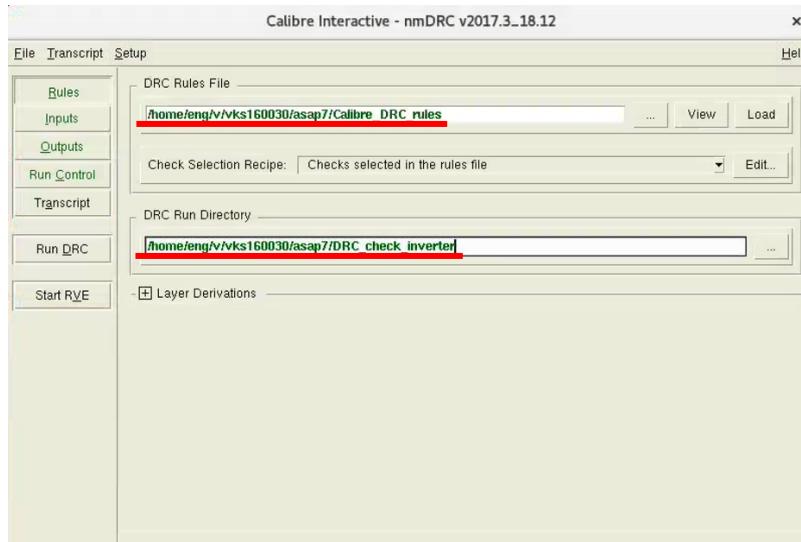
Inverter schematic is now completed.

## Design Rule Check

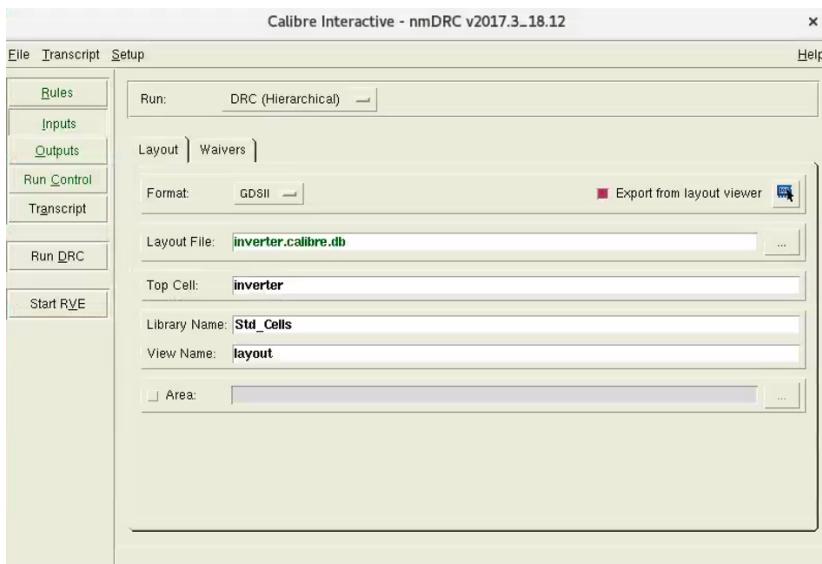
In the layout view, on the tool bar at the top  
Calibre -> Run nmDRC

**Rules:** In DRC Rules File, browse and select the **Calibre\_DRC\_Rules** file which is in **your work directory (asap7)**

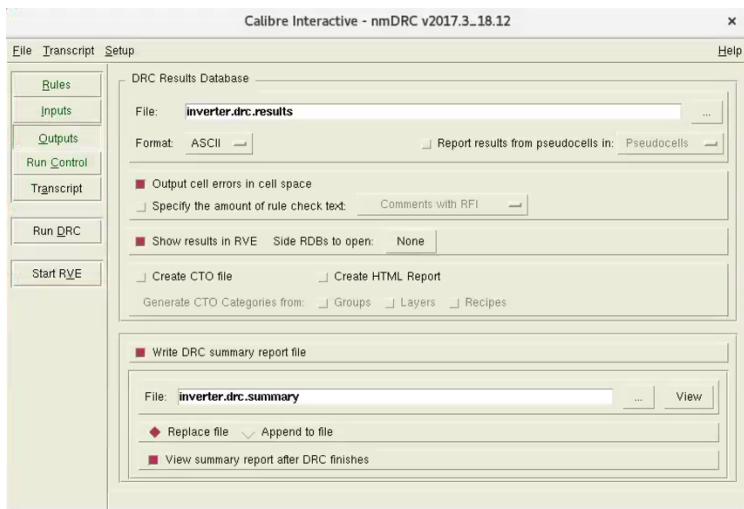
In DRC Run Directory, if you are unable to edit in the interactive window, go to files and create a new directory and browse that directory in the interactive window.



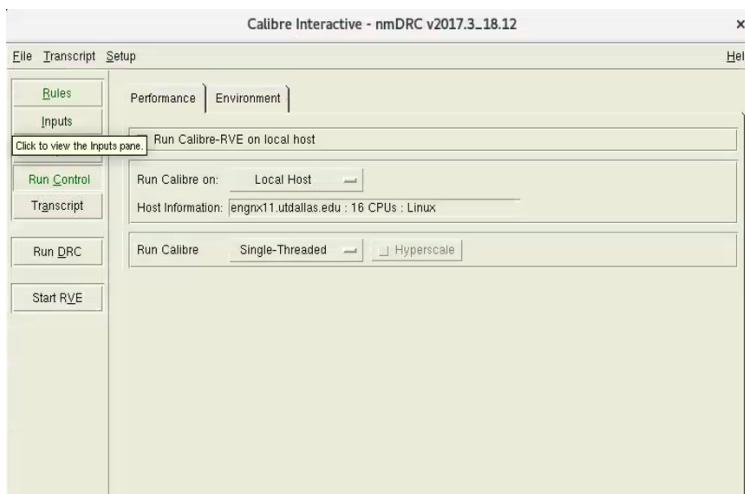
**Inputs:**



## Outputs:



## Run Control:



Click on the **Run DRC** tab

You will get 1 error as shown in picture below:

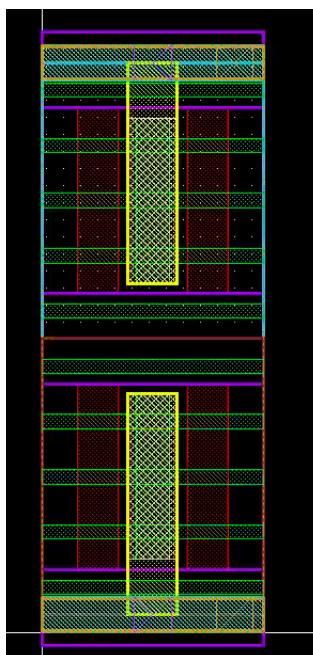


If you get any other errors, you have to fix them before proceeding.

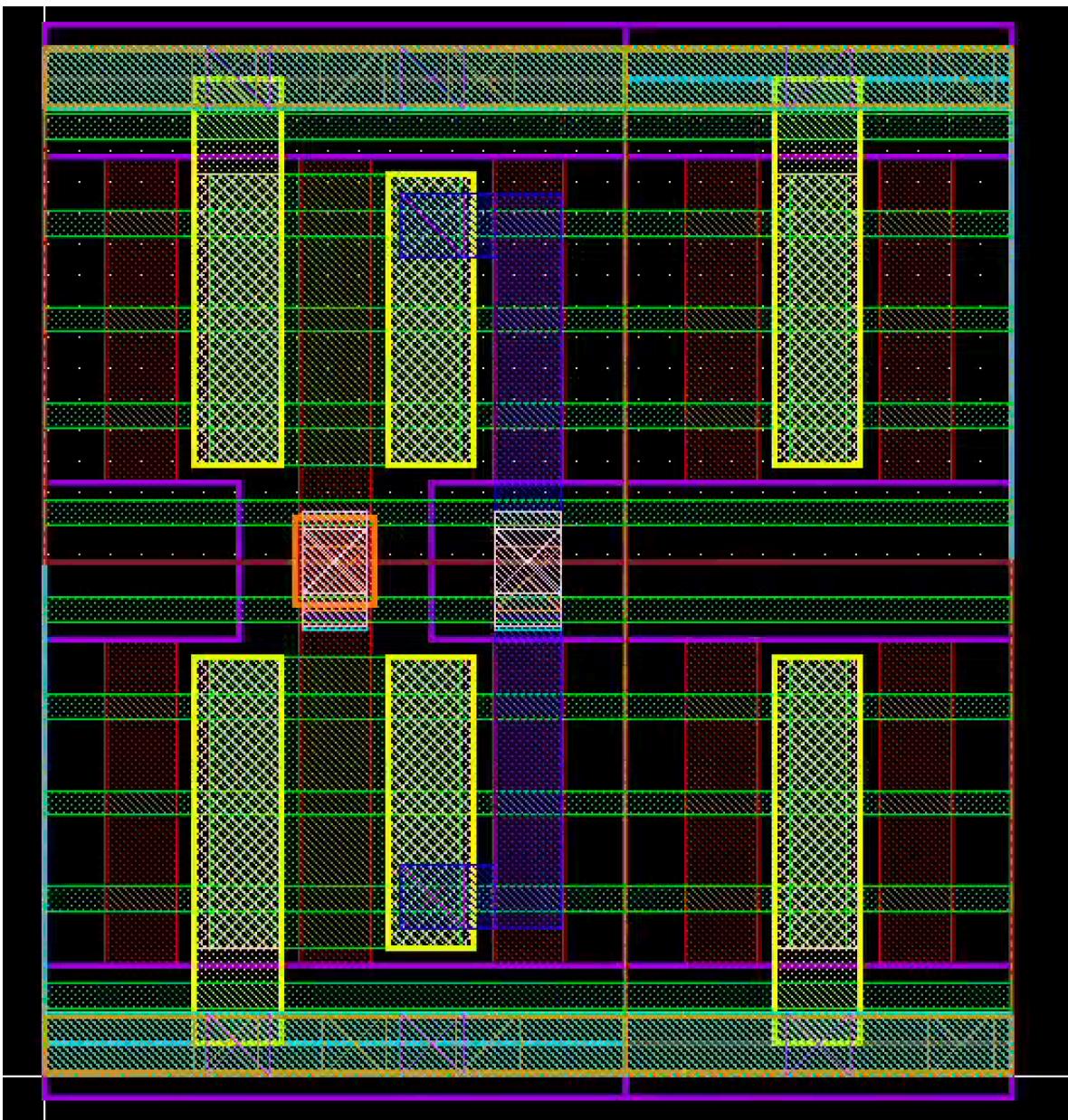
If you have only 1 error, proceed ahead

In order to get a DRC clean inverter, you need to add a Tap Cell

Go to **Library Manager** -> In **Library** column, select **asap7\_TechLib** -> **Tap\_Cell** -> Open layout



Copy the entire Tap\_Cell and paste it beside the inverter as shown below

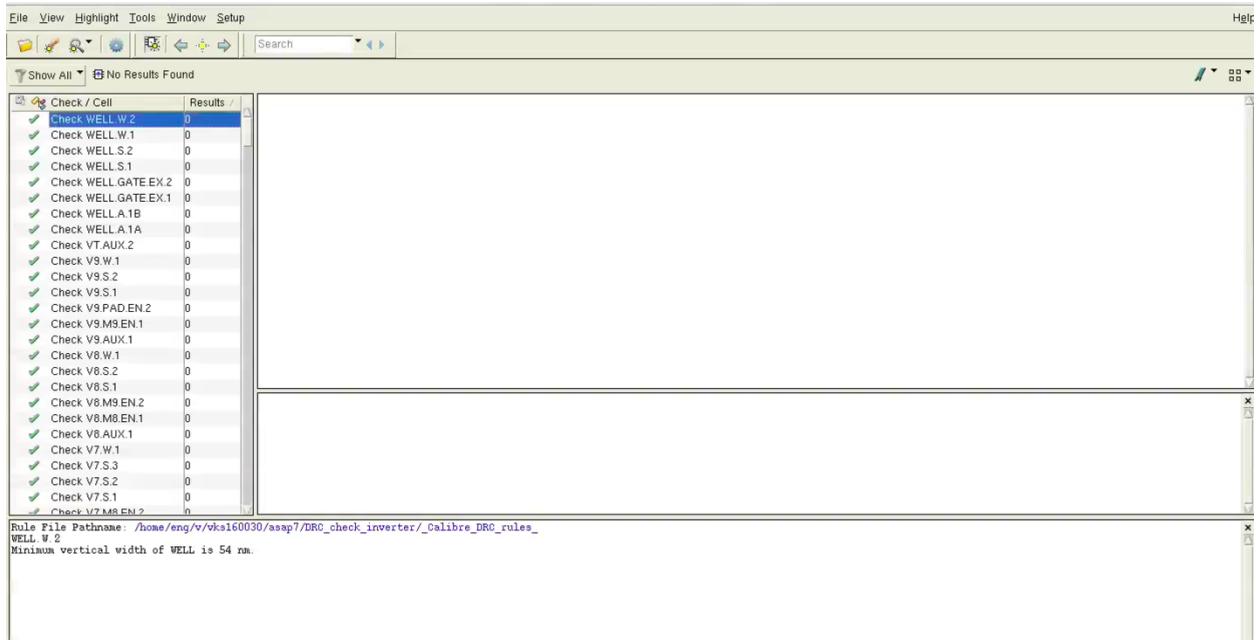


Make sure all the layers of Tap\_Cell align with your inverter layout

**Note:** When you draw layouts manually and place them one beside another, you just need to have **1 Tap\_Cell in entire row**. Tap cells help pfets and nfets to tie to VDD and GND levels so that they don't drift too much.

This means that in the final stages of your project 1 when you perform DRC of all standard cell, only 1 Tap cell needs to be placed at the right corner.

Run DRC again, you should have no errors

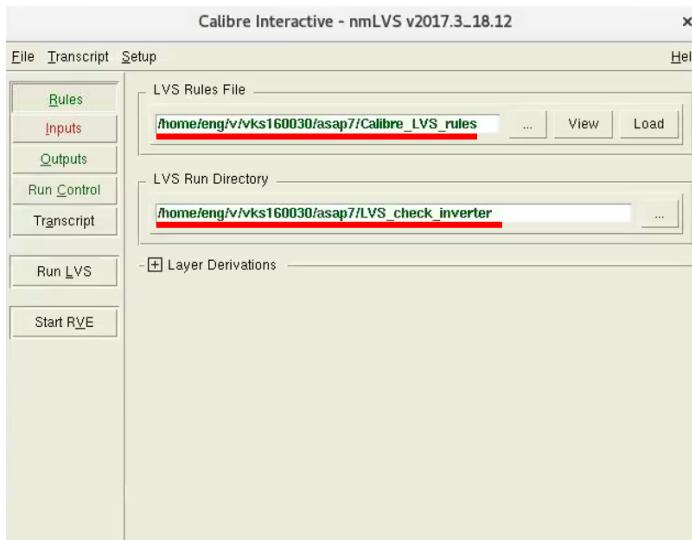


## Layout vs Schematic

In the layout view, Calibre -> Run nmLVS

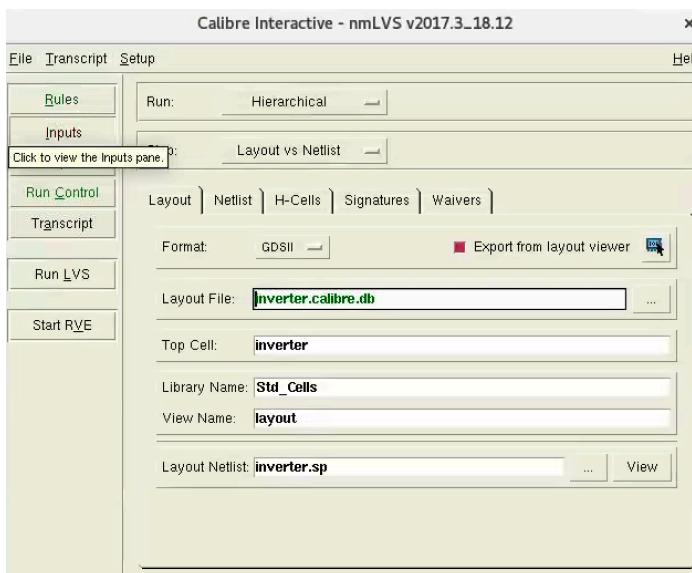
**Rules:** In LVS Rules File, browse and select the **Calibre\_LVS\_Rules** file which is in **your** work directory (asap7)

In LVS Run Directory, if you are unable to edit in the interactive window, go to files and create a new directory and browse that directory in the interactive window.

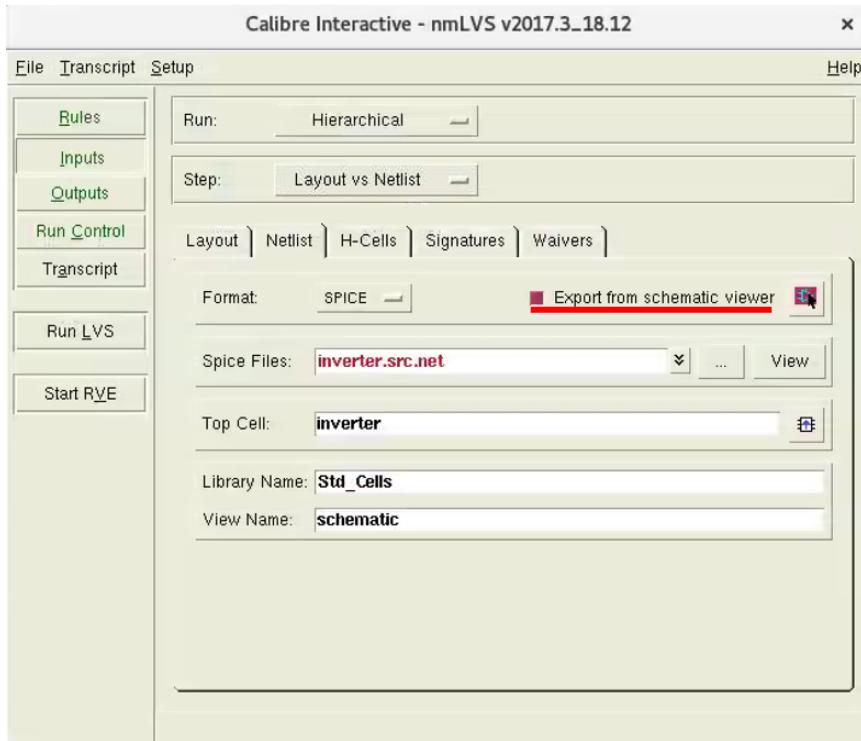


## **Inputs:**

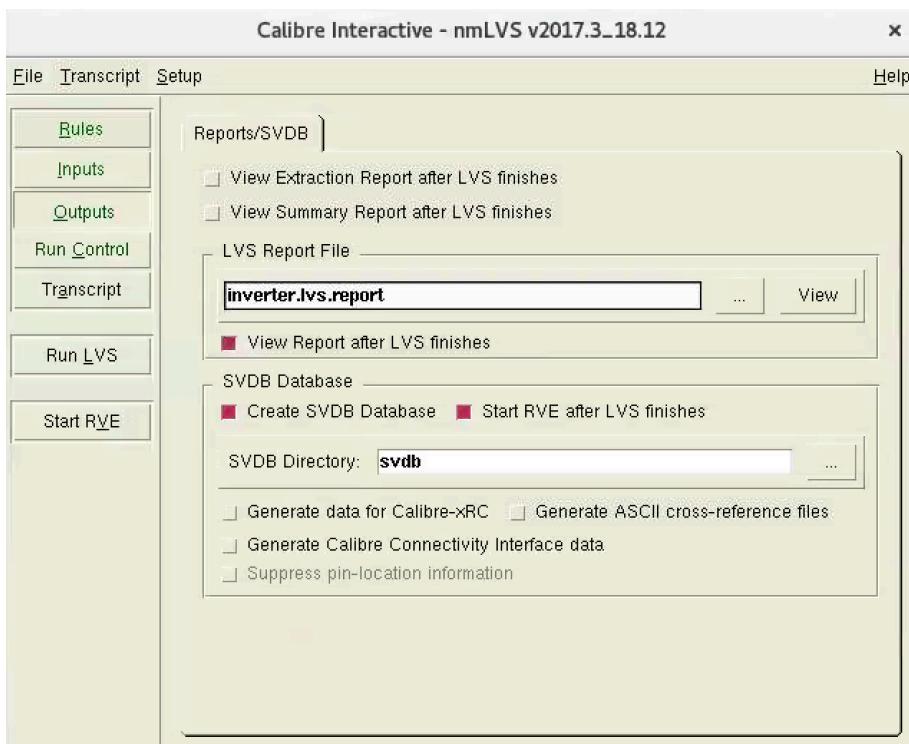
Layout tab: Select the option **Export from layout viewer**



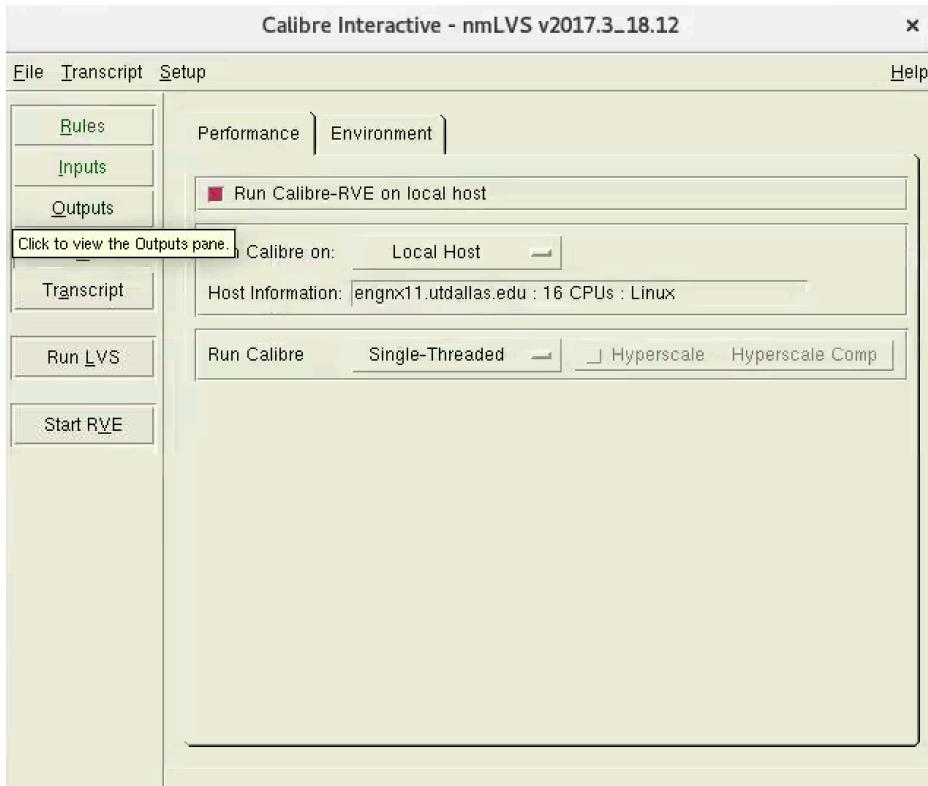
Netlist tab: Select the option **Export from schematic viewer**, Format: SPICE



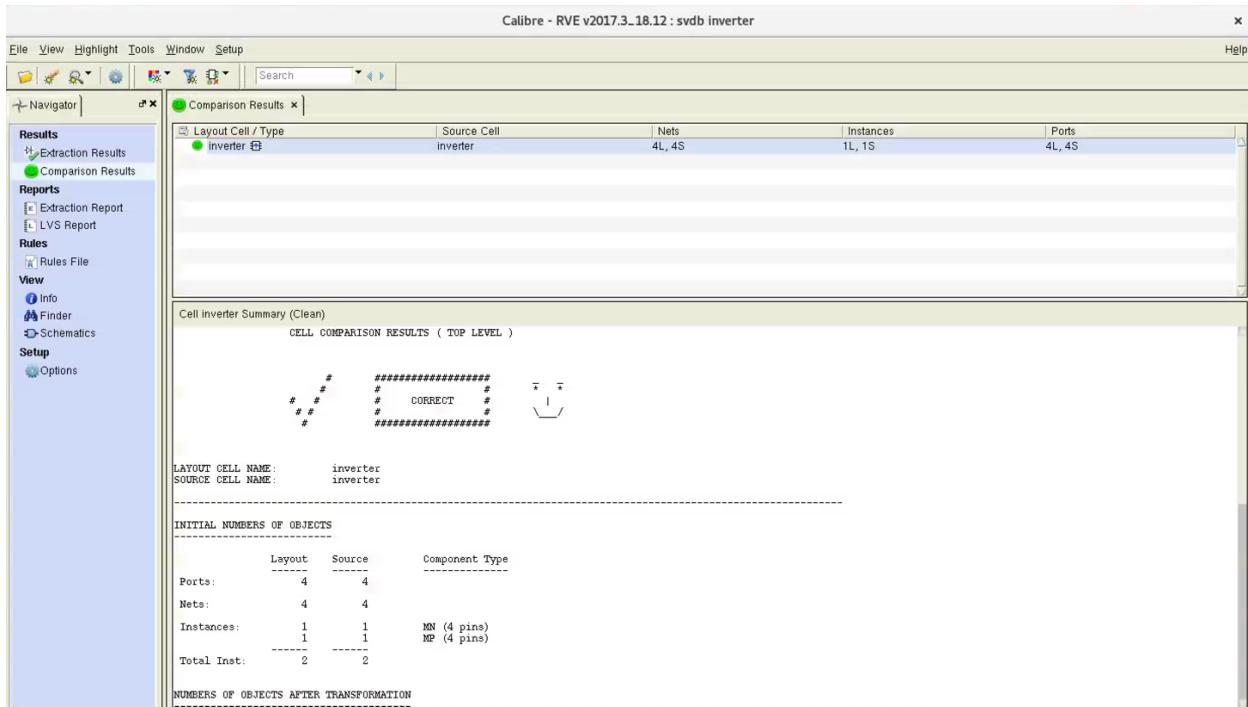
**Outputs:**



### Run Control:



## Click on Run LVS

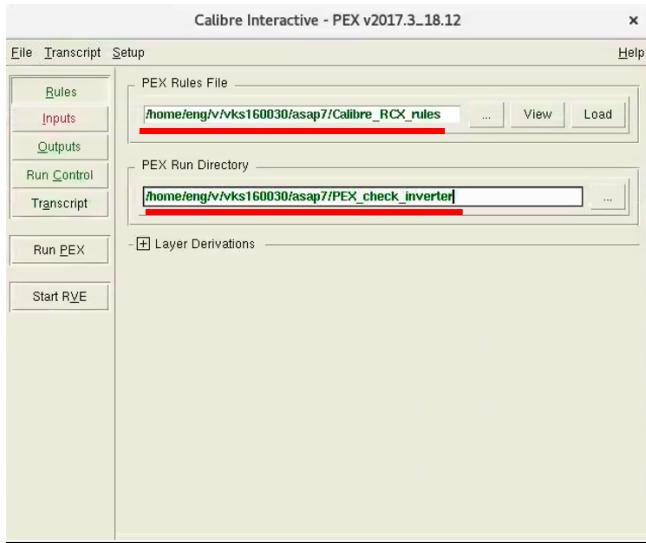


## Parasitic Extraction

**Rules:** In the layout view, Calibre -> Run PEX

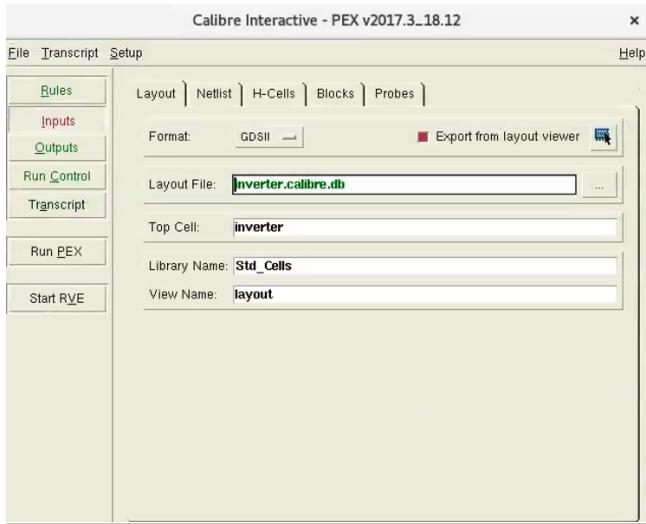
**Rules:** In PEX Rules File, browse and select the **Calibre\_RCX\_Rules** file which is in **your** work directory (asap7)

In PEX Run Directory, if you are unable to edit in the interactive window, go to files and create a new directory and browse that directory in the interactive window.

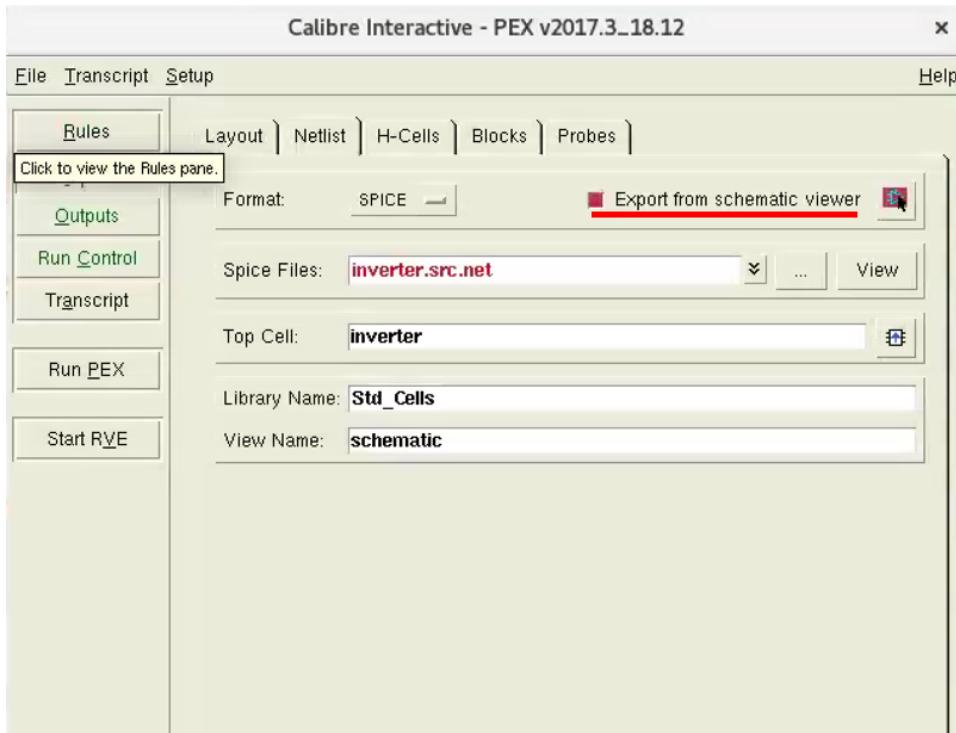


### Inputs:

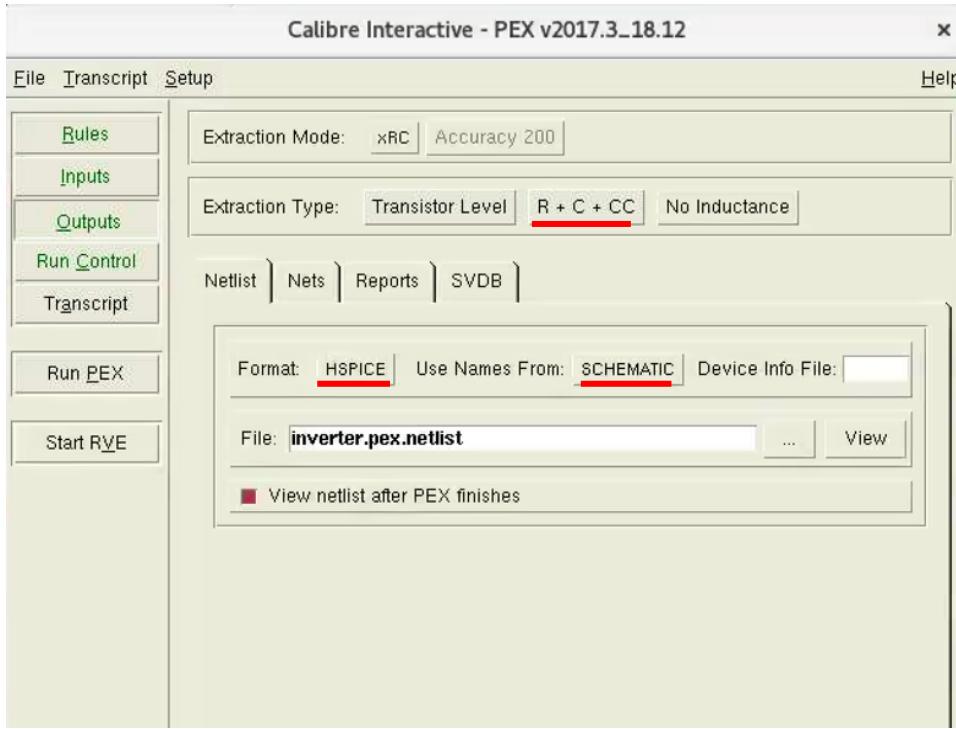
Layout tab: Select the option **Export from layout viewer**



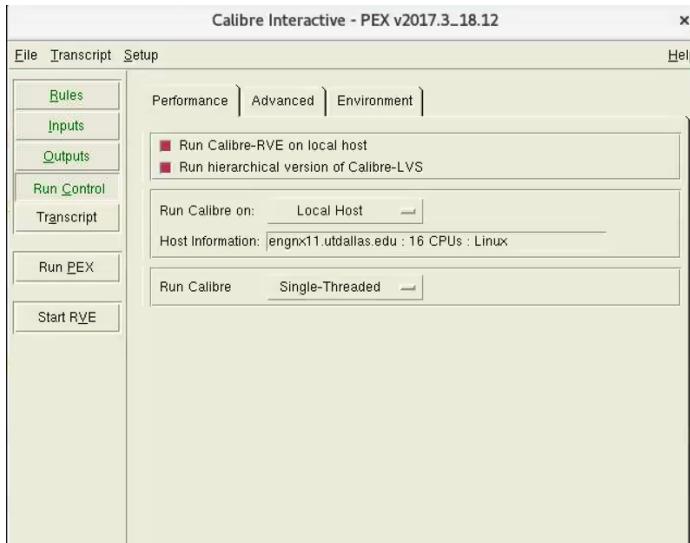
Netlist tab: Select the option **Export from schematic viewer**, Format: SPICE



**Outputs:** Format -> HSPICE, Use Names From -> SCHEMATIC



**Run Control**



Click on Run PEX

Ignore the 6 warnings.

```

Calibre Interactive - PEX v2017.3_18.12          PEX Netlist File - inverter.pex.netlist
File Transcript Setup                                File Edit Options Windows
Help
Rules Inputs Outputs Run Control Transcript Run PEX Start RVE
// makes no warranties, express or implied with respect to software
// including any warranty of merchantability or fitness for a
// particular purpose.
//
// LIMITATION OF LIABILITY: Mentor Graphics is not liable for any
// property damage, personal injury, loss of profits, interruption
// of business, or for any other special, consequential or
// incidental damages, however caused, whether for breach of
// warranty, negligence, strict liability, negligent misstatement
// or otherwise. In no event shall Mentor Graphics' liability
// exceed the amount paid for the product giving rise
// to the claim.
INFO: Map for layout placement hierarchy takes 1.6440e-02 Mbytes.
INFO: Net summary reporting completed.
--- NET SUMMARY REPORTING ENDING TIME = Fri Aug 21 13:10:16 2020
--- TOTAL CPU TIME = 0 REAL TIME = 1 LVMEM = 3/9/268 MALLOC = 105/105/187 ELI
=====
CALIBRE XRC WARNING / ERROR Summary
=====
XRC Warnings = 0
=====
--- CALIBRE XRC :FORMATTER COMPLETED - Fri Aug 21 13:10:16 2020
--- TOTAL CPU TIME = 1 REAL TIME = 2 LVMEM = 3/9/268 MALLOC = 105/105/187 ELI
=====

6 Warnings
Layer "psub" is not mapped to a calibrated layer.
Layer "psub" is not mapped to a calibrated layer.
Alias layer "XCALIBRATE_Active" is not coplanar with primary layer "XCALIBRATE_Active".
Alias layer "XCALIBRATE_SDT" is not coplanar with primary layer "XCALIBRATE_LSD".
No ground net name defined in PEX NETLIST statement and "0" will be used in the netlist.
PEX TEMPERATURE is set, but TC1/TC2 is not defined.

```

Parasitic extraction of inverter is now completed.

Go to the location where you saved **inverter.pex.netlist** file and use this file to run HSPICE.

## HSPICE

Make a new directory for HSPICE simulations in your work directory

```
mkdir ~/asap7/hspice
```

```
cd ~/asap7/hspice
```

Make another directory for inverter files

```
mkdir inverter
```

```
cd inverter
```

Copy the parasitic extracted files into this directory: 3 files should be copied into this location

⇒ inverter.pex.netlist

⇒ inverter.pex.netlist.pex

⇒ inverter.pex.netlist.INVERTER.pxi

Create a hspice file:

```
gedit inverter_hspice.sp
```

```
$example HSPICE setup file

$transistor model
.include "~/asap7/7nm_TT.pm"

.include inverter.pex.netlist

.option post runlvl=5

xi GND! VDD! IN OUT inverter

VDD! VDD! GND! 0.7v

$make changes below as per requirement
vin IN GND! pwl(0ps 0.7v 1000ps 0.7v 1210.7ps 0v 2000ps 0v 2210.7ps 0.7v)
cout OUT GND! 0.72fF

$transient analysis
.tr 1ps 3000ps

.end
```

Transistor Model file **7nm\_TT.pm** is already available in your work directory

Save this file and run HSPICE

```
. /proj/cad/startup/profile.synopsys_2016  
hspice inverter_hspice.sp  
Run Waveview and analyze the results  
wv&
```

For more details about analyzing results: <https://personal.utdallas.edu/~Xiangyu.Xu/wv/>