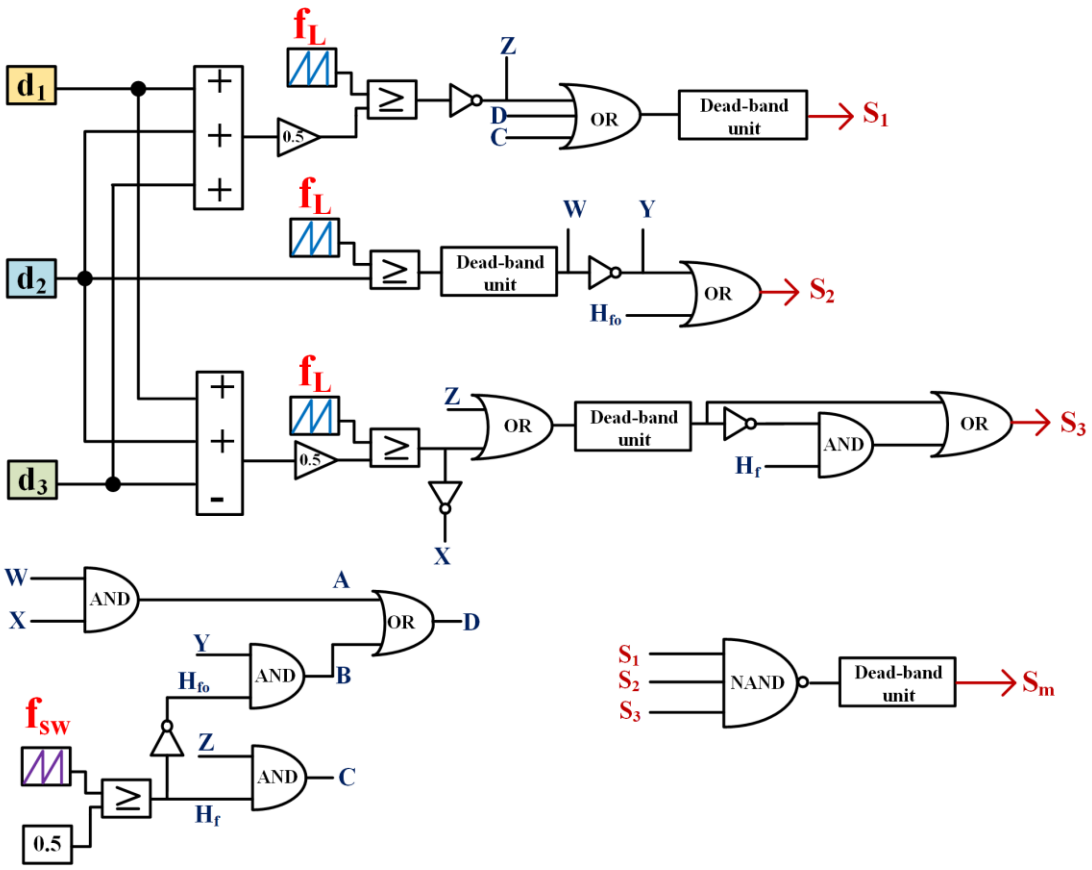
- **Control logic diagram:**



- **Description of control logic:**

The load duty cycles d_1, d_2 and d_3 are decided based on the required load powers. A combined duty ratio $(d_1+d_2+d_3)/2$ is compared with a low-frequency reference signal f_L, and the resulting signal is inverted and logically combined with auxiliary control inputs C and D through a three-input OR gate to produce gating pulse V_{gs1}. Similarly, d_2 is compared with f_L, and the inverted output is ORed with the high-frequency signal H_{fo} to produce V_{gs2}. The third gating pulse V_{gs3} is derived from $(d_1+d_2-d_3)/2$ compared with f_L, logically processed with the signal Z, and combined with H_f signal through OR and AND operations. The three pulses V_{gs1}, V_{gs2} and V_{gs3} are further combined using a NAND gate to obtain the final signal V_{gsm}. A

dead-band circuit is provided for all gating pulses to mitigate switching overlap and ensure reliable inverter operation.