ECE-585 Microprocessor System Design
DDR5 Memory Scheduler Test Plans on Closed Page Policy

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Policy Description:
We implemented a Level 0 - closed page policy with all banks precharged initially and precharged before processing any input request from the queue.

Approach to implementation: When the time of request from the input file matches the CPU clock ticks, we read into the queue, and at the next DRAM or DIMM clock, the request processing will start. The request is marked completed and removed from the queue only after the precharge of that bank is finished. So here, based on the policy we chose, all the timing parameters are satisfied within the timings tRCD, tRTP (or tCL, tburst) and tRP

Testcase1:

This testcase was used to verify if the Memory Scheduler can perform sequential reads and follows proper timings. When input time is at 111, it reads and issues the first command at 112. At 880, DRAM is ready for the next command, bit as we received input request at 880, it will be taken up an processed at next cycle. again at 1137 input request, by 1138, previous precharge command's tRP is satisfied and ready to issue next ACT0 command

Input Trace file:

time	core	op	address
111	1	2	01FFFFC00
112	2	2	01A254D11
313	3	2	10FFFFE22
880	4	2	012514F33
1137	5	2	01FFFFC40

Output:

	Time	Channel	Command	Bank	Bankgroup	Address
	112	0	ACT0	0	3	07FF
	114	0	ACT1	0	3	07FF
	190	0	RD0	0	3	3F0
	192	0	RD1	0	3	3F0
111	266	0	PRE	0	3	
	342	0	ACT0	2	3	689

112

	344	0	ACT1	2	3	689
	420	0	RD0	2	3	144
	422	0	RD1	2	3	144
	496	0	PRE	2	3	
	572	0	ACT0	4	3	43FF
	574	0	ACT1	4	3	43FF
	650	0	RD0	4	3	3F8
	652	0	RD1	4	3	3F8
313	726	0	PRE	4	3	
	882	0	ACT0	6	3	494
	884	0	ACT1	6	3	494
	960	0	RD0	6	3	14C
	962	0	RD1	6	3	14C
880	1036	0	PRE	6	3	
	1138	1	ACT0	0	3	07FF
	1140	1	ACT1	0	3	07FF
	1216	1	RD0	0	3	3F0
	1218	1	RD1	0	3	3F0
1137	1292	1	PRE	0	3	
			End of Simulation			

TEST PASSED. VALIDATED

Testcase2:

To verify the Memory Scheduler is able to read the request with different timing and large time advancement

Input Trace file:

time	core	op	address
10	1	0	01FFFFC00
22	2	1	01A254D11
41	3	2	10FFFFE22
55	4	0	012514F33
106	5	1	01FFFFC40
1000	6	0	01A254D11
10100	7	1	01FFFFC00

Output:

	time	channel	command	bankgroup	bank	row/col
	12	0	ACT0	0	3	07FF
	14	0	ACT1	0	3	07FF
	90	0	RD0	0	3	3F0
	92	0	RD1	0	3	3F0
10	166	0	PRE	0	3	
	242	0	ACT0	2	3	0689
	244	0	ACT1	2	3	0689
	320	0	WR0	2	3	144
	322	0	WR1	2	3	144
22	474	0	PRE	2	3	
	550	0	ACT0	4	3	43FF
	552	0	ACT1	4	3	43FF
	628	0	RD0	4	3	3F8
	630	0	RD1	4	3	3F8
41	704	0	PRE	4	3	
	780	0	ACT0	6	3	0494
	782	0	ACT1	6	3	0494
	858	0	RD0	6	3	14C
	860	0	RD1	6	3	14C
55	934	0	PRE	6	3	
	1010	1	ACT0	0	3	07FF
	1012	1	ACT1	0	3	07FF
	1088	1	WR0	0	3	3F0
	1090	1	WR1	0	3	3F0
106	1242	1	PRE	0	3	
	1318	0	ACT0	2	3	0689
	1320	0	ACT1	2	3	0689
	1396	0	RD0	2	3	144
	1398	0	RD1	2	3	144
1000	1472	0	PRE	2	3	
	10102	0	ACT0	0	3	07FF
	10104	0	ACT1	0	3	07FF
	10180	0	WR0	0	3	3F0
	10182	0	WR1	0	3	3F0
10100	10334	0	PRE	0	3	
			end of simulation			

TEST PASSED. VALIDATED

Testcase 3:

To verify the Memory Scheduler is able to perform 2 writes and one read in order

Input Trace file:

time	core	op	address
0	1	1	01FFFFC00
2	2	1	01A254D11
3	3	0	10FFFFE22
4	4	1	012514F33
500	5	1	01FFFFC40

Output:

	time	channel	cmd	bankgroup	bank	row/col
	2	0	ACT0	0	3	07FF
	4	0	ACT1	0	3	07FF
	80	0	WR0	0	3	3F0
	82	0	WR1	0	3	3F0
0	234	0	PRE	0	3	
	310	0	ACT0	2	3	689
	312	0	ACT1	2	3	689
	388	0	WR0	2	3	144
	390	0	WR1	2	3	144
2	542	0	PRE	2	3	
	618	0	ACT0	4	3	43FF
	620	0	ACT1	4	3	43FF
	696	0	RD0	4	3	3F8
	698	0	RD1	4	3	3F8
3	772	0	PRE	4	3	
	848	0	ACT0	6	3	494
	850	0	ACT1	6	3	494
	926	0	WR0	6	3	14C
	928	0	WR1	6	3	14C
4	1080	0	PRE	6	3	
	1156	1	ACT0	0	3	07FF
	1158	1	ACT1	0	3	07FF
	1234	1	WR0	0	3	3F0
	1236	1	WR1	0	3	3F0
500	1388	1	PRE	0	3	
			End of Simulatio			

			n			

TEST PASSED. VALIDATED

Testcase 4:

To verify the Memory Scheduler is able to perform 2 simultaneous reads and one write. Here the cases considered are 2 consecutive reads to same address followed a write to different one at a very later time. After this 2 reads and one write to same address at immediate clock tick. Then 2 different reads (inst fetch and data read) for 2 different addresses followed by a write to a different address

Input Trace file:

time	core	op	address
1	1	0	01FFFFC00
2	2	0	01FFFFC00
3000	3	1	10FFFFE22
4000	4	2	012514F33
4001	5	2	012514F33
4002	1	1	012514F33
4003	2	0	01A254D11
4004	3	2	01FFFFC40
4005	4	1	01FFFFC00

Output:

	time	channel	cmd	bankgroup	bank	row/col
	2	0	ACT0	0	3	07FF
	4	0	ACT1	0	3	07FF
	80	0	RD0	0	3	3F0
	82	0	RD1	0	3	3F0
1	156	0	PRE	0	3	
	232	0	ACT0	0	3	07FF
	234	0	ACT1	0	3	07FF
	310	0	RD0	0	3	3F0
	312	0	RD1	0	3	3F0
2	386	0	PRE	0	3	
	3002	0	ACT0	4	3	43FF
	3004	0	ACT1	4	3	43FF
	3080	0	WR0	4	3	3F8
	3082	0	WR1	4	3	3F8
3000	3234	0	PRE	4	3	
	4002	0	ACT0	6	3	494
4000						

	4004	0	ACT1	6	3	494
	4080	0	RD0	6	3	14C
	4082	0	RD1	6	3	14C
	4156	0	PRE	6	3	
	4232	0	ACT0	6	3	494
	4234	0	ACT1	6	3	494
	4310	0	RD0	6	3	14C
	4312	0	RD1	6	3	14C
4001	4386	0	PRE	6	3	
	4462	0	ACT0	6	3	494
	4464	0	ACT1	6	3	494
	4540	0	WR0	6	3	14C
	4542	0	WR1	6	3	14C
4002	4694	0	PRE	6	3	
	4770	0	ACT0	2	3	689
	4772	0	ACT1	2	3	689
	4848	0	RD0	2	3	144
	4850	0	RD1	2	3	144
4003	4924	0	PRE	2	3	
	5000	1	ACT0	0	3	07FF
	5002	1	ACT1	0	3	07FF
	5078	1	RD0	0	3	3F0
	5080	1	RD1	0	3	3F0
4004	5154	1	PRE	0	3	
	5230	0	ACT0	0	3	07FF
	5232	0	ACT1	0	3	07FF
	5308	0	WR0	0	3	3F0
	5310	0	WR1	0	3	3F0
4005	5462	0	PRE	0	3	
			End of Simulation			

TEST PASSED. VALIDATED

Testcase 5:

To verify the Memory Scheduler is able to process sequential requests which are to the different Column, Bank and Bank Group in different Row

Input Trace file:

time	core	op	address

1	1	0	01FFFFC00
2	2	1	10FFFA252
3	3	2	11FFF0182
4	4	0	01FFF054C
5	5	1	10FFFB211

Output:

	Time	Channel	Command	Bank group	Bank	Address
	2	0	ACT0	0	3	07FF
	4	0	ACT1	0	3	07FF
	80	0	RD0	0	3	3F0
	82	0	RD1	0	3	3F0
1	156	0	Pre	0	3	
	232	1	ACT0	4	0	43FF
	234	1	ACT1	4	0	43FF
	310	1	WR0	4	0	3a4
	312	1	WR1	4	0	3a4
2	464	1	Pre	4	0	
	540	0	ACT0	3	0	47FF
	542	0	ACT1	3	0	47FF
	618	0	RD0	3	0	300
	620	0	RD1	3	0	300
3	694	0	Pre	3	0	
	770	1	ACT0	2	1	07FF
	772	1	ACT1	2	1	07FF
	848	1	RD0	2	1	303
	850	1	RD1	2	1	303
4	924	1	Pre	2	1	
	1000	0	ACT0	4	0	43FF
	1002	0	ACT1	4	0	43FF
	1078	0	WR0	4	0	3B4
	1080	0	WR1	4	0	3B4
5	1232	0	Pre	4	0	
		End of Simulation				

TEST PASSED. VALIDATED

Testcase 6:

To verify the Memory Scheduler is able to process sequential requests which are to the same Bank, Bank Group and different Row in same Column

Input Trace file:

time	core	op	address
1	1	0	01FFFFC00
2	2	1	0587FFC01
3	3	2	0F1AFFC02
4	4	0	10FFFFC03
5	5	1	01CAFFC00

Output:

	Time	Channel	Command	Bank group	Bank	Address
	2	0	ACT0	0	3	07FF
	4	0	ACT1	0	3	07FF
	80	0	RD0	0	3	3F0
	82	0	RD1	0	3	3F0
1	156	0	Pre	0	3	
	232	0	ACT0	0	3	161F
	234	0	ACT1	0	3	161F
	310	0	WR0	0	3	3F0
	312	0	WR1	0	3	3F0
2	464	0	Pre	0	3	
	540	0	ACT0	0	3	3C6B
	542	0	ACT1	0	3	3C6B
	618	0	RD0	0	3	3F0
	620	0	RD1	0	3	3F0
3	694	0	Pre	0	3	
	770	0	ACT0	0	3	43FF
	772	0	ACT1	0	3	43FF
	848	0	RD0	0	3	3F0
	850	0	RD1	0	3	3F0
4	924	0	Pre	0	3	
	1000	0	ACT0	0	3	072B
	1002	0	ACT1	0	3	072B
	1078	0	WR0	0	3	3F0
	1080	0	WR1	0	3	3F0
5	1232	0	Pre	0	3	
		End of Simulation				

TEST PASSED. VALIDATED

Testcase 7:

To verify the Memory Scheduler is able to process the sequential requests which is to the same Column, Bank and Bank Group in same Row

Input File:

time	core	op	address
1	1	0	01FFFFC00
2	2	1	01FFFFC01
3	3	2	01FFFFC02
4	4	0	01FFFFC03
5	5	1	01FFFFC00

Output:

	Time	Channel	Command	Bankgroup	Bank	Address
	2	0	ACT0	0	3	07ff
	4	0	ACT1	0	3	07ff
	80	0	RD0	0	3	3f0
	82	0	RD1	0	3	3f0
1	156	0	PRE	0	3	
	232	0	ACT0	0	3	07ff
	234	0	ACT1	0	3	07ff
	310	0	WR0	0	3	3f0
	312	0	WR1	0	3	3f0
2	464	0	PRE	0	3	
	540	0	ACT0	0	3	07ff
	542	0	ACT1	0	3	07ff
	618	0	RD0	0	3	3f0
	620	0	RD1	0	3	3f0
3	694	0	PRE	0	3	
	770	0	ACT0	0	3	07ff
	772	0	ACT1	0	3	07ff
	848	0	RD0	0	3	3f0
	850	0	RD1	0	3	3f0
4	924	0	PRE	0	3	
	1000	0	ACT0	0	3	07ff
	1002	0	ACT1	0	3	07ff
	1078	0	WR0	0	3	3f0
	1080	0	WR1	0	3	3f0
5	1232	0	PRE	0	3	
		End of				

		Simulation				

TEST PASSED. VALIDATED

Testcase 8:

To verify the Memory Scheduler is able to process the request which is to the same Bank, Bank Group, same Row and different Column

Input:

time	core	op	address
1	1	0	01FFFFC00
2	2	1	01FFFEC04
3	3	2	01FFF6C05
4	4	0	01FFFAC06
5	5	1	01FFF3C07

Output:

	Time	Channel	Command	Bankgroup	Bank	Address
	2	0	ACT0	0	3	07ff
	4	0	ACT1	0	3	07ff
	80	0	RD0	0	3	3f0
	82	0	RD1	0	3	3f0
1	156	0	PRE	0	3	
	232	0	ACT0	0	3	07ff
	234	0	ACT1	0	3	07ff
	310	0	WR0	0	3	3e1
	312	0	WR1	0	3	3e1
2	464	0	PRE	0	3	
	540	0	ACT0	0	3	07ff
	542	0	ACT1	0	3	07ff
	618	0	RD0	0	3	361
	620	0	RD1	0	3	361
3	694	0	PRE	0	3	
	770	0	ACT0	0	3	07ff
	772	0	ACT1	0	3	07ff
	848	0	RD0	0	3	3a1
	850	0	RD1	0	3	3a1
4	924	0	PRE	0	3	
5	1000	0	ACT0	0	3	07ff

	1002	0	ACT1	0	3	07ff
	1078	0	WR0	0	3	331
	1080	0	WR1	0	3	331
	1232	0	PRE	0	3	
		End of Simulation				

TEST PASSED. VALIDATED

Testcase 9:

To verify the Memory Scheduler is able to process the sequential requests which is to the same Column, Bank Group, same Row and Different Bank

Input:

time	core	op	address
1	1	0	01FFFFC00
2	2	1	01FFFF001
3	3	2	01FFFF402
4	4	0	01FFFF803
5	5	1	01FFFFC00

Output:

	Time	Channel	Command	Bankgroup	Bank	Address
	2	0	ACT0	0	3	07ff
	4	0	ACT1	0	3	07ff
	80	0	RD0	0	3	3f0
	82	0	RD1	0	3	3f0
1	156	0	PRE	0	3	
	232	0	ACT0	0	0	07ff
	234	0	ACT1	0	0	07ff
	310	0	WR0	0	0	3f0
	312	0	WR1	0	0	3f0
2	464	0	PRE	0	0	
	540	0	ACT0	0	1	07ff
	542	0	ACT1	0	1	07ff
	618	0	RD0	0	1	3f0
	620	0	RD1	0	1	3f0
3	694	0	PRE	0	1	
4	770	0	ACT0	0	2	07ff

	772	0	ACT1	0	2	07ff
	848	0	RD0	0	2	3f0
	850	0	RD1	0	2	3f0
	924	0	PRE	0	2	
	1000	0	ACT0	0	3	07ff
	1002	0	ACT1	0	3	07ff
	1078	0	WR0	0	3	3f0
	1080	0	WR1	0	3	3f0
5	1232	0	PRE	0	3	
		End of Simulation				

TEST PASSED. VALIDATED

Testcase 10:

To verify the Memory Scheduler is able to process the sequential requests which is to the same Column, Bank, same Row and different Bank Group

Input:

time	core	op	address
1	1	0	01FFFFC00
2	2	1	01FFFFF01
3	3	2	01FFFF202
4	4	0	01FFFF103
5	5	1	01FFFFC00

Output:

	Time	Channel	Command	Bank	Bankgroup	Address
	2	0	ACT0	0	3	07ff
	4	0	ACT1	0	3	07ff
	80	0	RD0	0	3	3f0
	82	0	RD1	0	3	3f0
1	156	0	PRE	0	3	
	232	0	ACT0	6	3	07ff
	234	0	ACT1	6	3	07ff
	310	0	WR0	6	3	3f0
	312	0	WR1	6	3	3f0
2	464	0	PRE	6	3	
	540	0	ACT0	4	0	07ff
	542	0	ACT1	4	0	07ff
3						

	618	0	RD0	4	0	3f0
	620	0	RD1	4	0	3f0
	694	0	PRE	4	0	
	770	0	ACT0	2	0	07ff
	772	0	ACT1	2	0	07ff
	848	0	RD0	2	0	3f0
	850	0	RD1	2	0	3f0
4	924	0	PRE	2	0	
	1000	0	ACT0	0	3	07ff
	1002	0	ACT1	0	3	07ff
	1078	0	WR0	0	3	3f0
	1080	0	WR1	0	3	3f0
5	1232	0	PRE	0	3	
		End of Simulation				

TEST PASSED. VALIDATED

Testcase 11:

To verify the Memory Scheduler is able to process sequential requests which are to the different Bank and Bank Group and same Row in same Column

Input:

time	core	op	address
1	1	0	01FFFFC00
2	2	1	01FFFFA00
3	3	2	01FFFF800
4	4	0	01FFFFC00
5	5	1	01FFFF900

Output:

	Time	Channel	Command	Bankgroup	Bank	Address
	2	0	ACT0	0	3	07ff
	4	0	ACT1	0	3	07ff
	80	0	RD0	0	3	3f0
	82	0	RD1	0	3	3f0
1	156	0	PRE	0	3	
	232	0	ACT0	4	2	07ff
	234	0	ACT1	4	2	07ff
	310	0	WR0	4	2	3f0
2						

	312	0	WR1	4	2	3f0
	464	0	PRE	4	2	
	540	0	ACT0	0	2	07ff
	542	0	ACT1	0	2	07ff
	618	0	RD0	0	2	3f0
	620	0	RD1	0	2	3f0
3	694	0	PRE	0	2	
	770	0	ACT0	0	3	07ff
	772	0	ACT1	0	3	07ff
	848	0	RD0	0	3	3f0
	850	0	RD1	0	3	3f0
4	924	0	PRE	0	3	
	1000	0	ACT0	2	2	07ff
	1002	0	ACT1	2	2	07ff
	1078	0	WR0	2	2	3f0
	1080	0	WR1	2	2	3f0
5	1232	0	PRE	2	2	
		End of Simulation				

TEST PASSED. VALIDATED

Testcase 12:

To verify the Memory Scheduler is able to process sequential requests which are to the same Bank, Bank Group and different Row in different Column

Input:

time	core	op	address
1	1	0	01FFFFC00
2	2	1	0587FFC04
3	3	2	0F1AFFC05
4	4	0	10FFFFC06
5	5	1	01CAFFC07

Output:

	Time	Channel	Command	Bankgroup	Bank	Address
	2	0	ACT0	0	3	07ff
	4	0	ACT1	0	3	07ff

1

	80	0	RD0	0	3	3f0
	82	0	RD1	0	3	3f0
	156	0	PRE	0	3	
	232	0	ACT0	0	3	161f
	234	0	ACT1	0	3	161f
	310	0	WR0	0	3	3f1
	312	0	WR1	0	3	3f1
2	464	0	PRE	0	3	
	540	0	ACT0	0	3	3c6b
	542	0	ACT1	0	3	3c6b
	618	0	RD0	0	3	3f1
	620	0	RD1	0	3	3f1
3	694	0	PRE	0	3	
	770	0	ACT0	0	3	43ff
	772	0	ACT1	0	3	43ff
	848	0	RD0	0	3	3f1
	850	0	RD1	0	3	3f1
4	924	0	PRE	0	3	
	1000	0	ACT0	0	3	072b
	1002	0	ACT1	0	3	072b
	1078	0	WR0	0	3	3f1
	1080	0	WR1	0	3	3f1
5	1232	0	PRE	0	3	
		End of Simulation				

TEST PASSED. VALIDATED

Testcase 13:

To verify the Memory Scheduler is able to process the sequential requests which are to the different Column, Bank and Bank Group with same Row

Input:

time	core	op	address
1	1	0	01FFFFC00
2	2	1	01FFFA252
3	3	2	01FFF0182
4	4	0	01FFF054C
5	5	1	01FFFB211

Output:

	Time	Channel	Command	Bank	Bankgroup	Address
	2	0	ACT0	0	3	07ff
	4	0	ACT1	0	3	07ff
	80	0	RD0	0	3	3f0
	82	0	RD1	0	3	3f0
1	156	0	PRE	0	3	
	232	1	ACT0	4	0	07ff
	234	1	ACT1	4	0	07ff
	310	1	WR0	4	0	3a4
	312	1	WR1	4	0	3a4
2	464	1	PRE	4	0	
	540	0	ACT0	3	0	07ff
	542	0	ACT1	3	0	07ff
	618	0	RD0	3	0	300
	620	0	RD1	3	0	300
3	694	0	PRE	3	0	
	770	1	ACT0	2	1	07ff
	772	1	ACT1	2	1	07ff
	848	1	RD0	2	1	303
	850	1	RD1	2	1	303
4	924	1	PRE	2	1	
	1000	0	ACT0	4	0	07ff
	1002	0	ACT1	4	0	07ff
	1078	0	WR0	4	0	3b4
	1080	0	WR1	4	0	3b4
5	1232	0	PRE	4	0	
		End of Simulation				

TEST PASSED. VALIDATED

Testcase 14:

To verify the Memory Scheduler is able to process the sequential requests which are to the different Column, Bank and Bank Group with same Row

Input:

time	core	op	address
1	1	0	01FFFFC00
2	2	1	100FFF241
3	3	2	01AAFF402

4	4	0	01F5FF800
5	5	1	01FFFFC00

Output:

	Time	Channel	Command	Bankgroup	Bank	Address
	2	0	ACT0	0	3	07ff
	4	0	ACT1	0	3	07ff
	80	0	RD0	0	3	3f0
	82	0	RD1	0	3	3f0
1	156	0	PRE	0	3	
	232	1	ACT0	4	0	403f
	234	1	ACT1	4	0	403f
	310	1	WR0	4	0	3f0
	312	1	WR1	4	0	3f0
2	464	1	PRE	4	0	
	540	0	ACT0	0	1	06ab
	542	0	ACT1	0	1	06ab
	618	0	RD0	0	1	3f0
	620	0	RD1	0	1	3f0
3	694	0	PRE	0	1	
	770	0	ACT0	0	2	07d7
	772	0	ACT1	0	2	07d7
	848	0	RD0	0	2	3f0
	850	0	RD1	0	2	3f0
4	924	0	PRE	0	2	
	1000	0	ACT0	0	3	07ff
	1002	0	ACT1	0	3	07ff
	1078	0	WR0	0	3	3f0
	1080	0	WR1	0	3	3f0
5	1232	0	PRE	0	3	
		End of Simulation				

TEST PASSED. VALIDATED

Testcase 15:

To verify the Memory Scheduler is able to process the sequential requests which are to the different Column, Bank and Bank Group with same Row

Input:

time	core	op	address
1	1	0	01FFFFC00
2	2	1	01A254011
3	3	2	10FFFF422
4	4	0	012514833
5	5	1	01FFFF840

Output:

	Time	Channel	Command	Bankgroup	Bank	Address
	2	0	ACT0	0	3	07ff
	4	0	ACT1	0	3	07ff
	80	0	RD0	0	3	3f0
	82	0	RD1	0	3	3f0
1	156	0	PRE	0	3	
	232	0	ACT0	0	0	689
	234	0	ACT1	0	0	689
	310	0	WR0	0	0	144
	312	0	WR1	0	0	144
2	464	0	PRE	0	0	
	540	0	ACT0	0	1	43ff
	542	0	ACT1	0	1	43ff
	618	0	RD0	0	1	3f8
	620	0	RD1	0	1	3f8
3	694	0	PRE	0	1	
	770	0	ACT0	0	2	494
	772	0	ACT1	0	2	494
	848	0	RD0	0	2	14c
	850	0	RD1	0	2	14c
4	924	0	PRE	0	2	
	1000	1	ACT0	0	2	07ff
	1002	1	ACT1	0	2	07ff
	1078	1	WR0	0	2	3f0
	1080	1	WR1	0	2	3f0
5	1232	1	PRE	0	2	
		End of Simulation				

TEST PASSED. VALIDATED

Testcase 16:

To verify the Memory Scheduler is able to work for sequential data read operations from different addresses

Input:

time	core	op	address
1	1	0	01FFFFC00
2	2	0	01A254D11
3	3	0	10FFFFE22
4	4	0	012514F33
5	5	0	01FFFFC40

Output:

	Time	Channel	Command	Bankgroup	Bank	Address
	2	0	ACT0	0	3	07ff
	4	0	ACT1	0	3	07ff
	80	0	RD0	0	3	3f0
	82	0	RD1	0	3	3f0
1	156	0	PRE	0	3	
	232	0	ACT0	2	3	689
	234	0	ACT1	2	3	689
	310	0	RD0	2	3	144
	312	0	RD1	2	3	144
2	386	0	PRE	2	3	
	462	0	ACT0	4	3	43ff
	464	0	ACT1	4	3	43ff
	540	0	RD0	4	3	3f8
	542	0	RD1	4	3	3f8
3	616	0	PRE	4	3	
	692	0	ACT0	6	3	494
	694	0	ACT1	6	3	494
	770	0	RD0	6	3	14c
	772	0	RD1	6	3	14c
4	846	0	PRE	6	3	
	922	1	ACT0	0	3	07ff
	924	1	ACT1	0	3	07ff
	1000	1	RD0	0	3	3f0
	1002	1	RD1	0	3	3f0
5	1076	1	PRE	0	3	
		End of Simulation				

TEST PASSED. VALIDATED

Testcase 17:

To verify the Memory Scheduler is able to process sequential requests which are to the different Row, Column and Bank Group in same Bank

Input:

time	core	op	address
1111	1	0	01FFFFC00
2222	2	1	01A254D11
3333	3	2	10FFFFE22
4444	4	2	012514F33
5555	5	1	01FFFFC40
6666	6	1	01FFFFC00
7777	7	1	01A254D11
8888	8	2	10FFFFE22
9999	9	2	012514F33
11111	10	0	01FFFFC40
22222	11	0	01FFFFC00
33333	12	2	01A254D11
44444	1	1	10FFFFE22
55555	2	2	012514F33
66666	3	0	01FFFFC40
77777	4	1	01FFFFC00
88888	5	2	01A254D11
99999	6	0	10FFFFE22
111111	7	1	012514F33
222222	8	0	01FFFFC40

Output:

	Time	Channel	Command	Bankgroup	Bank	Address
	1112	0	ACT0	0	3	07ff
	1114	0	ACT1	0	3	07ff
	1190	0	RD0	0	3	3f0
	1192	0	RD1	0	3	3f0

1111

	1266	0	PRE	0	3	
	2224	0	ACT0	2	3	689
	2226	0	ACT1	2	3	689
	2302	0	WR0	2	3	144
	2304	0	WR1	2	3	144
2222	2456	0	PRE	2	3	
	3334	0	ACT0	4	3	43ff
	3336	0	ACT1	4	3	43ff
	3412	0	RD0	4	3	3f8
	3414	0	RD1	4	3	3f8
3333	3488	0	PRE	4	3	
	4446	0	ACT0	6	3	494
	4448	0	ACT1	6	3	494
	4524	0	RD0	6	3	14c
	4526	0	RD1	6	3	14c
4444	4600	0	PRE	6	3	
	5556	1	ACT0	0	3	07ff
	5558	1	ACT1	0	3	07ff
	5634	1	WR0	0	3	3f0
	5636	1	WR1	0	3	3f0
5555	5788	1	PRE	0	3	
	6668	0	ACT0	0	3	07ff
	6670	0	ACT1	0	3	07ff
	6746	0	WR0	0	3	3f0
	6748	0	WR1	0	3	3f0
6666	6900	0	PRE	0	3	
	7778	0	ACT0	2	3	689
	7780	0	ACT1	2	3	689
	7856	0	WR0	2	3	144
	7858	0	WR1	2	3	144
7777	8010	0	PRE	2	3	
	8890	0	ACT0	4	3	43ff
	8892	0	ACT1	4	3	43ff
	8968	0	RD0	4	3	3f8
	8970	0	RD1	4	3	3f8
8888	9044	0	PRE	4	3	
	10000	0	ACT0	6	3	494
	10002	0	ACT1	6	3	494
	10078	0	RD0	6	3	14c
	10080	0	RD1	6	3	14c
9999	10154	0	PRE	6	3	
	11112	1	ACT0	0	3	07ff
	11114	1	ACT1	0	3	07ff
11111						

	11190	1	RD0	0	3	3f0
	11192	1	RD1	0	3	3f0
	11266	1	PRE	0	3	
	22224	0	ACT0	0	3	07ff
	22226	0	ACT1	0	3	07ff
	22302	0	RD0	0	3	3f0
	22304	0	RD1	0	3	3f0
22222	22378	0	PRE	0	3	
	33334	0	ACT0	2	3	689
	33336	0	ACT1	2	3	689
	33412	0	RD0	2	3	144
	33414	0	RD1	2	3	144
33333	33488	0	PRE	2	3	
	44446	0	ACT0	4	3	43ff
	44448	0	ACT1	4	3	43ff
	44524	0	WR0	4	3	3f8
	44526	0	WR1	4	3	3f8
44444	44678	0	PRE	4	3	
	55556	0	ACT0	6	3	494
	55558	0	ACT1	6	3	494
	55634	0	RD0	6	3	14c
	55636	0	RD1	6	3	14c
55555	55710	0	PRE	6	3	
	66668	1	ACT0	0	3	07ff
	66670	1	ACT1	0	3	07ff
	66746	1	RD0	0	3	3f0
	66748	1	RD1	0	3	3f0
66666	66822	1	PRE	0	3	
	77778	0	ACT0	0	3	07ff
	77780	0	ACT1	0	3	07ff
	77856	0	WR0	0	3	3f0
	77858	0	WR1	0	3	3f0
77777	78010	0	PRE	0	3	
	88890	0	ACT0	2	3	689
	88892	0	ACT1	2	3	689
	88968	0	RD0	2	3	144
	88970	0	RD1	2	3	144
88888	89044	0	PRE	2	3	
	100000	0	ACT0	4	3	43ff
	100002	0	ACT1	4	3	43ff
	100078	0	RD0	4	3	3f8
	100080	0	RD1	4	3	3f8

99999

	100154	0	PRE	4	3	
	111112	0	ACT0	6	3	494
	111114	0	ACT1	6	3	494
	111190	0	WR0	6	3	14c
	111192	0	WR1	6	3	14c
111111	111344	0	PRE	6	3	
	222224	1	ACT0	0	3	07ff
	222226	1	ACT1	0	3	07ff
	222302	1	RD0	0	3	3f0
	222304	1	RD1	0	3	3f0
222222	222378	1	PRE	0	3	

TEST PASSED. VALIDATED