Samar Perwez
Electrical Engineering
Indian Institute of Technology Bombay

22B3913
B.Tech.
Gender: Male
DOB: 11/08/2004

Examination	University	Institute	Year	CPI / %
Graduation	IIT Bombay	IIT Bombay	2026	
Intermediate	ISC	Lilavatibai Podar High School	2022	99.00%
Matriculation	ICSE	Lilavatibai Podar High School	2020	98.60%

Pursuing a **Minor** degree offered by Department of **Computer Science & Engineering**

Scholastic Achievements

- Secured **Department Rank 1** in Electrical Engineering Department among **120+** students in IIT Bombay *('24)*
- Received **13 AP** grades (awarded to the **top 1%**) in various courses including **Microprocessors**, **Digital Design**, **Signal Processing – I**, **Power Engineering – II** and **Data Structures & Algorithms** *('24)*
- Conferred with **Institute Prize** for securing **Institute Rank 6** among **1400+** students in IIT Bombay *('23)*
- Scored an **All India Rank** of **572** among 260,000+ candidates in the **JEE Advanced** Examination *('22)*
- Scored an **All India Rank** of **155** among 800,000+ candidates in the **JEE Main** Examination *('22)*
- Awarded the **Kishore Vaigyanik Protsahan Yojana (KVPY)** fellowship award by IISc Bangalore *('21)*

Professional Experience

University Research Intern | Technische Universität Braunschweig, Germany *(May'24 – Jul'24)*

*A **3-month on-site internship** under **Prof. Dr.-Ing Vadim Issakov** in the field of **CMOS design***

- Surveyed literature on design and analysis of **Voltage Controlled Oscillators** (VCOs) including the **Groszkowski Effect** and **Ali Hajimiri's** Linear Time Variant model using **Impulse Sensitivity Functions** (ISF).
- Streamlined and automated **ISF extraction** by leveraging **PXF & PSS analysis** in **Cadence** with a Python script.
- Contributed to the design and improvement of a **Class F VCO** in **22nm CMOS** technology with a frequency range of **19GHz - 21GHz** in **Cadence**, utilizing **3rd harmonic injection** for **waveform shaping** and **ISF analysis**.
- Tuned the VCO for a low phase noise of **-117dBc/Hz** and a high Figure of Merit of **-197dB** at an offset of 1MHz.

Key Projects

Pipelined Processor Design *(Jan'24 – May'24)*

Guide: Prof. Virendra Singh | Course Project | EE309

- Designed and simulated a **6-stage pipelined Reduced Instruction Set** architecture for a set of 26 instructions.
- Implemented custom blocks such as **Register Files**, ALU, **Pipeline Registers**, memory along with **Data Forwarding** and **Hazard Detection** functional units to handle edge cases, in **VHDL** using **Intel Quartus Prime**.
- Employed a 1-bit **Branch Predictor** with a **Least Recently Used** replacement policy to improve performance.
- Verified designs by executing **assembly programs** and conducting **RTL simulations** in a **ModelSim** environment, and subsequently, implemented them on an **FPGA** Board by mapping ports using the Pin Planner.

DSP using the 8051 Microcontroller *(Jan'24 – May'24)*

Guide: Prof. Nikhil Karamchandani | Course Project | EE337

- Designed and implemented a **Low-Pass Digital FIR Filter**, determining filter coefficients through **SciPy**, capturing input through an **ADC** and transmitting processed data through **serial transmission** using **PySerial**.
- Utilized **8051-Assembly** and **Embedded C** with **µVision Kiel** & **Flip** to program the Pt-51 development board.
- Configured **hardware timers**, interrupts, **SPI** & **UART** communication protocols and interfaced with peripherals such as keyboard, **analog-to-digital converters**, temperature sensors, **LCD displays**, keypads and speakers.

Multi-cycle CPU Design *(Aug'23 – Dec'23)*

Guide: Prof. Virendra Singh | Course Project | EE224

- Designed a **16-bit** reduced instruction set CPU as a **Finite State Machine** model having 19 states using VHDL.
- Developed **combinational logic** to execute 14 instructions including arithmetic, control flow and memory R/W.
- Created **Hardware Flowcharts** to achieve **minimal number of states** in the processor, enhancing efficiency.

Digital Logic Design *(Aug'23 – Dec'23)*

Guide: Prof. Siddharth Tallur | Course Project | EE214

- Modeled a **Sequence Detector** circuit as a **Mealy Type Finite State Machine** accepting arbitrary length words.
- Developed **8-bit ALU**, comparators, 4-bit adder-subtractors using **behavioral** & **structural** modeling in VHDL.
- Utilized **UrJTAG**, **ScanChain**, Intel Quartus to implement digital logic circuits on **Intel Xen 10 FPGA Board.**

Other Projects

Discrete Analog Circuit Design *(Jan'24 – May'24)*

Guide: Prof. Anil Kottanthrayanil | Course Project | EE230

- Designed and realized **square root amplifier** using **log** and **anti-log** stages calibrated with **diode characteristics** after performing detailed **simulations** in **LTSpice** to optimize performance and validate circuit behavior.
- Designed an **ECG amplifier** circuit with a **50Hz notch filter** and **amplification stages**, utilizing **Low Noise Amplifiers** with feedback to improve performance and captured **real-time** ECG signals on a **DSO** for analysis.
- Refined the ECG amplifier with a **right leg drive** and **advanced filtering sections**, reducing noise & interference.

Savitzky-Golay Digital Filter *(Aug'23 – Dec'23)*

Guide: Prof. Vikram M. Gadre | Course Project | EE229

- Performed application-focused literature review on the **Savitzky-Golay Filter** using articles from **IEEEXplore**.
- Demonstrated how a **finite impulse response** system allows for **fast and easy filtering** at the source of the signal.
- Implemented and demonstrated the **smoothening** of **noisy spectroscopic data** in Python using the digital filter.

Combinatorial Computing *(May'23 – Jul'23)*

Seasons of Code | Web and Coding Club, IIT Bombay

- Explored and applied concepts like **backtrack programming,** complexity theory and **dynamic programming**.
- Acquired knowledge about **SAT solvers** and developed a Sudoku solver using the **z3-solver library** in Python.
- Incorporated graph theory principles, including **Bipartite Matching**, the **Max Flow Min Cut Theorem**, and the **Ford-Fulkerson Algorithm**, to solve practical applications such as the optimization of worker-job assignments.

Image Recolorization *(Nov'23 – Dec'23)*

Winter in Data Science | Analytics Club, IIT Bombay

- Leveraged **Deep Learning** techniques, such as **Convolutional Neural Networks**, to colorize grayscale images.
- Predicted a* and b* **color channels** from lightness channel using **Lab color space** to achieve high-quality images.
- Implemented a complex neural network architecture featuring an **encoder-decoder framework** augmented by a **fusion layer**, supplemented with the **Inception ResNet v3 classifier** to enhance object recognition capabilities.

Computer Vision Project *(Aug'22 – Nov'22)*

Self – Project

- Created an **automated solution** for the measurement of **Contact Angle** of water drops from images to accurately determine surface tension aiding in **impurity estimation** and assessing the **quality of coating** on various surfaces.
- Utilized python library, **skimage** to perform **morphological image processing**, including **image segmentation**.
- Performed **polynomial regression** using **numpy** library on data points for **curve-fitting** and precise calculations.

Positions of Responsibility

Teaching Assistant | CS101 *(Jan'24 – May'24)*

- Facilitated **weekly lab sessions**, offering individual support and resolving questions for a group of **24** students.
- Organized and conducted a **problem-solving lecture** for **350** students aimed to assist in examination preparation.
- Assisted the professor in administrative matters including paper grading, exam proctoring, and course logistics.

Relevant Courses

Electrical Engineering	Analog Circuits, Power Engineering, Electronic Devices, Control Systems, EM Waves*
Signal Processing	Signal Processing – I, Probability & Random Processes, Communication Systems*
Computer Science	Data Structures & Algorithms, Operating Systems*, Logic for Computer Science
Computer Architecture	Microprocessors, Digital Systems

**Ongoing courses*

Technical Skills

Programming Languages	C, C++, Python, Java, VHDL, Embedded C, Assembly, MATLAB, Mathematica
Python Libraries	Numpy, Pandas, Matplotlib, SciPy, SciKit-Learn, z3-solver, skimage, PyTorch
Software	Cadence, Intel Quartus, μVision Kiel, LTSpice, VSCode, Git, Jupyter, AutoCAD

Extra Curriculars

Managerial

- Participated in the organizing committee of **'Zenith'**, an inter-school fest. *(Nov'20)*
- Showcased **leadership** and **project management** skills by heading **Tech Team**.
- Managed the online **digital transformation** using **automation** to increase efficiency.
- Developed Python scripts to automate email dispatch and generation of certificates.

Sports

- Selected in **NSO Chess Team**, IIT Bombay and completed a one academic year long chess training under an **International Master (IM)**. *(Oct'22 – Mar'23)*
- Avid chess player, participated in multiple tournaments representing my school.
- Enthusiastic **tennis** player, participated in multiple **regional tournaments**.