Pursuing **Minor** in **Computer Science and Engineering**

Scholastic Achievements

- Secured **All India Rank 338** in **JEE (Advanced)** among 1,40,000+ students (2021)
- Achieved **All India Rank 124** in **JEE (Main)** among 9,00,000+ students (2021)
- Secured **All India Rank 82** in **KVPY 2021 - SX Stream**, held by **IISC, Banglore** (2021)
- Recipient of the prestigious **NTSE Scholarship** by **NCERT, Government of India** (2019)

Olympiads & Competitions

- Among the **National** Top **1%** in Indian Olympiad Qualifier in Chemistry (IOQC) (2021)
- Among the **State** Top **1%** in Indian Olympiad Qualifier in Astronomy (IOQA) (2021)
- Achieved **State Rank 3** in **State Scholarship Exam** conducted Govt.of Maharashtra (2017)
- Achieved **State Rank 6** for two years in **Maharashtra Talent Search Exam** (MTSE) (2019,2018)

Key Projects

Student Satellite Program IIT Bombay

A 70+member student team striving to make IIT Bombay a centre of excellence in space technology

- **CubeSat | Guidance and Navigation(GNC) Subsystem** (May '22 - Present)
  A Nanosatellite mission to be proposed to ISRO for launching into Low-Earth Orbit (LEO)
  - working on the **Multiplicative Extended Kalman Filter** (MEKF), which will be the estimator used on Cubesat and on the **QuEst** algorithm, used to find the initial attitude estimate
  - currently working on the **Estimator** block in **CLS** to optimize the **attitude** of the satellite
  - wrote and tested the code for **Extended Kalman Filter** for attitude estimation of a quadrotor
- **Kalman Filter | Learning Task** (Apr '22 - May '22)
  - learnt about Random vectors and processes, estimation techniques like **least square** estimation, Best Linear Unbiased Estimator**(BLUE)** and Minimum Variance Unbiased Estimator**(MVUE)**
  - studied about the **Kalman Filter Algorithm** and its derivation, and implemented the algorithm for estimating the position and velocity of an object undergoing oscillatory motion
- **Attitude Parametrization | Mini Project** (Mar '22)
  - studied about different types of methods to represent attitude of a satellite, like **Euler Angles**, **Rotation vector**, **Rotation matrix**, and **Quaternion** and their drawbacks, like **Gimbal Lock**
  - studied about the **Euler Rotation Theorem**, Motion in Rotating frames and **Transport theorem**, and numerical methods of Integration like **Runge-Kutta** (RK) methods
  - wrote and tested the code for interconversion between different parametrizations of attitude

Data Science Project

- **Real Estate Rent Prediction Model | DS Minor Project** (Autumn '22)
  Guide: Prof Amit Sethi
  - Scraped and collected data about factors affecting rent from various resources available on web
  - Analyzed different types of data using python libraries like **NumPy, Pandas, SciPy, Seaborn**
  - Performed EDA on factors like location, size, interior and predicting models using MLE parameters
  - Trained and tested machine learning models like **Linear, Lasso and Ridge Regression** on the data

VHDL Projects | Digital Systems Lab

Guide: Prof Maryam Shojaei

- **Sequence Detector** (Autumn' 22)
  - Designed a **Sequence Detector Meale Machine** which detected a **alphabetical sub sequence** inside a given sequence using **Behavioural Description**
- **Arithmetic and Logic Unit** (Autumn' 22)
  - Implemented a basic **Arithmetic and Logic unit**, using Behavioural Description
  - Verified the outputs of the implemented code using **Scanchain Mechanism on Xenon Board**
- **Sequence Generator** (Autumn' 22)
  - Designed a sequence generator **Finite State Machine** using sequential circuit elements like **Data(D) Flip Flops** in **Structural Modelling mechanism** and verified output on Xenon Board
- **Multiplier** (Autumn' 22)
  - Designed a 4x3 binary multiplier using Behavioural description and verified the outputs using Scanchain mechanism on Xenon board
- **Ripple Adder** (Autumn' 22)
  - designed a Ripple carry adder using Full Adders using Behavioural description

Implementing CPU in VHDL | EE 224 Course Project

Guide: Prof Virendra Singh

- Designed a **16 bit CPU** having 8 general purpose registers, based on given Instruction Set Architecture that contained 14 different instructions and used **point to point communication** infrastructure
- Simulated the working of the CPU and the **controller Finute State Machine** in VHDL

Bubble Trouble | Course Project (Autumn' 21)

CS101 course project | Prof Parag Chaudhari

- Enhanced an GUI based bubble shooting game with C++ using Simplecpp graphics
- Added a variety of features like splitting a bubble into multiple bubbles with varying speeds
- Implemented a Health counter of the shooter and a time counter using classes and strings
- Added levels and increased difficulty of each level in the game using **Object Oriented Programming**

Technical Skills

Languages	Python, MATLAB, SImulink, C++, VHDL, HTML
Libraries	Numpy, Scipy, Matplotlib, Pandas
Softwares	AutoCad, Quartus, Git, LaTeX

Key Courses Undertaken

Electrical Engineering	Control Systems*, Miccroprocessors*, Probability & Random Processes, Analog Circuits, Digital Circuits, Signal Processing
Programming	Data Structures and Algorithms*, Data Science, Computer Programming
Maths and Physics	Matrix Computations*, Differential Equations, Complex Analysis, Calculus, Linear Algebra, Quantum Physics, Electromagnetism

** to be completed by Spring 2023*

Extracurriculars

- Among the top Qaurtile students who participated in the **Simon Marais Maths Competetion** (2022)
- Built a **Ultrasonic Radar Detection System** using **Arduino micro controller** (2019)
- Actively engaged in **Competitive Programming** and currently a **2 star coder** on **Codechef**
- Secured **Rank 5** in Chess Tournament **Freshie Rapid Open**, organised by IIT Bombay (June '22)
- Underwent excessive training in **Chess** under by **National Sports Organisation** (2021)
- Participated in **All India Open University Chess Tournament** under **Avahan IIT Bombay**
- Participated in **All India Chess League** 3.0 and 4.0 in which IIT Bombay bagged **1st** position in both the years in which all major Indian Universities participated