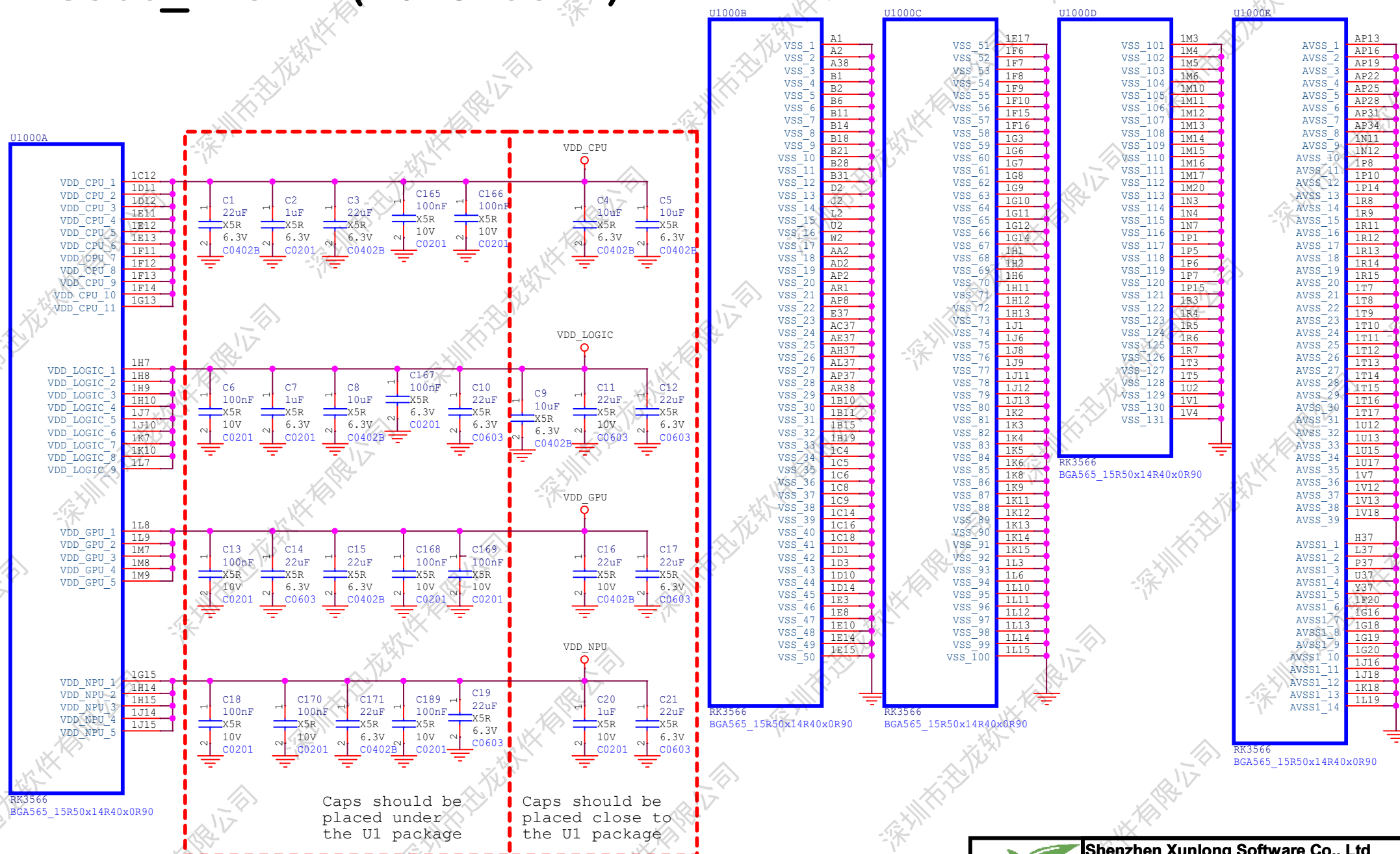


## RK3566 ABCDE (Power&GND)



**Shenzhen Xunlong Software Co., Ltd**

<b>Project:</b>	<b>OPI 3B</b>
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<b>File:</b>	<b>01.RK3566 Power/GND</b>
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<b>Date:</b>	<b>Monday, May 27, 2024</b>	<b>Rev:</b>	<b>V2.1</b>
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<b>Size:</b>	<b>A3</b>	<b>Sheet:</b>	<b>0</b>	<b>Of:</b>	<b>0</b>
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# RK3566\_F (DDR PHY)

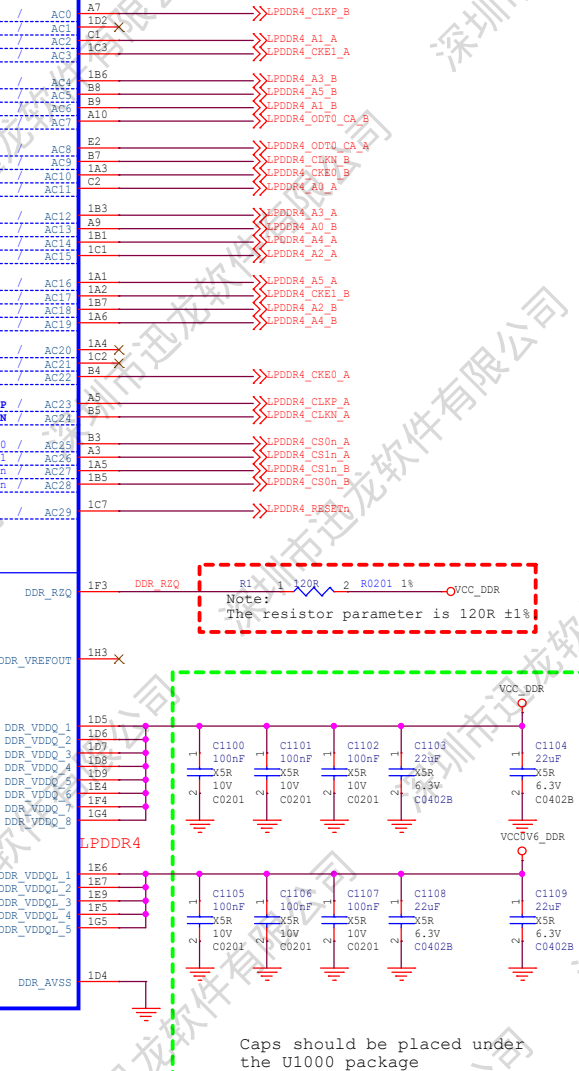
U1000F

	DDR4	LPDDR4	DDR3	LPDDR3		DDR4	LPDDR4	DDR3	LPDDR3	
LPDDR4 DQ0_A <<>	G2	DDR DQ0_A / DDR4 DQ0_A / LPDDR4 DQ0_A / DDR3 DQ0 / LPDDR3 DQ05				DDR4 A0 / LPDDR4 CLKP_B / DDR3 A9 / --- / AC0				A7 >>> LPDDR4 CLKP_B
LPDDR4 DQ1_A <<>	F1	DDR DQ1_A / DDR4 DQ1_A / LPDDR4 DQ1_A / DDR3 DQ1 / LPDDR3 DQ14				DDR4 A1 / LPDDR4 CLKP_A / DDR3 A2 / --- / AC1				D1 >>> LPDDR4 A1_A
LPDDR4 DQ2_A <<>	E1	DDR DQ2_A / DDR4 DQ2_A / LPDDR4 DQ2_A / DDR3 DQ2 / LPDDR3 DQ19				DDR4 A2 / LPDDR4 CLKP_A / DDR3 A4 / LPDDR3 A6 / --- / AC2				IC3 >>> LPDDR4 CEK1_A
LPDDR4 DQ3_A <<>	M2	DDR DQ3_A / DDR4 DQ3_A / LPDDR4 DQ3_A / DDR3 DQ3 / LPDDR3 DQ18				DDR4 A3 / LPDDR4 CLKP_A / DDR3 A5 / LPDDR3 A7 / --- / AC3				IB6 >>> LPDDR4 A3_B
LPDDR4 DQ4_A <<>	K1	DDR DQ4_A / DDR4 DQ4_A / LPDDR4 DQ4_A / DDR3 DQ4 / LPDDR3 DQ12				DDR4 A4 / LPDDR4 A3_B / DDR3 BA1 / LPDDR3 A3 / --- / AC4				B8 >>> LPDDR4 A5_B
LPDDR4 DQ5_A <<>	K2	DDR DQ5_A / DDR4 DQ5_A / LPDDR4 DQ5_A / DDR3 DQ5 / LPDDR3 DQ8				DDR4 A5 / LPDDR4 A5_B / DDR3 A11 / LPDDR3 A2 / --- / AC5				B9 >>> LPDDR4 A1_B
LPDDR4 DQ6_A <<>	J1	DDR DQ6_A / DDR4 DQ6_A / LPDDR4 DQ6_A / DDR3 DQ6 / LPDDR3 DQ11				DDR4 A6 / LPDDR4 A1_B / DDR3 A13 / LPDDR3 A1 / --- / AC6				A10 >>> LPDDR4 OD70_CA_B
LPDDR4 DQ7_A <<>	J2	DDR DQ7_A / DDR4 DQ7_A / LPDDR4 DQ7_A / DDR3 DQ7 / LPDDR3 DQ11				DDR4 A7 / LPDDR4 OD70_CA_B / DDR3 A8 / --- / AC7				
LPDDR4 DM0_A <<>	H2	DDR DM0_A / DDR4 DM1_A / LPDDR4 DM0_A / DDR3 DM0 / LPDDR3 DM1				DDR4 A8 / LPDDR4 OD70_CA_A / DDR3 A6 / LPDDR3 A5 / --- / AC8				E2 >>> LPDDR4 OD70_CA_A
LPDDR4 DQS0P_A <<>	H1	DDR DQS0P_A / DDR4 DQSL_P_A / LPDDR4 DQS0P_A / DDR3 DQS0P / LPDDR3 DQS1P				DDR4 A9 / LPDDR4 CLKP_B / DDR3 A5 / --- / AC9				B7 >>> LPDDR4 CKEN_B
LPDDR4 DQS0N_A <<>	H1	DDR DQS0N_A / DDR4 DQSL_N_A / LPDDR4 DQS0N_A / DDR3 DQS0N / LPDDR3 DQS1N				DDR4 A10 / LPDDR4 CKEO_B / DDR3 A10 / --- / AC10				IA3 >>> LPDDR4 CKEO_B
						DDR4 A11 / LPDDR4 A0_A / DDR3 A7 / LPDDR3 A6 / --- / AC11				C2 >>> LPDDR4 A0_A
LPDDR4 DQ8_A <<>	P2	DDR DQ8_A / DDR4 DQ3_A / LPDDR4 DQ8_A / DDR3 DQ8 / LPDDR3 DQ25				DDR4 A12 / LPDDR4 A3_A / DDR3 BA2 / --- / AC12				IB3 >>> LPDDR4 A3_A
LPDDR4 DQ9_A <<>	R1	DDR DQ9_A / DDR4 DQ01_A / LPDDR4 DQ9_A / DDR3 DQ9 / LPDDR3 DQ24				DDR4 A13 / LPDDR4 A0_B / DDR3 A17 / LPDDR3 A0 / --- / AC13				A9 >>> LPDDR4 A0_B
LPDDR4 DQ10_A <<>	R2	DDR DQ10_A / DDR4 DQ07_A / LPDDR4 DQ10_A / DDR3 DQ10 / LPDDR3 DQ28				DDR4 A14 / LPDDR4 A1_A / DDR3 A15 / LPDDR3 A1 / --- / AC14				IB1 >>> LPDDR4 A4_A
LPDDR4 DQ11_A <<>	T2	DDR DQ11_A / DDR4 DQ05_A / LPDDR4 DQ11_A / DDR3 DQ11 / LPDDR3 DQ29				DDR4 A15 / LPDDR4 A2_A / DDR3 A0 / --- / AC15				IC1 >>> LPDDR4 A2_A
LPDDR4 DQ12_A <<>	M1	DDR DQ12_A / DDR4 DQ02_A / LPDDR4 DQ12_A / DDR3 DQ12 / LPDDR3 DQ26								
LPDDR4 DQ13_A <<>	J2	DDR DQ13_A / DDR4 DQ09_A / LPDDR4 DQ13_A / DDR3 DQ13 / LPDDR3 DQ31				DDR4 A16 / RASn / LPDDR4 A5_A / DDR3 RASn / LPDDR3 A7 / --- / AC16				IA1 >>> LPDDR4 A5_A
LPDDR4 DQ14_A <<>	J1	DDR DQ14_A / DDR4 DQ06_A / LPDDR4 DQ14_A / DDR3 DQ14 / LPDDR3 DQ30				DDR4 A17 / LPDDR4 CKE1_B / DDR3 CASn / --- / AC17				IA2 >>> LPDDR4 CKE1_B
LPDDR4 DQ15_A <<>	J2	DDR DQ15_A / DDR4 DQ03_A / LPDDR4 DQ15_A / DDR3 DQ15 / LPDDR3 DQ34				DDR4 A18 / LPDDR4 A4_B / DDR3 A12 / LPDDR3 A4 / --- / AC18				IB7 >>> LPDDR4 A2_B
LPDDR4 DM1_A <<>	I1	DDR DM1_A / DDR4 DMU_A / LPDDR4 DM1_A / DDR3 DM1 / LPDDR3 DM3								IA6 >>> LPDDR4 A4_B
LPDDR4 DQS1P_A <<>	N1	DDR DQS1P_A / DDR4 DQSU_P_A / LPDDR4 DQS1P_A / DDR3 DQS1P / LPDDR3 DQS3P				DDR4 B0 / LPDDR4 OD71_CA_B / DDR3 WEH / --- / AC20				IA4 >>> LPDDR4 CKEO_A
LPDDR4 DQS1N_A <<>	N2	DDR DQS1N_A / DDR4 DQSU_N_A / LPDDR4 DQS1N_A / DDR3 DQS1N / LPDDR3 DQS3N				DDR4 B1 / LPDDR4 OD71_CA_A / DDR3 BA0 / --- / AC21				IC2 >>> LPDDR4 CKEO_A
						DDR4 CKE / LPDDR4 CKEO_A / DDR3 CKE / LPDDR3 CKE / --- / AC22				B4 >>> LPDDR4 CKEO_A
LPDDR4 DQ0_B <<>	B12	DDR DQ0_B / DDR4 DQ07_B / LPDDR4 DQ0_B / DDR3 DQ16 / LPDDR3 DQ1				DDR4 CLKP / LPDDR4 CLKP_A / DDR3 CLKP / LPDDR3 CLKP / --- / AC23				A5 >>> LPDDR4 CLKP_A
LPDDR4 DQ1_B <<>	B10	DDR DQ1_B / DDR4 DQ05_B / LPDDR4 DQ1_B / DDR3 DQ17 / LPDDR3 DQ5				DDR4 CLKN / LPDDR4 CLKN_A / DDR3 CLKN / LPDDR3 CLKN / --- / AC24				B5 >>> LPDDR4 CLKN_A
LPDDR4 DQ2_B <<>	IA9	DDR DQ2_B / DDR4 DQ03_B / LPDDR4 DQ2_B / DDR3 DQ18 / LPDDR3 DQ4								
LPDDR4 DQ3_B <<>	IA7	DDR DQ3_B / DDR4 DQ00_B / LPDDR4 DQ3_B / DDR3 DQ19 / LPDDR3 DQ4				DDR4 CS0n / LPDDR4 CS1n_A / DDR3 CS1n / LPDDR3 CS1n / --- / AC25				B3 >>> LPDDR4 CS0n_A
LPDDR4 DQ4_B <<>	IA10	DDR DQ4_B / DDR4 DQ01_B / LPDDR4 DQ4_B / DDR3 DQ20 / LPDDR3 DQ2				DDR4 CS1n / LPDDR4 CS1n_B / DDR3 CS1n / LPDDR3 CS1n / --- / AC26				A3 >>> LPDDR4 CS1n_A
LPDDR4 DQ5_B <<>	IB9	DDR DQ5_B / DDR4 DQ02_B / LPDDR4 DQ5_B / DDR3 DQ21 / LPDDR3 DQ3				DDR4 CS0n / LPDDR4 CS1n_B / DDR3 CS0n / LPDDR3 CS1n / --- / AC27				IB5 >>> LPDDR4 CS1n_B
LPDDR4 DQ6_B <<>	IA9	DDR DQ6_B / DDR4 DQ02_B / LPDDR4 DQ6_B / DDR3 DQ22 / LPDDR3 DQ3				DDR4 CS1n / LPDDR4 CS1n_B / DDR3 CS1n / LPDDR3 CS1n / --- / AC28				IB8 >>> LPDDR4 CS0n_B
LPDDR4 DM0_B <<>	IB8	DDR DM0_B / DDR4 DMU_B / LPDDR4 DM0_B / DDR3 DM2 / LPDDR3 DM0				DDR4 RESETn / LPDDR4 RESETn / DDR3 RESETn / --- / AC29				IC7 >>> LPDDR4 RESETn
LPDDR4 DQS0P_B <<>	A13	DDR DQS0P_B / DDR4 DQSU_P_B / LPDDR4 DQS0P_B / DDR3 DQS2P / LPDDR3 DQS0P								
LPDDR4 DQS0N_B <<>	A12	DDR DQS0N_B / DDR4 DQSU_N_B / LPDDR4 DQS0N_B / DDR3 DQS2N / LPDDR3 DQS0N								
LPDDR4 DQ8_B <<>	B19	DDR DQ8_B / DDR4 DQ10_B / LPDDR4 DQ8_B / DDR3 DQ24 / LPDDR3 DQ18 DZ								
LPDDR4 DQ9_B <<>	A19	DDR DQ9_B / DDR4 DQ12_B / LPDDR4 DQ9_B / DDR3 DQ25 / LPDDR3 DQ19 D3								
LPDDR4 DQ10_B <<>	A20	DDR DQ10_B / DDR4 DQ14_B / LPDDR4 DQ10_B / DDR3 DQ26 / LPDDR3 DQ22 D6								
LPDDR4 DQ11_B <<>	B20	DDR DQ11_B / DDR4 DQ11_B / LPDDR4 DQ11_B / DDR3 DQ27 / LPDDR3 DQ28 D7								
LPDDR4 DQ12_B <<>	A15	DDR DQ12_B / DDR4 DQ07_B / LPDDR4 DQ12_B / DDR3 DQ28 / LPDDR3 DQ31								
LPDDR4 DQ13_B <<>	B15	DDR DQ13_B / DDR4 DQ04_B / LPDDR4 DQ13_B / DDR3 DQ29 / LPDDR3 DQ34								
LPDDR4 DQ14_B <<>	IC10	DDR DQ14_B / DDR4 DQ01_B / LPDDR4 DQ14_B / DDR3 DQ30 / LPDDR3 DQ20 D1								
LPDDR4 DQ15_B <<>	B16	DDR DQ15_B / DDR4 DQ03_B / LPDDR4 DQ15_B / DDR3 DQ31 / LPDDR3 DQ21 D5								
LPDDR4 DM1_B <<>	IA11	DDR DM1_B / DDR4 DMU_B / LPDDR4 DM1_B / DDR3 DM3 / LPDDR3 DM2								
LPDDR4 DQS1P_B <<>	A17	DDR DQS1P_B / DDR4 DQSL_P_B / LPDDR4 DQS1P_B / DDR3 DQ32P / LPDDR3 DQS2P								
LPDDR4 DQS1N_B <<>	B17	DDR DQS1N_B / DDR4 DQSL_N_B / LPDDR4 DQS1N_B / DDR3 DQ32N / LPDDR3 DQS2N								

Note:  
Except DDR3, other DQ sequences  
can not be swap

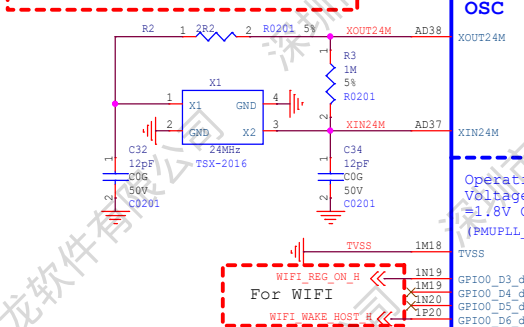
	VDDQ	VDDQL
DDR3L	1.35V	1.35V
DDR3	1.50V	1.50V
DDR4	1.20V	1.20V
LPDDR3	1.20V	1.20V
LPDDR4	1.10V	1.10V
LPDDR4X	1.10V	0.60V

Note: Sequences can not be swap

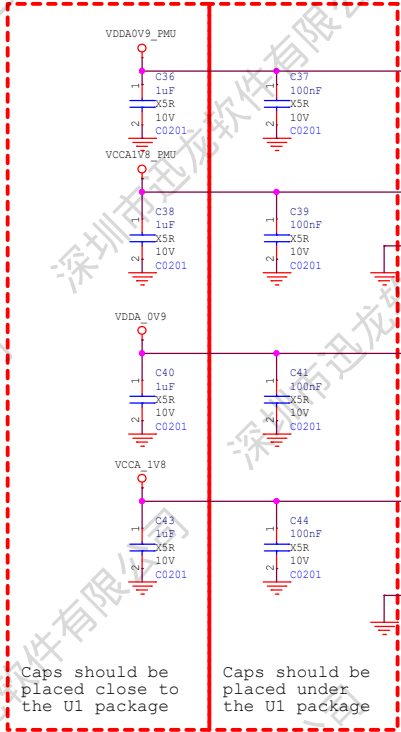


RK3566\_G (OSC/PLL/PMUIO1/2)

Adjust the load capacitor according to the crystal spec.



For WIFI  
WIFI\_REG\_ON\_H  
WIFI\_WAKE\_HOST\_H



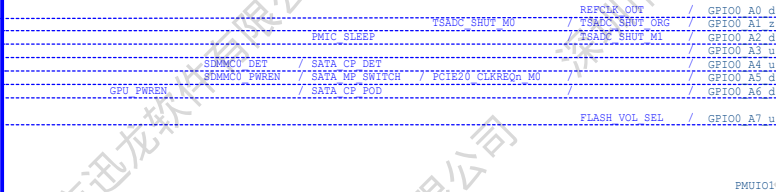
OSC  
XOUT24M  
XIN24M  
Operating Voltage = 1.8V Only (PMUPLL\_AVDD\_1V8)  
TVSS

PMU PLL  
PMUPLL\_AVDD\_OV9  
PMUPLL\_AVDD\_1V8  
PMUPLL\_AVSS

SYS PLL  
SYSPLL\_AVDD\_OV9  
SYSPLL\_AVDD\_1V8  
SYSPLL\_AVSS

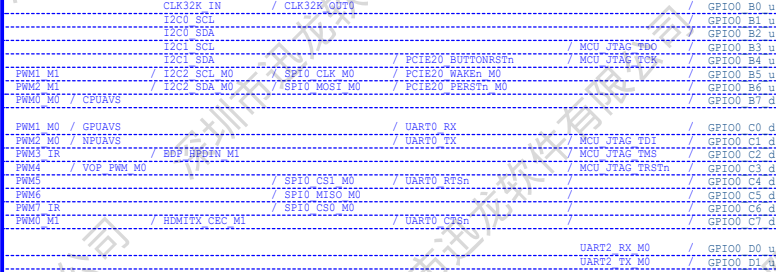
PMUIO1 Domain

Operating Voltage=3.3V Only



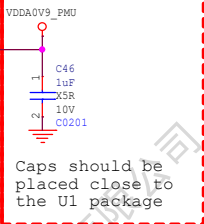
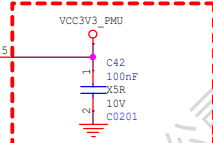
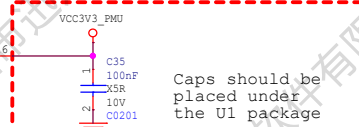
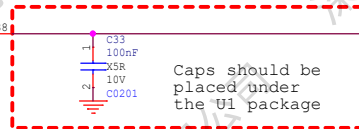
PMUIO2 Domain

Operating Voltage=1.8V/3.3V



PMUIO1/2/OSC Domain Logic Power

Operating Voltage=0.9V



Shenzhen Xunlong Software Co., Ltd				
Project:	OPI 3B			
File:	03.RK3566_OSC/PLL/PMUIO			
Date:	Monday, May 27, 2024			
Size:	A3	Sheet:	0	Of: 0
Rev:	V2.1			

# RK3566\_I (VCCIO2 Domain)

U1000I

## VCCIO2 Domain

Operating Voltage=1.8V/3.3V

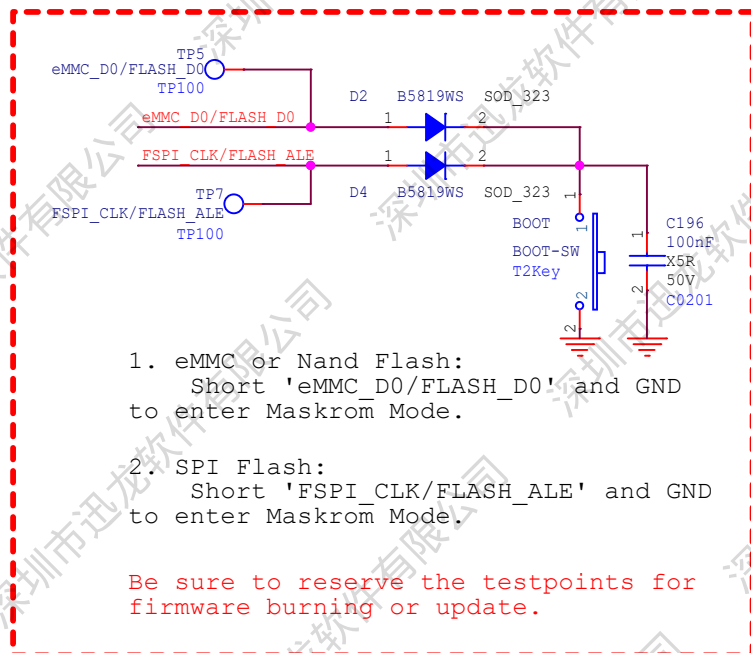
EMMC D0	/ FLASH D0	/ GPIO1 B4 u	A32	<<>	>>eMMC D0/FLASH D0
EMMC D1	/ FLASH D1	/ GPIO1 B5 u	B27	<<>	>>eMMC D1/FLASH D1
EMMC D2	/ FLASH D2	/ GPIO1 B6 u	B32	<<>	>>eMMC D2/FLASH D2
EMMC D3	/ FLASH D3	/ GPIO1 B7 u	B29	<<>	>>eMMC D3/FLASH D3
EMMC D4	/ FLASH D4	/ GPIO1 C0 u	B33	<<>	>>eMMC D4/FLASH D4
EMMC D5	/ FLASH D5	/ GPIO1 C1 u	A30	<<>	>>eMMC D5/FLASH D5
EMMC D6	/ FLASH D6	/ GPIO1 C2 u	B30	<<>	>>eMMC D6/FLASH D6
EMMC D7	/ FLASH D7	/ GPIO1 C3 u	A33	<<>	>>eMMC D7/FLASH D7
EMMC CMD	/ FLASH WRn	/ GPIO1 C4 u	A27	<<>	>>eMMC_CMD/FLASH_WRn
EMMC CLKOUT	/ FLASH DQS	/ GPIO1 C5 d	A29	<<>	>>eMMC_CLKOUT/FLASH_DQS
EMMC DATA STROBE	/ FSPI CS1n	/ FLASH CLE	1A16	<<>	>>eMMC_DATA_STROBE/FLASH_CLE
EMMC RSTn	/ FSPI D2	/ FLASH WPh	1B16	<<>	>>eMMC_RSTn/FSPI D2/FLASH WPh
FSPI CLK	/ FLASH ALE	/ GPIO1 D0 d	1A15	<<>	>>FSPI_CLK/FLASH ALE
FSPI D0	/ FLASH RDY	/ GPIO1 D1 u	1A17	<<>	>>FSPI_D0/FLASH RDY
FSPI D1	/ FLASH Rdn	/ GPIO1 D2 u	1A18	<<>	>>FSPI D1/FLASH Rdn
FSPI CS0n	/ FLASH CS0n	/ GPIO1 D3 u	1B17	<<>	>>FSPI_CS0n/FLASH CS0n
FSPI D3	/ FLASH CS1n	/ GPIO1 D4 u	1C15	<<>	>>FSPI_D3/FLASH CS1n

Default is determined by Pin  
FLASH VOL\_SEL/GPIO0 A7 u:  
L:VCCIO2 must supply 3.3V  
H:VCCIO2 must supply 1.8V

RK3566  
BGA565 15R50x14R40x0R90

VCCIO2

1.8V  
Caps should be placed under the U1 package



1. eMMC or Nand Flash:  
Short 'eMMC\_D0/FLASH\_D0' and GND to enter Maskrom Mode.
2. SPI Flash:  
Short 'FSPI\_CLK/FLASH\_ALE' and GND to enter Maskrom Mode.

Be sure to reserve the testpoints for firmware burning or update.

Check the software configuration (dts) of voltage level, which must be keep the same as hardware design.

# RK3566\_J (VCCIO3 Domain)

U1000J

## VCCIO3 Domain

Operating Voltage=1.8V/3.3V

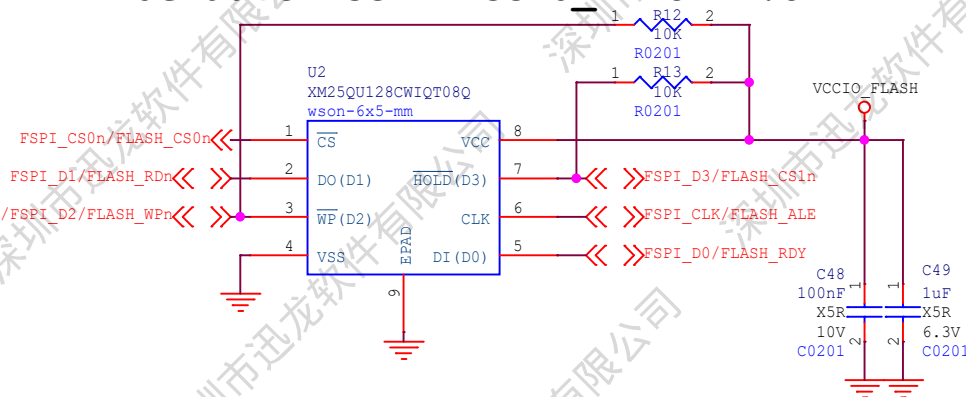
PWM8 M1	/ SDMMC0 D0	/ UART2 TX M1	/ UART6 TX M1	/ GPIO1 D5 u	1E20	<<>	>>SDMMC0_D0
PWM9 M1	/ SDMMC0 D1	/ UART2 RX M1	/ UART6 RX M1	/ GPIO1 D6 u	1F19	<<>	>>SDMMC0_D1
SDMMC0 D2	/ ARM JTAG TCK	/ UART5 CTSH M0	/ GPIO1 D7 u	1D20	<<>	>>SDMMC0_D2	
SDMMC0 D3	/ ARM JTAG TMS	/ UART5 RSTn M0	/ GPIO2 A0 u	1F18	<<>	>>SDMMC0_D3	
PWM10 M1	/ SDMMC0 CMD	/ UART5 RX M0	/ GPIO2 A1 u	1E19	<<>	>>SDMMC0_CMD	
SDMMC0 CLK	/ TEST CLKOUT	/ UART5 TX M0	/ GPIO2 A2 d	G38 R23 0R	R0201	<<>	>>SDMMC0_CLK

RK3566  
BGA565 15R50x14R40x0R90

VCCIO3

1.8V  
Caps should be placed under the U1 package

default VCC = VCCIO\_FLASH 1.8V



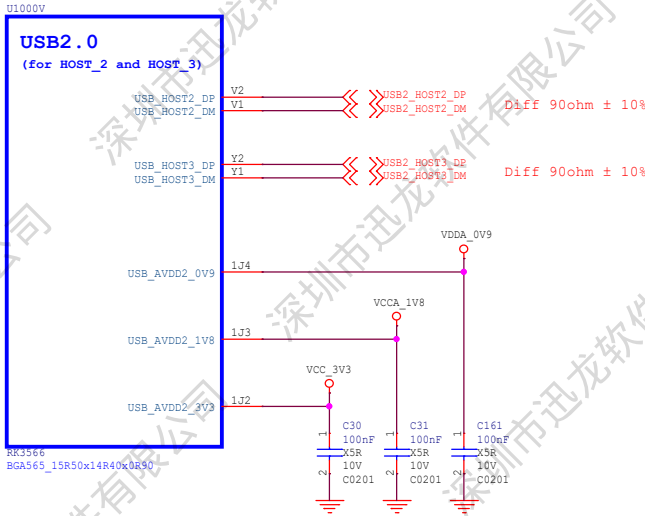
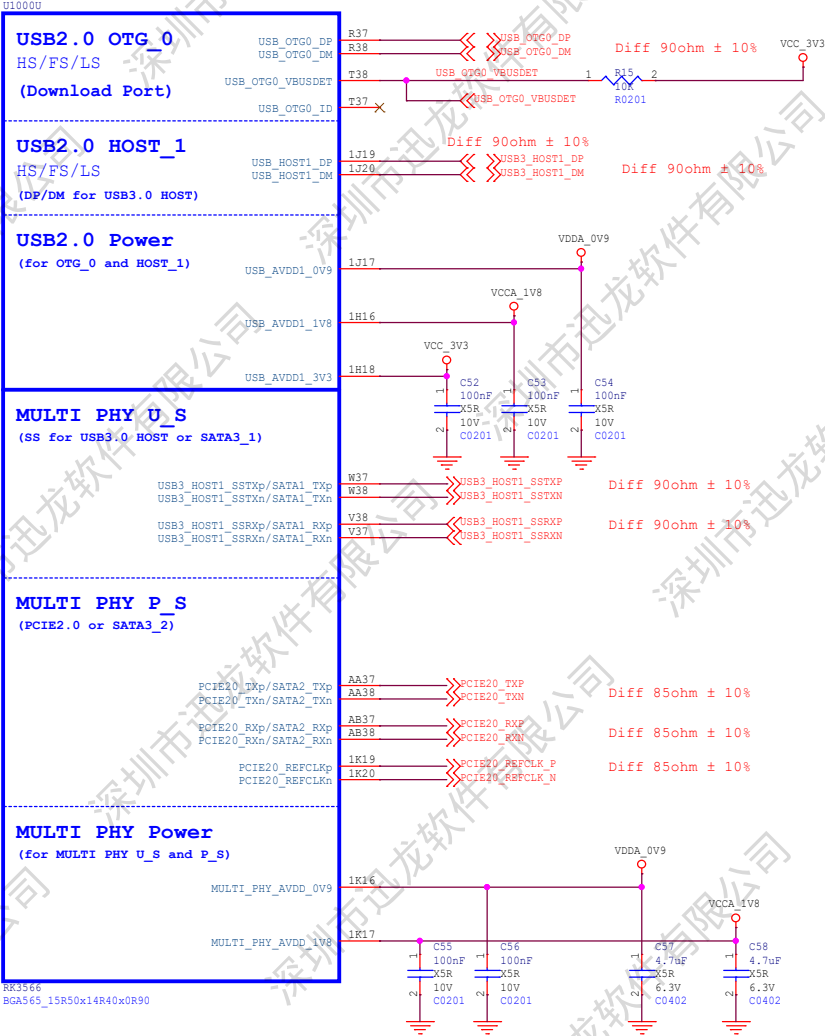
Shenzhen Xunlong Software Co., Ltd

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Date:	Monday, May 27, 2024
Size:	A3
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Rev:	V2.1
Of:	0



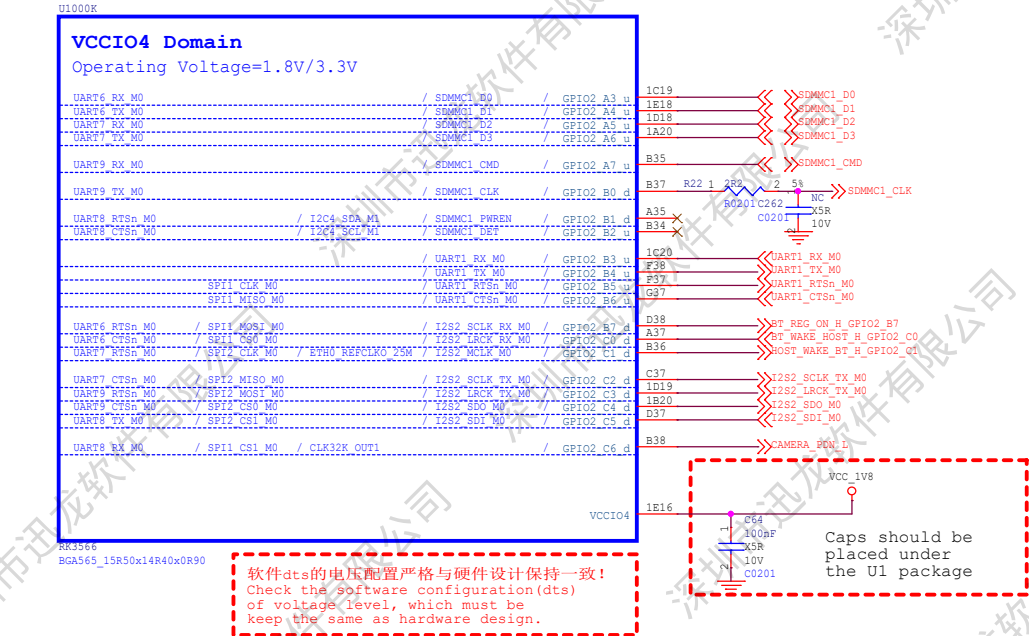
RK3566\_U (USB3.0/PCIe2.0x1/SATA)

RK3566\_V (USB2.0 HOST)

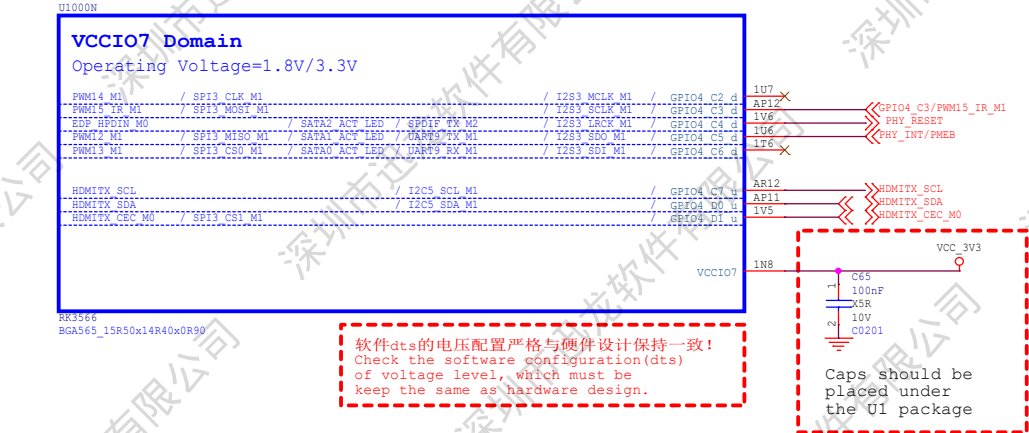


Shenzhen Xunlong Software Co., Ltd			
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File:	05.RK3566_USB/PCIe/SATA_PHY		
Date:	Monday, May 27, 2024	Rev:	V2.1
Size:	A3	Sheet:	0
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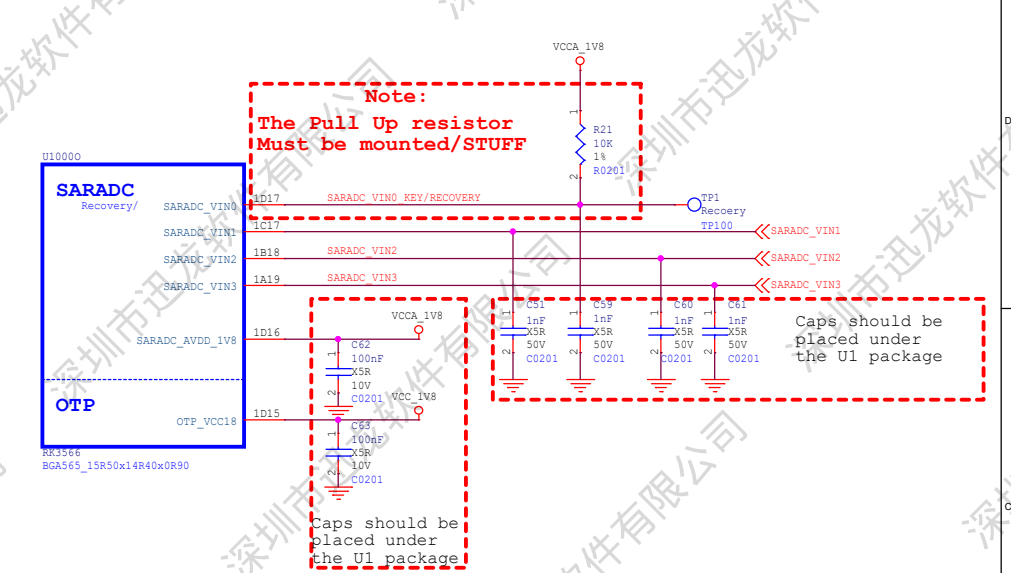
RK3566\_K (VCCIO4 Domain)



RK3566\_N (VCCIO7 Domain)

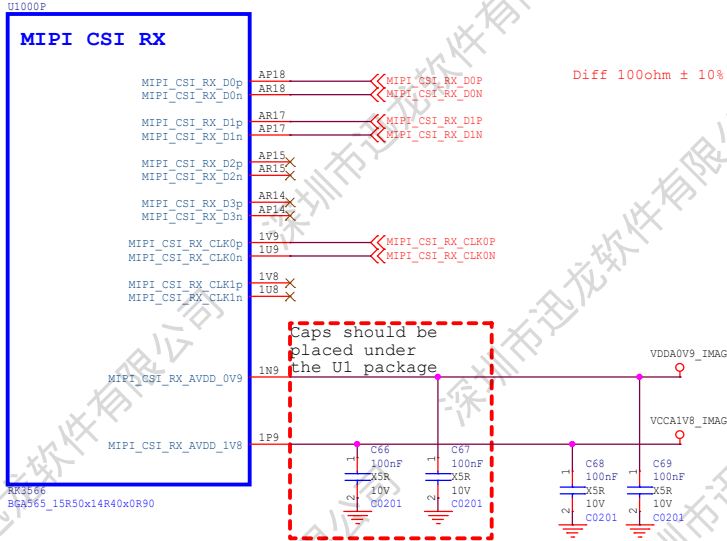


RK3566\_O (SARADC/OTP)



Shenzhen Xunlong Software Co., Ltd				
Project:	OPI 3B			
File:	06.RK3566_SARADC/GPIO			
Date:	Monday, May 27, 2024	Rev:	V2.1	
Size:	A3	Sheet:	0	Of: 0

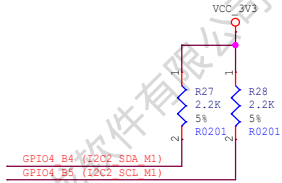
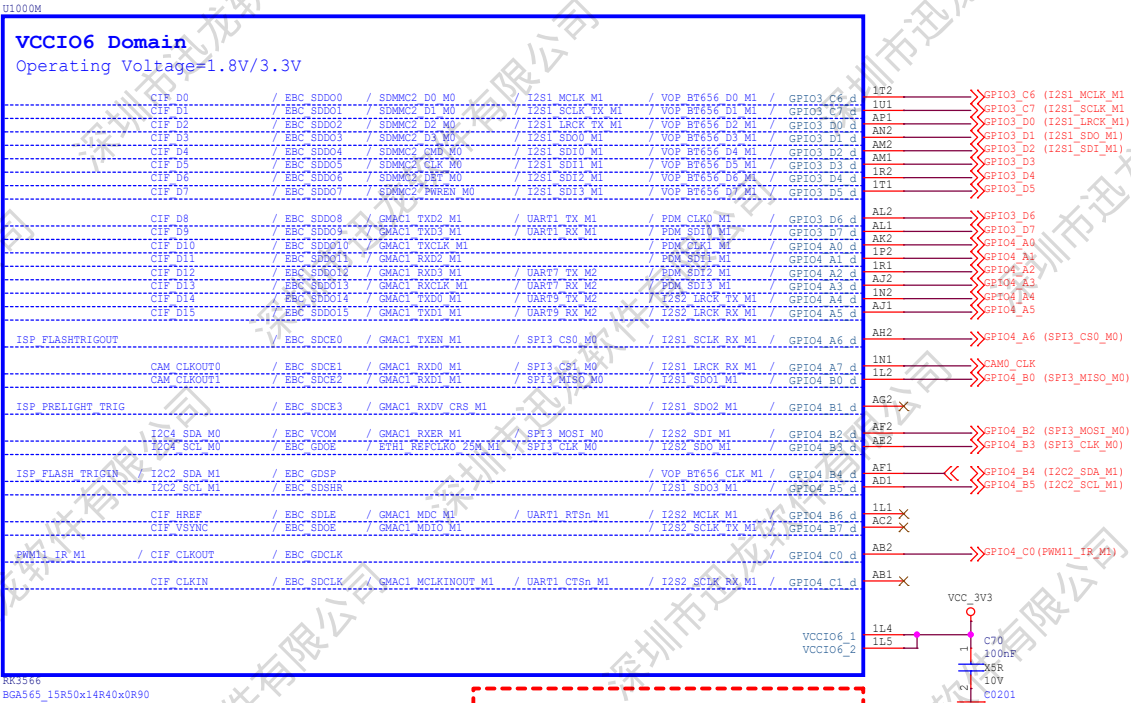
RK3566\_P (MIPI\_CSI\_RX)




**Usage of MIPI CSI Dx&CLKs**

Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane + Sensor2 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0 MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1

RK3566\_M (VCCIO6 Domain)

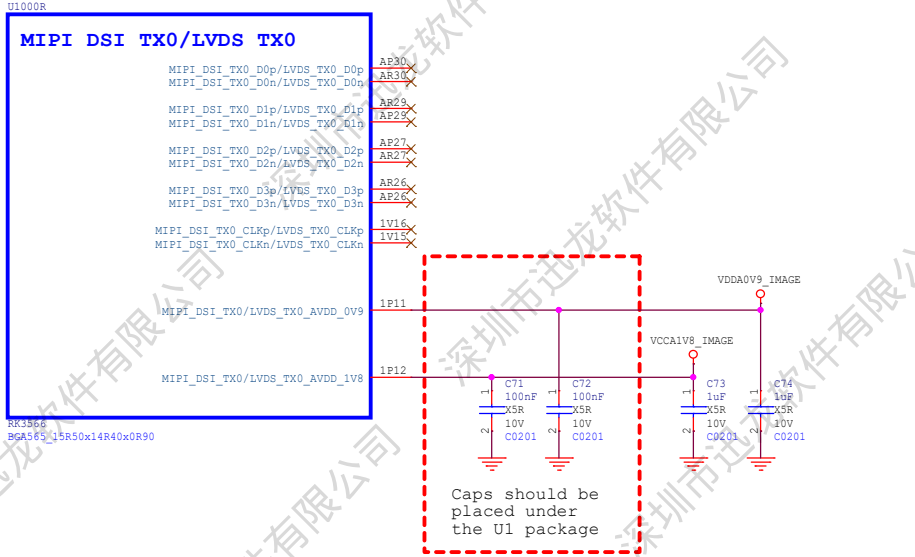


Check the software configuration(dts) of voltage level, which must be keep the same as hardware design.

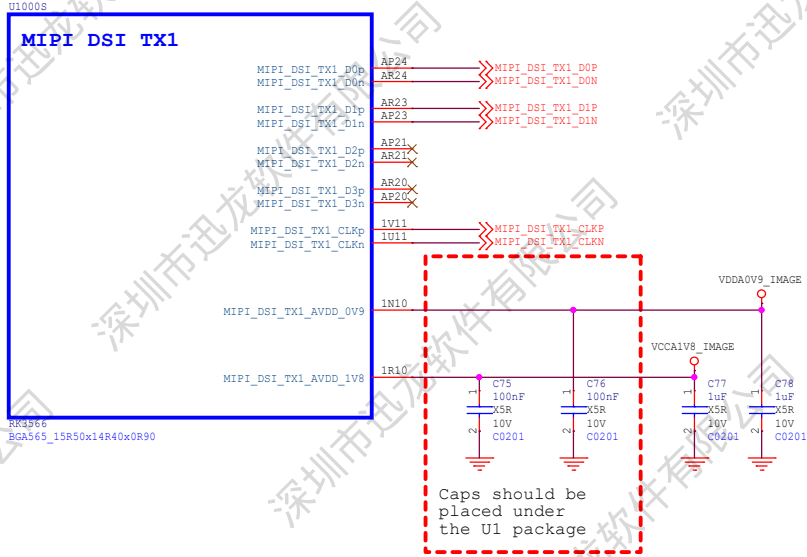
 **Shenzhen Xunlong Software Co., Ltd**

Project:	OPI 3B		
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Date:	Monday, May 27, 2024	Rev:	V2.1
Size:	A3	Sheet:	0
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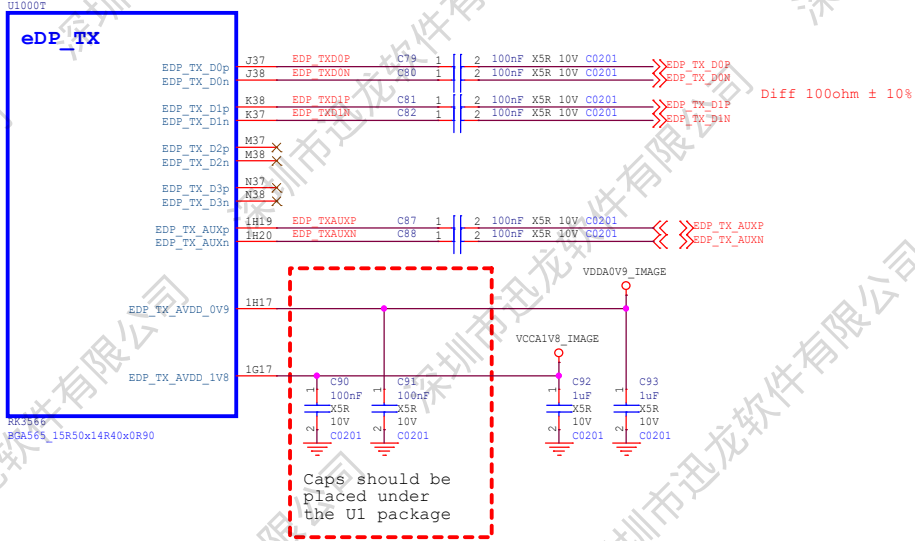
RK3566\_R(MIPI\_DSI\_TX0/LVDS\_TX0)



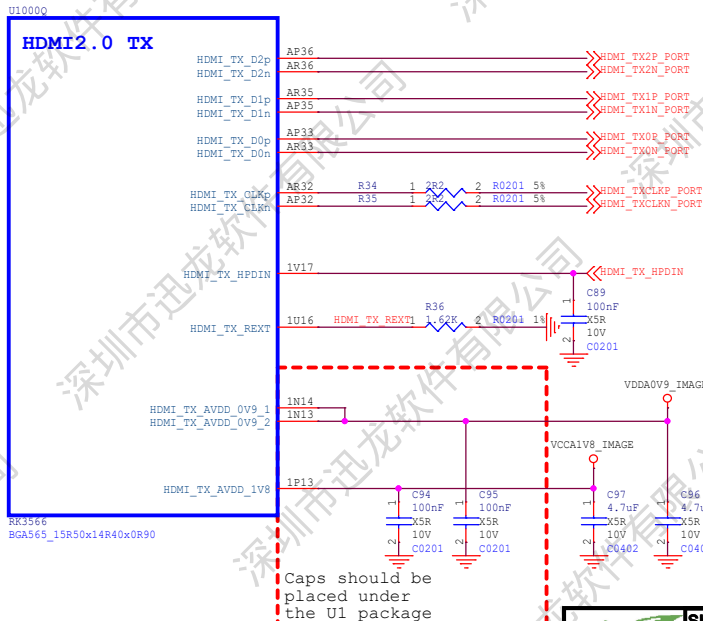
RK3566\_S(MIPI\_DSI\_TX1)



RK3566\_T(eDP TX)



RK3566\_Q(HDMI2.0 TX)



Shenzhen Xunlong Software Co., Ltd				
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Date:	Monday, May 27, 2024	Rev:	V2.1	
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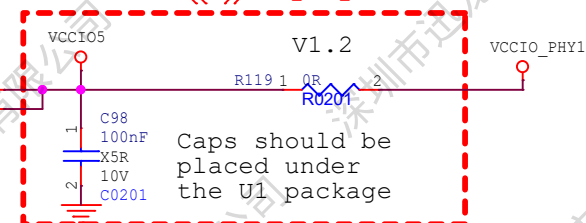
## U1000L

Operating Voltage=1.8V/3.3V

VOP BT1120 D0	/ SPI1 CS0 M1		/ SDMMC2 D0 M1	/ GPIO3 A1 d	IU5	
VOP BT1120 D1	/ GMAC1 TXD2 M0	/ I2S3 MCLK M0	/ SDMMC2 D1 M1	/ GPIO3 A2 d	AR10	
VOP BT1120 D2	/ GMAC1 TXD3 M0	/ I2S3 SCLK M0	/ SDMMC2 D2 M1	/ GPIO3 A3 d	AP10	>>>GMAC1_TXD2_M0
VOP BT1120 D3	/ GMAC1 RXD2 M0	/ I2S3 LRCK M0	/ SDMMC2 D3 M1	/ GPIO3 A4 d	AR9	>>>GMAC1_RXD2_M0
VOP BT1120 D4	/ GMAC1 RXD3 M0	/ I2S3 SDO M0	/ SDMMC2 CMD M1	/ GPIO3 A5 d	AP9	>>>GMAC1_RXD3_M0
VOP BT1120 CLK	/ GMAC1 TXCLK M0	/ I2S3 SDI M0	/ SDMMC2 CLK M1	/ GPIO3 A6 d	IU4	>>>GMAC1_TXCLK_M0
VOP BT1120 D5	/ GMAC1 RXCLK M0		/ SDMMC2 DET M1	/ GPIO3 A7 d	I1V3	>>>GMAC1_RXCLK_M0
VOP BT1120 D6	/ ETH1 REFCLK0 25M M0		/ SDMMC2 PWREN M1	/ GPIO3 B0 d	AR7	
PWM8 M0	/ VOP BT1120 D7	/ GMAC1 RXD0 M0	/ UART4 RX M1	/ GPIO3 B1 d	AP7	>>>GMAC1_RXD0_M0
PWM9 M0	/ VOP BT1120 D8	/ GMAC1 RXD1 M0	/ UART4 TX M1	/ GPIO3 B2 d	AR6	>>>GMAC1_RXD1_M0
VOP BT1120 D9	/ I2C5 SCL M0	/ GMAC1 RXDV CRS M0	/ PDM SDIO M2	/ GPIO3 B3 d	AP6	>>>GMAC1_RXDV_CRS_M0
VOP BT1120 D10	/ I2C5 SDA M0	/ GMAC1 RXER M0	/ PDM SDI1 M2	/ GPIO3 B4 d	IU3	
PWM10 M0	/ VOP BT1120 D11	/ I2C3 SCL M1	/ GMAC1 TXD0 M0	/ GPIO3 B5 d	I1T4	>>>GMAC1_TXD0_M0
PWM11 IR M0	/ VOP BT1120 D12	/ I2C3 SDA M1	/ GMAC1 TXD1 M0	/ GPIO3 B6 d	I1V2	>>>GMAC1_TXD1_M0
PWM12 M0		/ GMAC1 TXEN M0	/ UART3 TX M1	/ PDM SDI2 M2	AP5	>>>GMAC1_TXEN_M0
PWM13 M0		/ GMAC1 MCLKINOUT M0	/ UART3 RX M1	/ PDM SDI3 M2	AR4	>>>GMAC1_MCLKINOUT_M0
VOP BT1120 D13	/ SPI1 MOSI M1		/ PCIE20 PERSTn M1	/ I2S1 SDO2 M2	AP4	
VOP BT1120 D14	/ SPI1 MISO M1		/ UART5 TX M1	/ I2S1 SDO3 M2	AP3	
VOP BT1120 D15	/ SPI1 CLK M1		/ UART5 RX M1	/ I2S1 SCLK RX M2	AR2	
PWM14 M0	/ VOP PWM M1	/ GMAC1 MDC M0	/ UART7 TX M1	/ PDM CLK1 M2	GPIO3 C4 d	>>>GMAC1_MDC_M0
PWM15 IR M0	/ SPDIF TX M1	/ GMAC1 MDIO M0	/ UART7 RX M1	/ I2S1 LRCK RX M2	GPIO3 C5 d	>>>GMAC1_MDIO_M0

RK3566  
BGA565 15R50x14R40x0R90

Check the software configuration(dts) of voltage level, which must be keep the same as hardware design

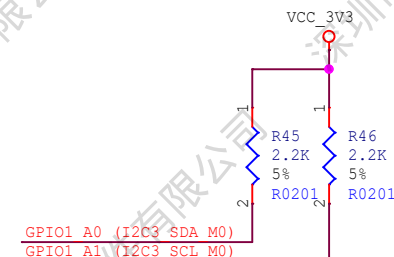


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## U1000H

Operating Voltage=1.8V/3.3V

A22	GPIO1_A0 (I2C3_SDA_M0)
B22	GPIO1_A1 (I2C3_SCL_M0)
A23	I2S1_MCLK_M0_PMIC
B23	I2S1_SCLK_TX_M0_PMIC
1A13	
B24	I2S1_LRCK_TX_M0_PMIC
1A14	PDM_CLK0_M0_PMIC
B25	I2S1_SDO0_M0_PMIC
1B13	PCIE20_CLKREQn_3V3_L
A26	PCIE20_WAKEn_3V3_L
B26	
1B14	I2S1_SDIO_M0/PDM_SDIO_M0_PMIC



GPIOD1	A0	(I2C3	SDA	M0
GPIOD1	A1	(I2C3	SCL	M0

VCCIO ACODEC

VCCIO ACODEC = 3.3V as default

Caps should be placed under the U1 package

Check the software configuration(dts) of voltage level, which must be keep the same as hardware design



**Shenzhen Xunlong Software Co., Ltd**

<b>Project:</b>	<b>OPI 3B</b>
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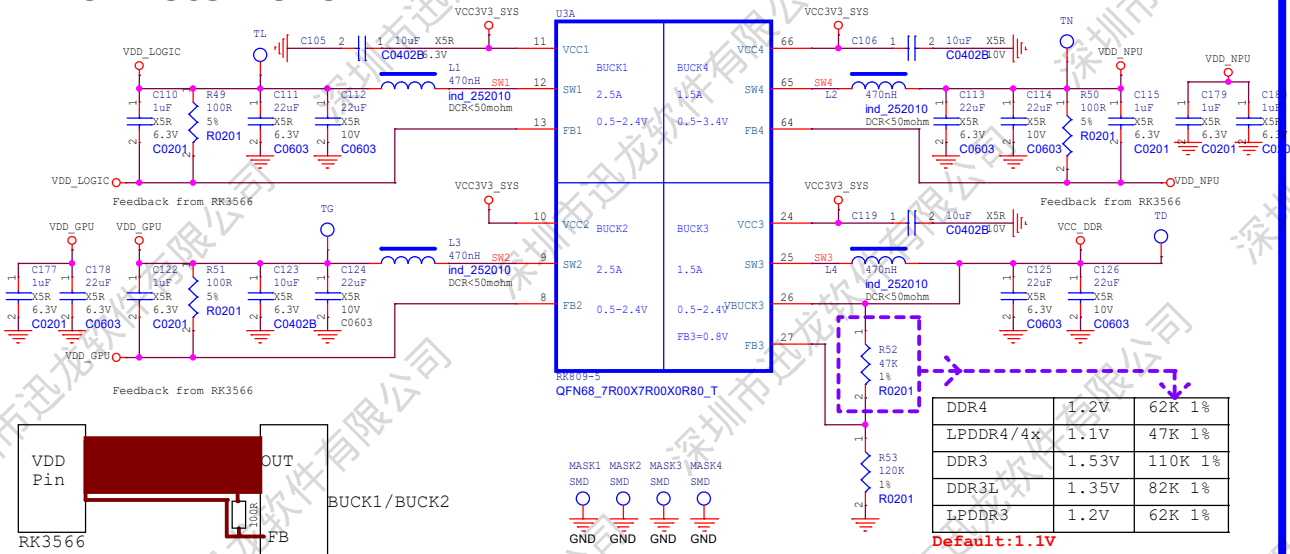
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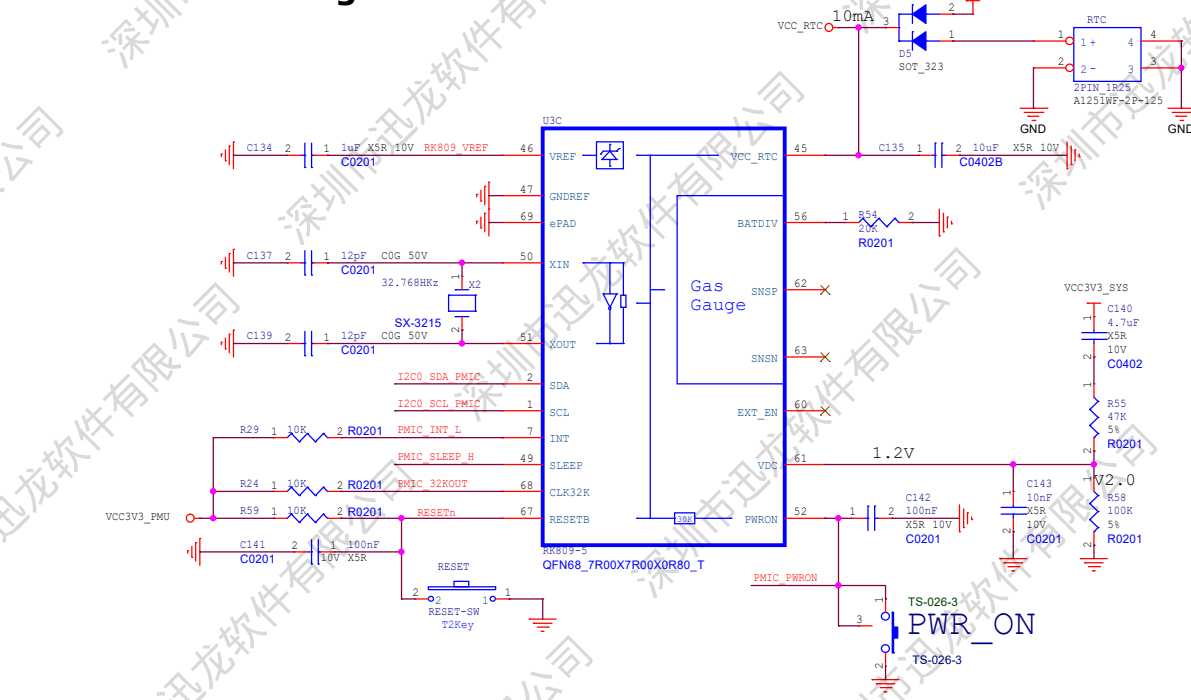
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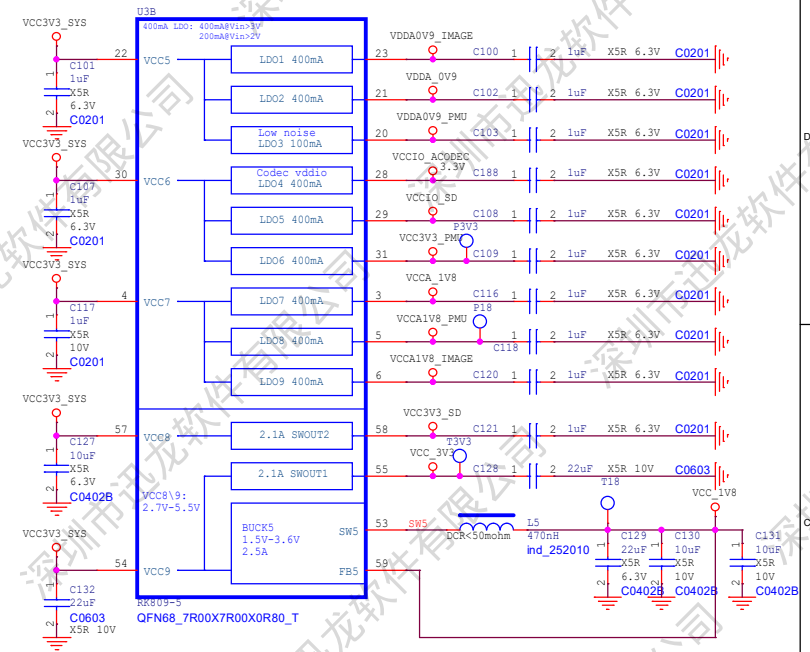
## PMIC RK809 DCDC



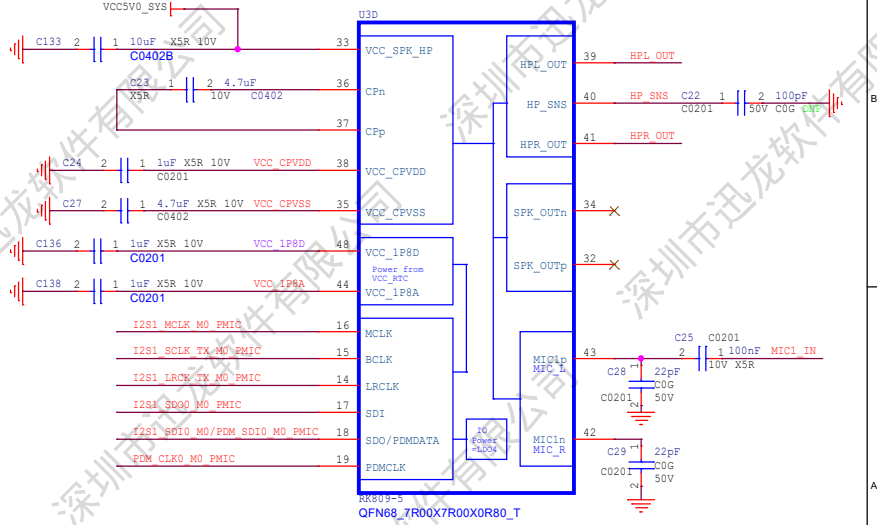
## PMIC RK809 Managerment



## PMIC RK809 LDO

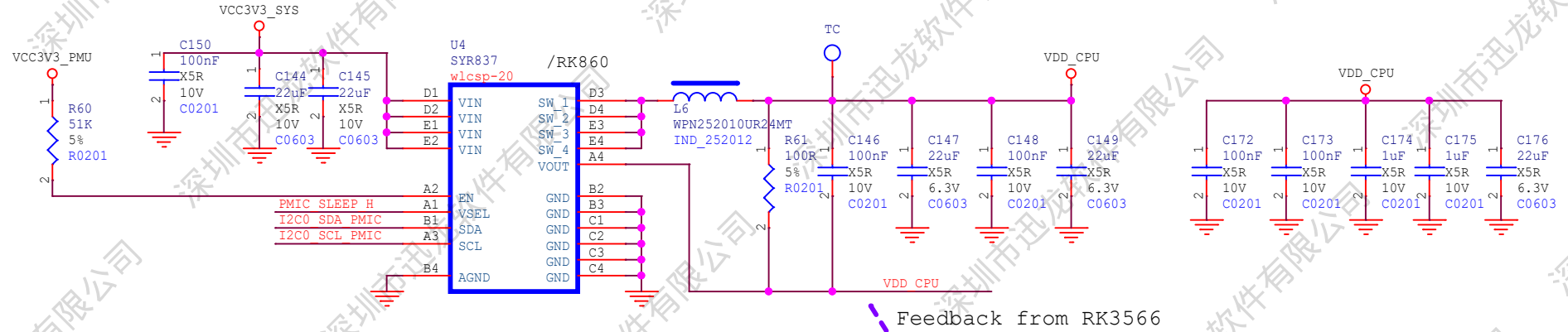


## PMIC RK809 CODEC

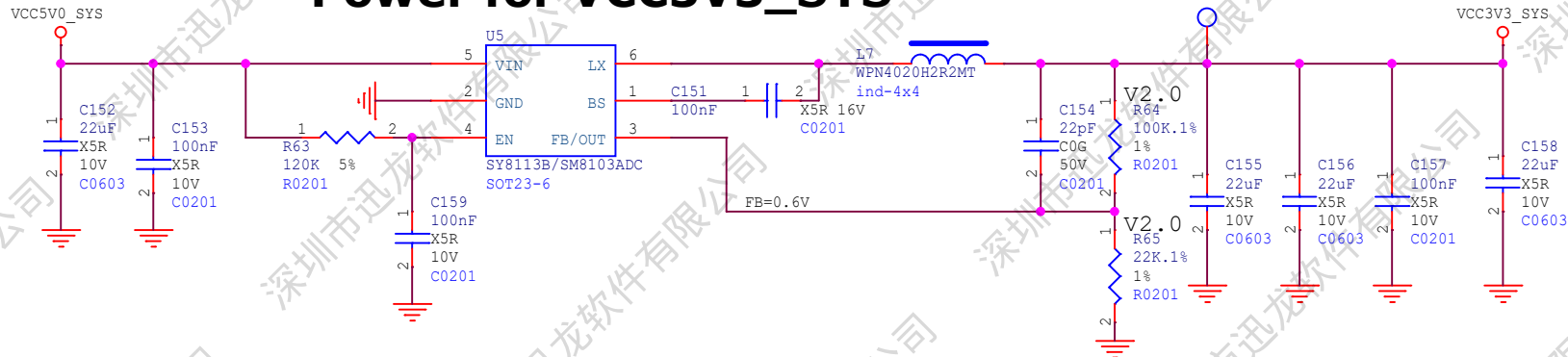


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Date:	Monday, May 27, 2024
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Of:	0

## VDD\_CPU\_EXT



## Power for VCC3V3\_SYS



Shenzhen Xunlong Software Co., Ltd

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Date:	Monday, May 27, 2024	Rev:	V2.1	
Size:	A3	Sheet:	0	Of: 0



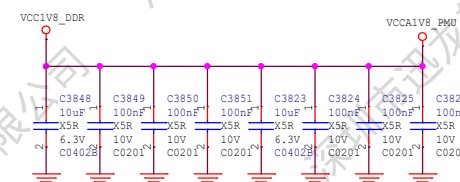
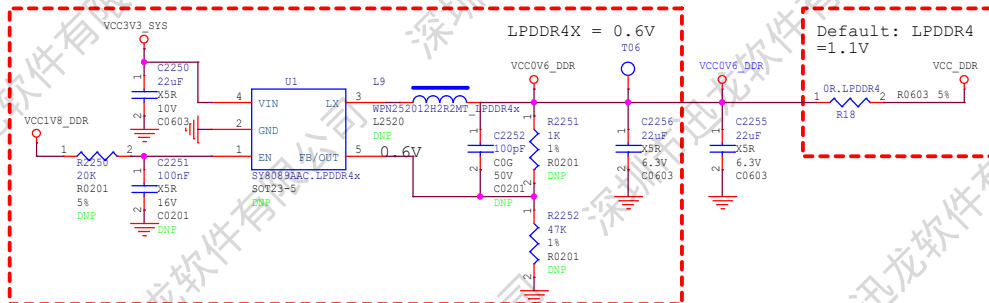
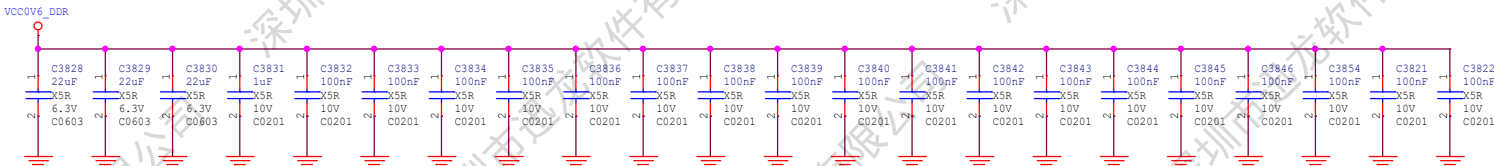
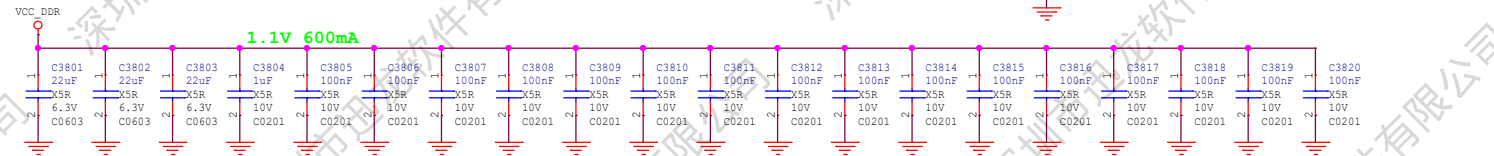
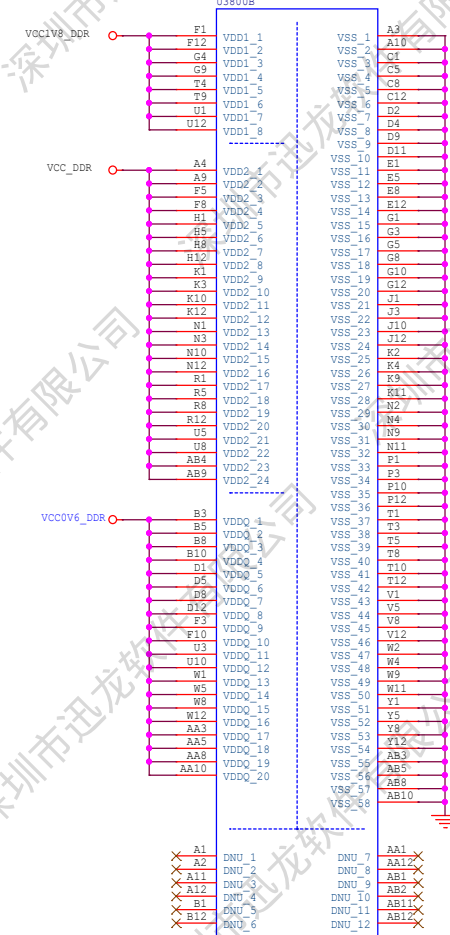
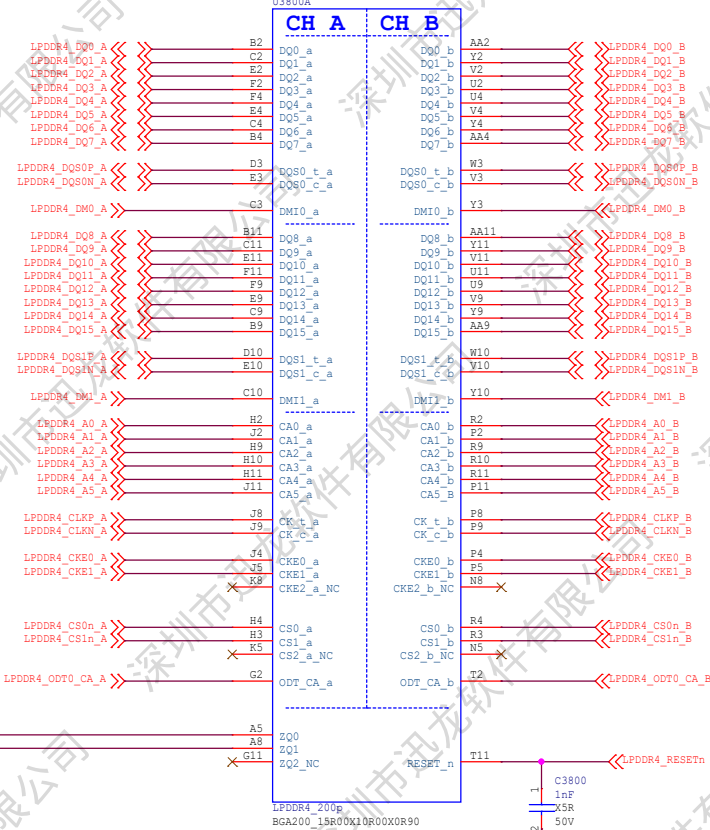
# Flash Power Manage

	VCCIO2 domain voltage: Recommend voltage value (VCCIO_FLASH)	FLASH_VOL_SEL state decided to VCCIO2 domain IO driven by default
eMMC	1.8V	FLASH_VOL_SEL --> Logic=H
Nand flash	Default 3.3V, Optional 1.8V	FLASH_VOL_SEL --> Logic=L(Default)
SPI flash	Default 1.8V, Optional 3.3V	FLASH_VOL_SEL --> Logic=L(Default)

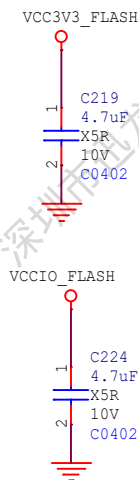
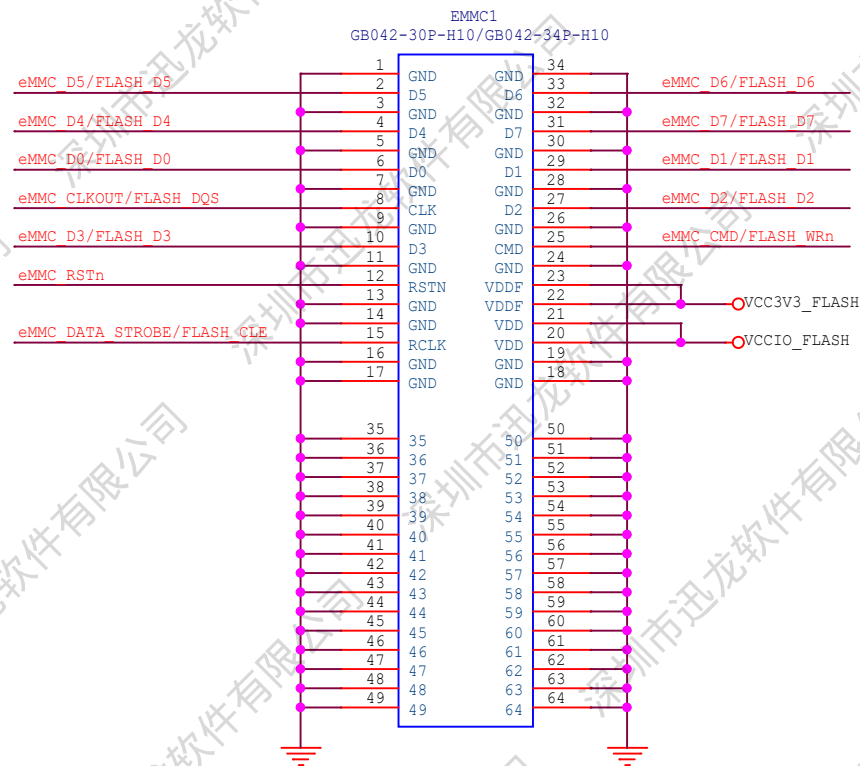
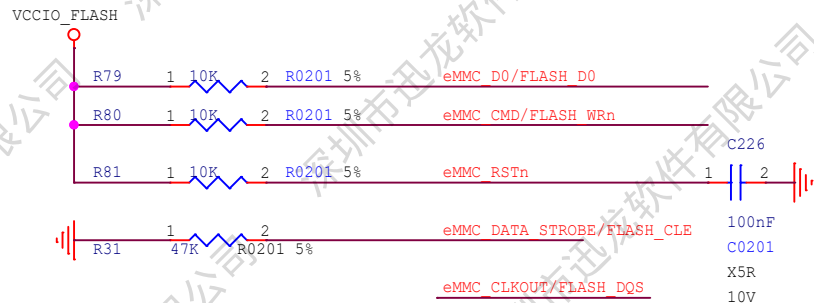
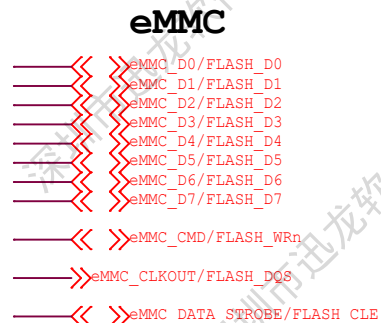


Shenzhen Xunlong Software Co., Ltd				
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File:	13.Power_Flash_Power_Manage			
Date:	Monday, May 27, 2024	Rev:	V2.1	
Size:	A3	Sheet:	0	Of: 0

LPDDR4 200B 1x32bit



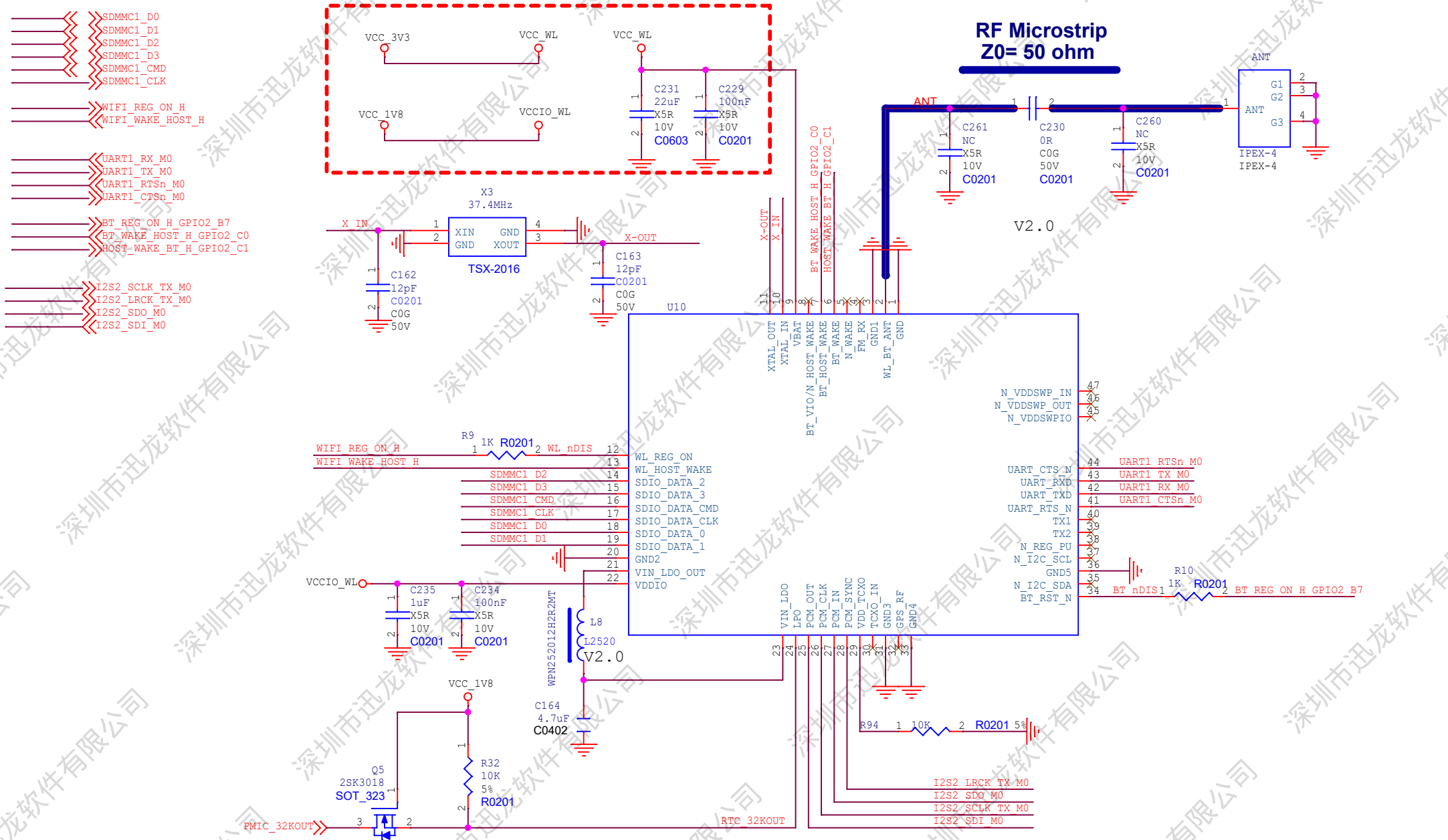
<b>Shenzhen Xunlong Software Co., Ltd</b>				
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<b>Date:</b>	Monday, May 27, 2024			<b>Rev:</b> V2.1
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Shenzhen Xunlong Software Co., Ltd					
Project:	OPI 3B				
File:	15.Flash-eMMC_Flash				
Date:	Monday, May 27, 2024	Rev:	V2.1		
Size:	A3	Sheet:	0	Of:	0



SDIO WIFI/BT Module-1T1R



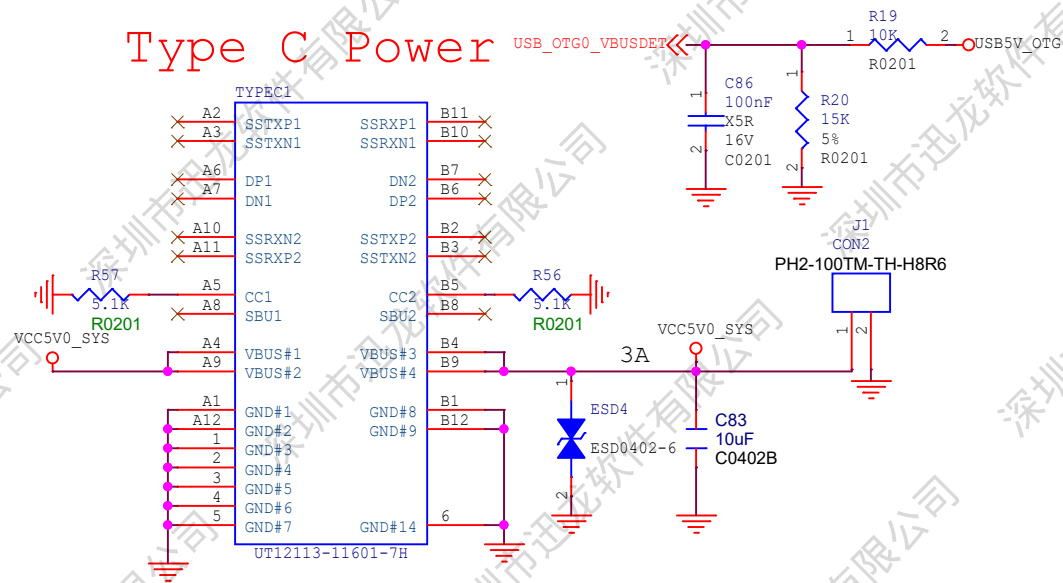
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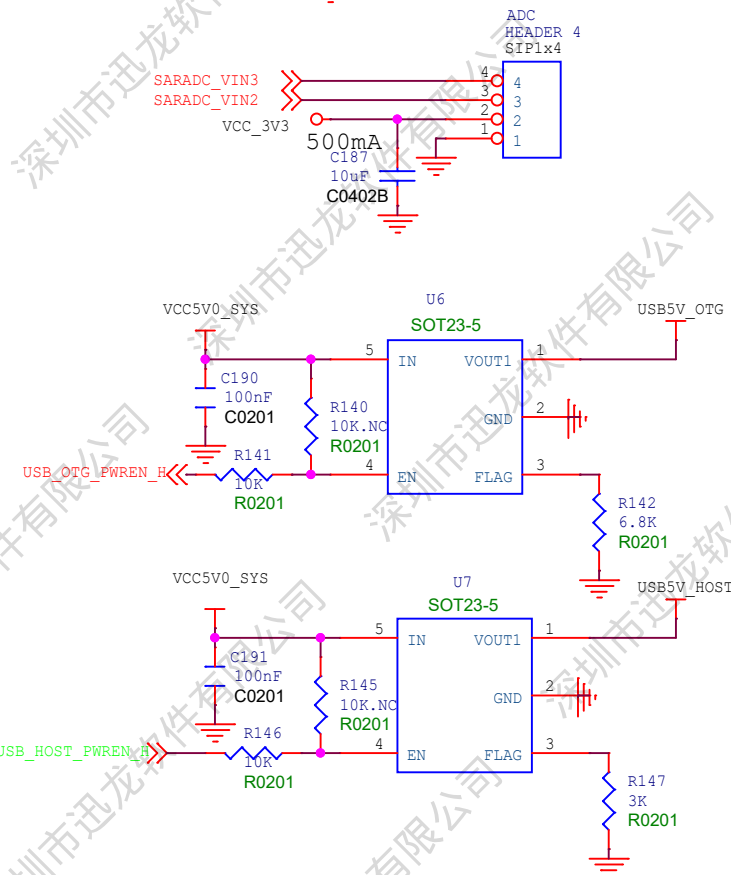
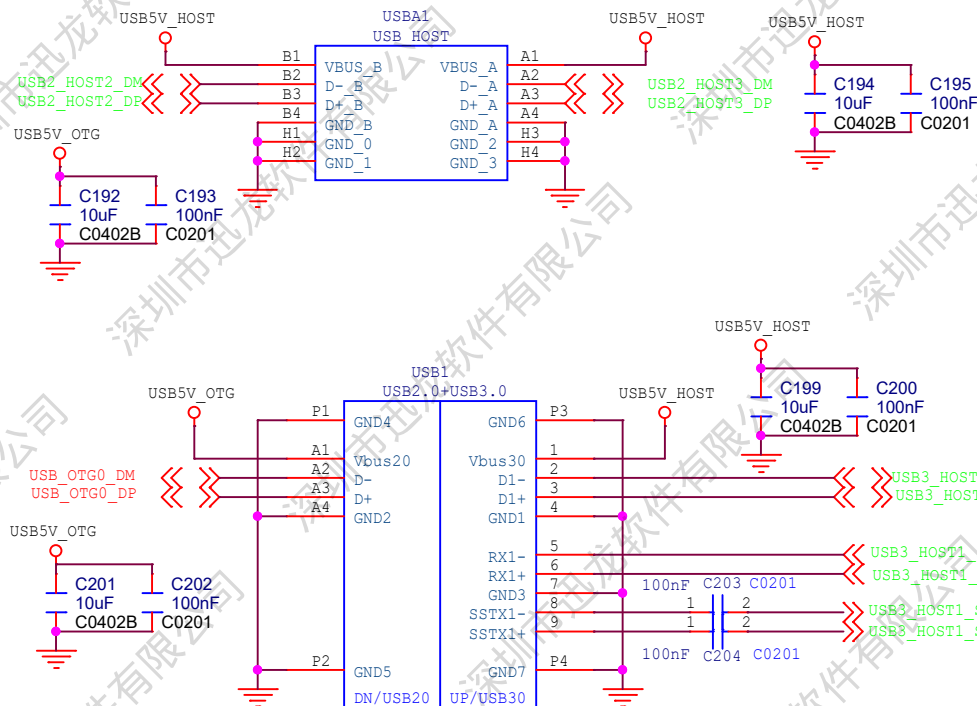




# Type C Power



# USB 2.0 X2



Shenzhen Xunlong Software Co., Ltd					
Project:	OPI 3B				
File:	21.USB_POWER/FAN				
Date:	Monday, May 27, 2024		Rev:	V2.1	
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