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EEE102-2
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Lab7 Report
FINITE STATE MACHINE

Purpose

The purpose of this lab is to design an FSM on the breadboard using logic ICs. In order to complete a functioning FSM, it is required to draw a state transition diagram, table for state variables and for outputs as well as a schematic of the gates and flip-flops.

Methodology

The design consist of 2 states, 1 input controlled by a button, 1 output and another additional output to check whether the clock signal is working or not. The outputs are shown via LEDs. After constructing the state diagram *(Fig.1)*, output tables *(Table1)* and schematic design *(Fig.2)* ; required logic gates are determined and the design is implemented on breadboard.

- **Input**

  Button:

  When pressed tells that the user switched positions (moved from position A to B), when pressed again tells that the position is again switched (moved from B to A). Pressing the button gives the output high(active high state), when it is not pressed the position don't change.

- **Output**

  Position:

  When the user is at position A it is assigned as 1 else (at B) 0.

When the input is high the output toggles and gives the opposite logic value with the next rising edge of the clock. Therefore it can also be said that the design is basically an implementation of a T-flipflop using a D flip-flop.

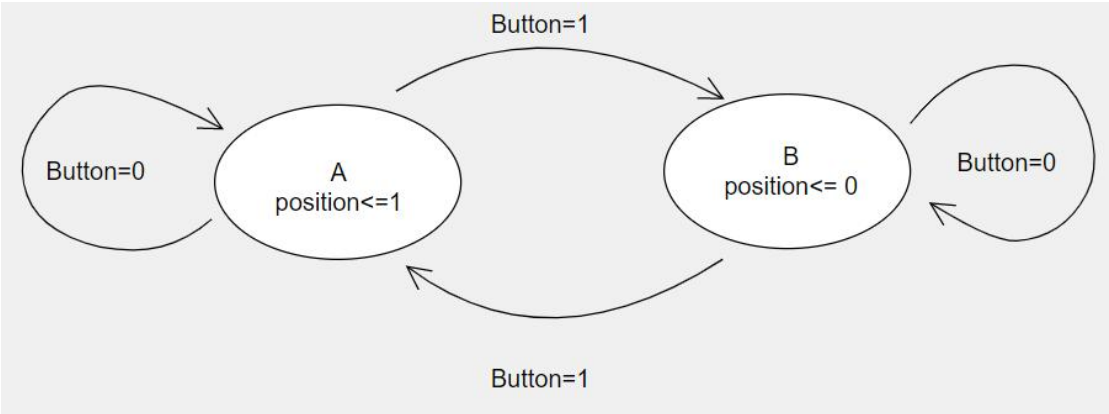

Fig.1 State Transition Diagram

Current State		Next State V		Output
	U	Button = 1	Button = 0	position
A	1	0	1	1
B	0	1	0	0

Table 1 Output Table

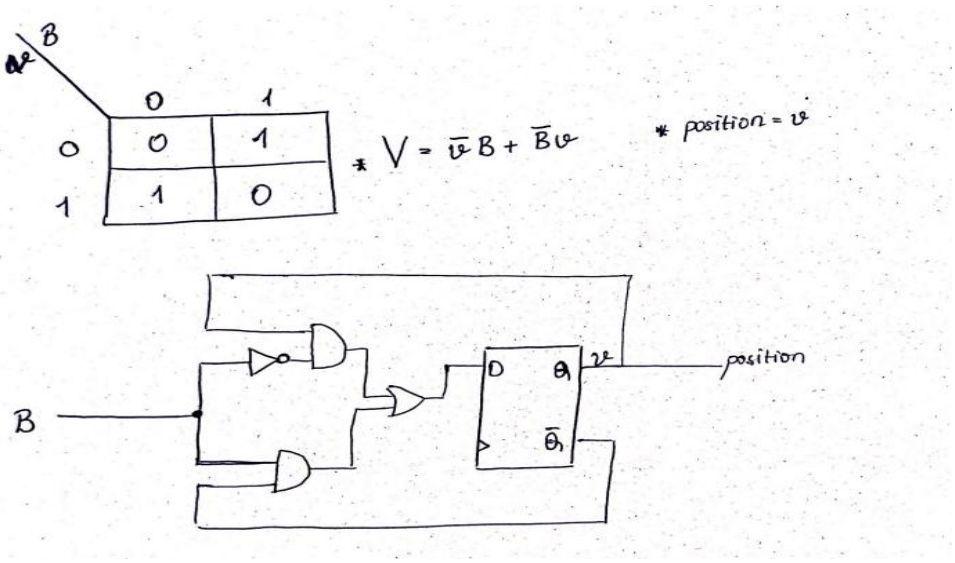

Fig.2 Karnaugh Maps & Schematic

Results

After creating the design it is implemented on breadboard as can be seen below.(*Fig.3)*

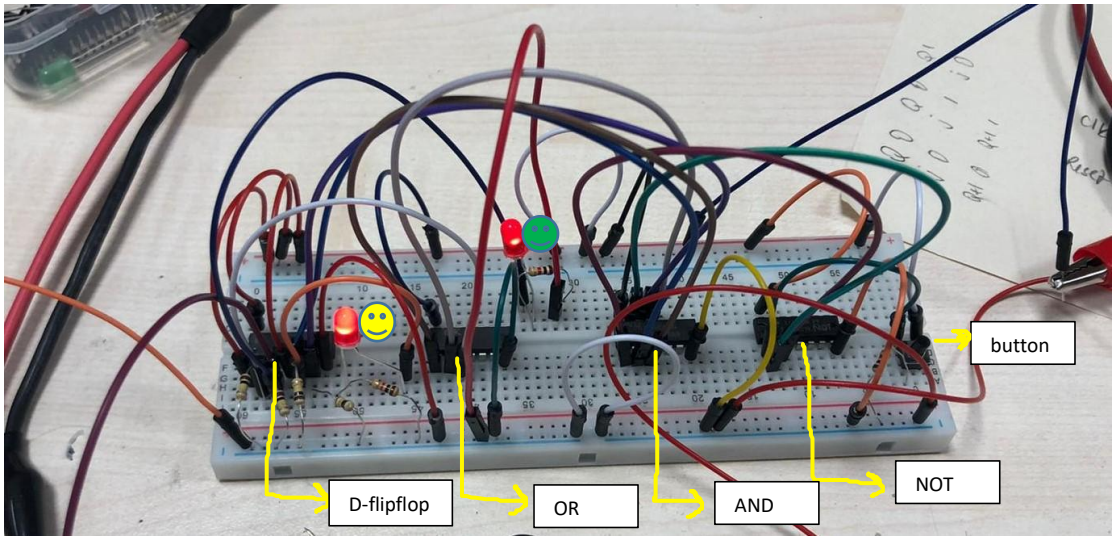

Fig.3 Design on breadboard

The results on breadborad can be seen below:

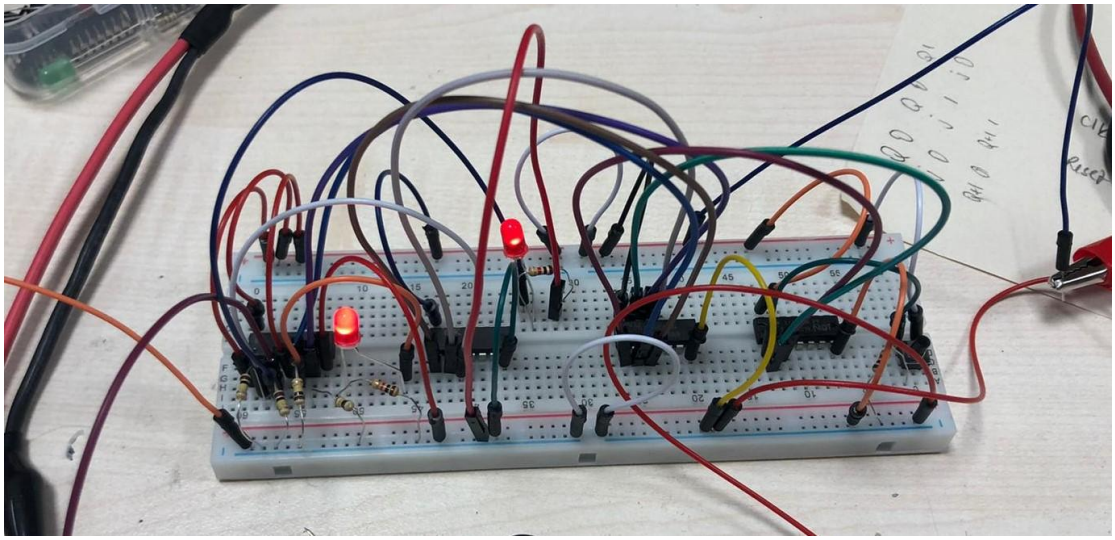

Fig.4 User is in position A -output =1

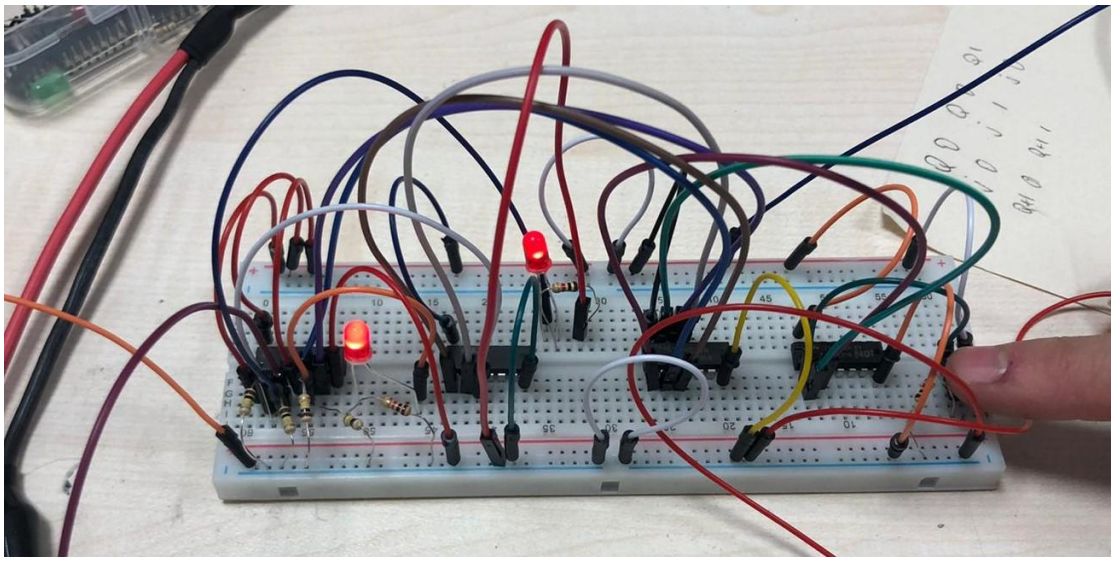

Fig.5 The button is pressed with the + edge of the clock

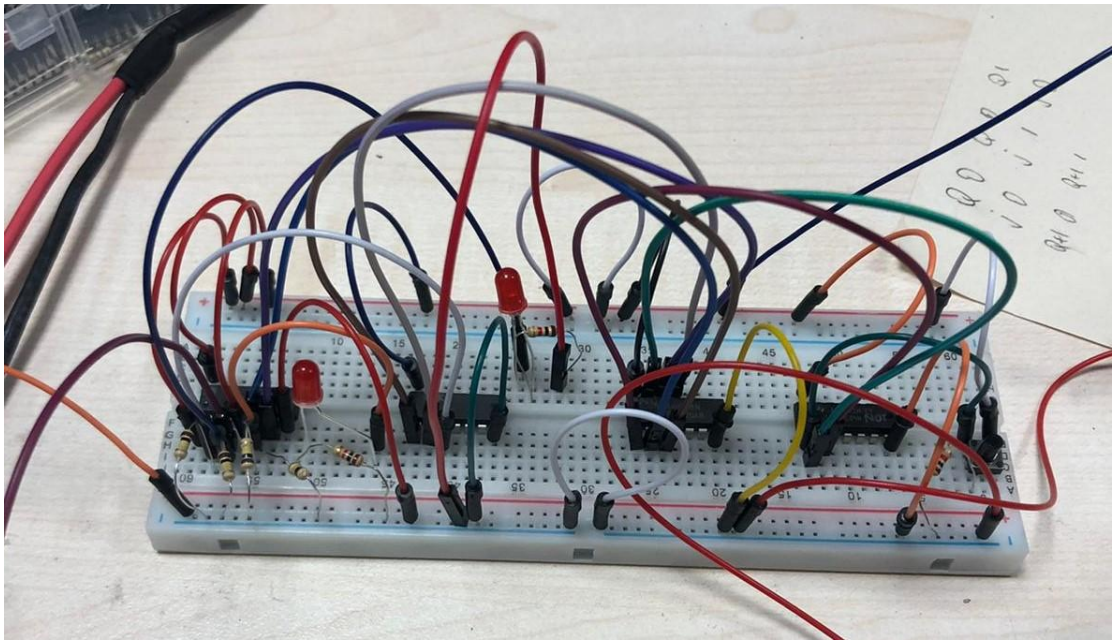

Fig.6 after pressing, user switched to position B -output =0

Conclusion

The results on the breadboard were consistent with the tables. As for the design choice a Moore machine is used to lessen the gate number. It would be better if it is implemented with a XOR gate however there isn't any in the lab. One of the most challenging part of this lab was to arrange the impedance because the signals were noisy enough that at some point the clock signal was present in the position output which prohibits the output signal. To prevent this resistors are used. Another challenge was to synchronise the push rhythm to the clock, since it toggles with the positive edge of the clock not pushing the button at that time was breaking the correct sequence.To prevent this clock frequency is changed according to push rythyhm.